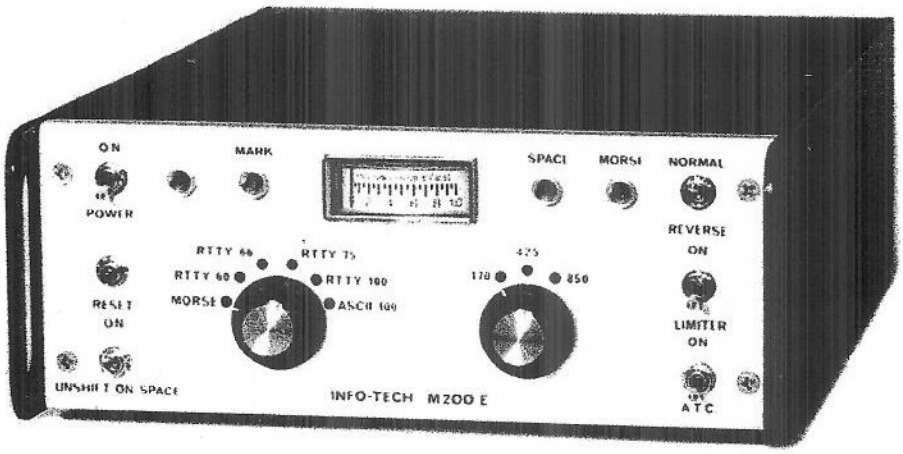
Service Manual

INFO-TECH

M-100E/M and M-200E
Trimode Converters



INFO-TECH ELECTRONIC EQUIPMENT

Digital Electronic Systems, Inc.
Englewood, Florida

#2476

INFO-TECH

M 100-E/M 200-E TRI-MODE CONVERTER
SERVICE MANUAL

CONTENTS

IC#	IC type	IC function	Circuit Function
Morse			
1A	1458	dual op-amp	input amplifier
B			IF active filter
2	796	balanced modulator	mixer
3	567	phase-locked-loop	detector
4	555	timer	local oscillator
RTTY*			
5	709	op-amp	RTTY input amplifier/limiter
6	3401	quad op amp	Mark and 170Hz shift active filter
7	3401	quad op-amp	425 & 850Hz shift active filter
8A	1458	dual op-amp	post-detection low-pass filter
B			ATC amplifier
9A	1458	dual op-amp	slicer
B			tuning aids driver
10A	1458	dual op-amp	signal inverter
B			RS-232 generator
11	3870	microprocessor	
*12	MM5303	UART	serial ASCII output generator
	or TMS6011		
	or AY5-1013		
*13	555	timer	serial ASCII output clock

* Note: On M100-E, ICs 5 through 10 and ICs 12 and 13 are not used.

Circuit Description

Morse Detector:

The Morse detector is a superhetrodyne receiver with a phase-locked-loop final detector. Although all of the signal frequencies dealt with in this circuit are within the audio-frequency spectrum, the configuration and theory of operation of the conversion portion of this circuit are identical to those of a superhetrodyne radio-frequency receiver, with the main segments of the circuit being an input amplifier, local oscillator, mixer, intermediate frequency (IF) amplifier, and detector. The fact that the detector is a digital (on or off) type rather than linear has no effect on the operation of the balance of the circuit.

Circuit Overview:

The Morse signal is amplified and mixed with a local oscillator frequency producing the sum and difference frequency outputs of the input and local oscillator signals. The sum frequency output is filtered and amplified by an active bandpass filter (IF amplifier) and fed to a phase-locked-loop (PLL) detector producing a digital output corresponding to the presence of an input signal of the proper frequency.

The normal IF frequency, which must be the locking frequency of the PLL, is 8500Hz. In order to obtain a sum frequency output of the mixer with a 1000Hz input signal, the local oscillator must be set to a normal 7500Hz. The optimum input frequency may be adjusted slightly by varying the frequency of the local oscillator with the fine tuning control. The range of input frequency may also be adjusted by setting the coarse local oscillator frequency using the formula: $f_{lo}=567-f_{in}$.

Circuit Operation:

The input signal is fed to the Morse input amplifier/buffer (IC 1A) through R2. R3 provides degenerative feedback for DC stability and sets the gain of the amplifier at approximately 4. The output of IC 1A is coupled through C1 and R4 to the non-inverting signal input of the mixer. The signal is attenuated by the divider formed by R4 and R5 which is required for impedance matching.

The other (local oscillator) signal input to the mixer is generated by IC4, a timer IC configured as an adjustable oscillator. At power on, C4 begins to charge through the series combination of R's 20 through 23 until the voltage on the capacitor, which is connected to pins 2 and 6 of IC4, which are the threshold and trigger inputs to the timer, reaches approximately 8 volts. When this occurs, the discharge output at pin 7 of IC 4 turns on, reducing the voltage at pin 7 to 0 volts, and C4 begins to discharge through R's 20 through 22. After C4 has discharged to approximately 4 volts, the discharge output at pin 7 turns off and C4 again charges through R's 20 through23. This cycle is repeated at a rate determined by the values of C4 and the combination of R's 20 through 23 with R20 being the coarse frequency adjust and R21 the fine frequency (fine tune) adjustment. Pin 4 of IC 4 is the enable input and is hard-wired to +12v. Pin 5 is a control voltage input which is not used in this circuit, but which must be AC bypassed to ground by C5.

The voltage across C4 which is nearly a triangle waveform from the charge/discharge of this capacitor, is buffered by Q1 in an emitter-follower configuration to minimize the loading effects of the output circuit on the frequency determining components. R17 provides a path to ground for the DC emitter current from Q1. The buffered output of Q1 is coupled through C6 to an RC low-pass filter formed by R18 and C7, which converts the triangle waveform to a nearly sine-wave signal which is further attenuated by a divider of R19 and R15 which provide impedance matching and level compatibility to the inverting carrier input to the mixer.

The signal input at pin 1 of IC 2 and the carrier input at pin 10 of IC 2 are mixed in IC 2, which is a double-balanced modulator/ demodulator, providing both sum and difference frequency outputs at pins 6 and 12. The -12 volt supply bus is reduced to approximately -9 volts from the drop across zener diode D3 and filtered by C2, to provide the negative supply to pin 14 of IC 2. Resistors R5, 6,7,8, and 9 form a divider network which sets the bias ratio to the inverting and non-inverting signal inputs, and R7 is adjusted for a bias ratio level which minimizes the carrier signal component at the output terminal. R11 determines the gain of the mixer stage. R12 and R16 provide collector supply to the open-collector output transistors, while R10 sets the internal operating bias. The voltage divider formed by R13 and R14, with C3 as a filter, provides the bias voltage of 6 volts for the carrier inputs at pins 8 and 10 of IC2.

the sum and difference frequency output at pin 6 of IC 2 is coupled through C8 to the input of an active bandpass filter formed by IC 1B, R24, R25, R26, C9 and C10 in a second order MFB configuration. This filter is tuned to pass only the sum frequency output of the mixer, which is approximately 8500Hz.

The output of the active filter intermediate frequency amplifier is coupled through C11 to the input (pin 3) of the phase-locked-loop detector (IC3). The phase-locked-loop has an internal oscillator with a free running (with no signal input at pin 3) frequency determined by the time constant of R27 and C12. This oscillator operates on a capacitor charge and discharge time similar to the operation of the local oscillator circuit of IC 4. Whenever the frequency of the signal input at pin 3 is sufficiently close to this free-running frequency of IC 3's internal oscillator, this internal oscillator will swing in frequency to match the input frequency, and the two will become'phase-locked'. When this occurs, the open-collector output transistor at pin 8 of IC 3 will turn on, pulling this pin to ground, indicating that a 'lock' has been achieved. The +12 supply bus is reduced to +9v through zener D4 and further filtered by C15 and C19 to provide the positive supply voltage for IC 3.

C 13 and C14 set the nominal bandwidth and operating speed. When a lock condition occurs, pin 8 goes to 0 volts pulling pin 3 of the 3870 low, this is the Morse input to the microprocessor, it also turns on Q2 through R29 causing current to flow through R30 and LED D7 turning that indicator on. The voltage at pin 8 of IC 3 may also be pulled low by a ground at the 'Morse Aux' input through R28. Diodes D5 and D6 are protection diodes preventing this input to the 3870 from exceeding its maximum ratings.

RTTY Demodulator:

The RTTY demodulator is a moderatley sophisticated detector utilizing two of four high Q active bandpass filters in a voltage differential envelope detector configuration with active low-pass post-detection filter and automatic threshold control to correct for signal bias distortion.

Circuit Overview:

The RTTY input signal, which is audio-frequency-shift-keyed (AFSK), is amplified in a high performance operational amplifier, which is externally compensated to provide the appropriate frequency response characteristics. The output of this amplifier is simultaneously fed to four active bandpass filters each tuned to a different frequency: one for the standard mark frequency,and one each for the three standard space frequencies. The output of the mark filter and one of the three space filters are detected to form a plus or minus voltage swing dependent upon the input frequency. This detected output voltage swing is filtered and then passed through a bias-correcting stage to slicing and inverting stages to drive the microprocessor input, monitor lines and loop keying circuit. The plus-minus output of the filter is also fed to a buffer to drive the tuning circuits.

Circuit Operation:

Input signals pass through R31 to diodes D1 and D2 which provide input clamping to protect IC 5 from damage due to high level signals or transient pulses at the input. After the protection circuit, the signal is coupled through C 17 to the inverting input of IC 5, a 709 high performance operational amplifier which serves as the input amplifier/limiter. Resistor R37 provides switch selectable inverse feedback for this stage. With the limiter switch on, the output amplitude of the limiter will be constant for any signal from 1 mv p-p to the maximum allowable input voltage. R33 provides a DC current path for the inverting input of IC 5, while R34, R35 and R36 are a means of adjusting the bias on IC 5 so that its output is at the center of its linear operating range. The combination of R38 and C19 determine the amplifier input circuit frequency characteristics, and C18 sets the output frequency compensation.

The output of IC 5 is passed through an RC low-pass filter made up of R39 and C20, to remove the high harmonic content of the square-wave limited output of IC 5, and coupled through C21 to the inputs of the four active filters.

Except for resistor component value variations, the circuit configuration and operation are identical for the four active filters. Each filter is a variation of a second order MFB active bandpass filter, with an additional amplifier stage to provide controlled positive feedback which greatly enhances the Q of the basic filter. The table below shows the components used for each of the four filters:

shift	filter frequency	IC	capacitor	resistor
all	2125	6A,B	22,23	40-47
17Ø	2295	6C,D	24,25	48-55
425	2550	7A,B	26,27	56-63
850	2975	7C,D	28,29	64-71

The output of the mark channel active filter is coupled through C39 and R100 to one channel of the 'scope' output jack for tuning scope applications. The mark output is also coupled through C30 to D8 which is used as a positive half-wave detector. R72 provides a ground reference at the junction of D8 and C30. The positive half wave detected output is fed through R73 to the inverting input of IC8A where it is mixed with the negative half-wave detected output from the selected space filter. The shift switch selects which one of the three space filters are to be used at any one time and the output of the selected filter is fed to the scope jack through C40 and R101,and to the input of IC8A through network C31, R74, D9 and R75. This network works similarly to the one described above for mark except that the detector is a negative half-wave type.

The mark and selected space active filter detected outputs are combined at the inverting input of IC8A which serves as a low-pass post-detection filter and amplifier to enhance the average D.C. differential between the mark and space detected signals, and to reduce the amount of ripple from the half-wave input. Resistors R76 determines the D.C. gain of the filter while the parallel combination of R76 and C32 sets the A.C. gain of the stage. The output of IC8A, which is a negative voltage for mark, and positive for space, drives the ATC averaging circuit, ATC amplifier input and also the tuning indicator buffer.

When the output of the IC8A swings positive, C33 is charged through D10 and temporarily stores approximately the peak positive voltage of this signal.Capacitor C34 stores the peak negative voltage reached at IC8A's output after being charged through D11. Capacitors C33 and C34 slowly discharge throughR77 and R78 which form a voltage divider. At the junction of these two resistors will be a voltage equal to one half of difference between the voltage on C33 and C34, or half of the average voltage at the output of IC8A. This voltage is then fed to the non-inverting input of IC8B when the ATC switch is on (in the open position). When the ATC switch is off (closed) the non-inverting input to IC8A is connected directly to ground. The output of IC8A is also connected to the inverting input of IC8B through R81. This input, along with the non-inverting input, which is either 0 volts or the ATC correcting voltage described above are amplified by IC8B whose gain is set by R82 to be one.

The effect of this circuit is that, as the relative tuned strength of the mark and space signals change, the output of IC8A will not swing equal amounts both positive and negative. By applying the ATC correction voltage at the input to IC8B, along with the signal voltage, the output of IC8B will swing equal voltages positive and negative with the signal centered about zero volts.

The bias-corrected signal at the output of IC8B is fed through R83 to the input of the slicer op-amp (IC9B) which has positive feedback through R84 to provide switching hysterisis to eliminate switching spikes as the input signal crosses zero, and to provide some noise immunity. Due to the positive feedback, the output of IC9B will not switch until the input to this stage (the output of IC8B) reaches approximately 2.2 volts of the opposite polarity of the output of IC9B.

The square-wave output of IC9B provides the driving output for the normal sense mode and also the input to IC 10B which inverts the square-wave for the reverse sense mode.

The selected driving output, either normal or reverse, is fed through R89 to the 'R/A Aux' input/output connector. This connection, when used as an output will provide a high impedance digital output of the received signal. This point may be used as as input by connecting a low impedance drive here, which will override the demodulator output, which must pass through R89, and drive the output keying circuits. This is the means used to monitor local keyboard signals when transmitting.

The signal at the R/A monitor point keys Q3 through R90, to provide the RTTY input signal to the microprocessor at pin 4 of IC 11. This signal also goes through R91 to Q4 which is an emitter-follower driving Q5, the high voltage output transistor for keying the RTTY loop. D18 prevents the R/A monitor line from swinging negative and D19 protects Q5 in the event that the connections to the RTTY loop jack are of the wrong polarity.

The output at pin 7 of IC8B also drives the inverting input of IC9A which is the tuning aid buffer/driver. This stage is set for a gain of 1 by R85 and R86. The output is fed through R88 to the Mark and Space LED's. When this signal goes positive, the Mark LED conducts and when the output swings negative the space LED conducts. The output is also connected to a full-wave bridge of D12 through D15 which provides positive current through R87, which is the meter adjust pot, and the meter regardless of the output polarity of IC 9A.

The Microprocessor:

The device which accepts, processes and converts the Morse or RTTY signals to ASCII data for loading to the video module and UART, is a 3870 single-chip microprocessor. The main segments of the microprocessor are the CPU, 64 bytes of RAM, 2 k (2048) bytes of ROM and 32 input/output lines.

This microprocessor replaces the equivalent of hundreds of individual integrated circuits and it is beyond the scope of this manual to explain in detail all of the inner workings or operations of this device. Additionally, such information would be of little assistance in the diagnosis or correction of operating defects.

For this part to operate under noraml conditions (the device not being defective) the requirements are: power supply (+5v), ground, a clock and appropriate input (data) and control signals. Power supply; +5 volts on pin 40 and ground on pin 20 are self-explanatory, the rest of the signals will be described below:

Clock:

The 3870 has an internal oscillator circuit which requires only a crystal to be connected between pins 1 and 2. While the 3870 will operate with a crystal between 1 and 4MHz, proper RTTY timing will only occur with a 4MHz clock crystal.

Data Input:

There are two seperate data input lines to the 3870, one for Morse (pin 3) and one for RTTY (Baudot and ASCII) (pin 4).
The appropriate levels for the Morse input are no tone = +5v;tone (key down)=0v. The generation of this signal from the audio input is described above. At the RTTY input, the required levels are mark=0v; space=+5v. The description of how this signal is obtained is also above.

The microprocessor only examines one of these two inputs at a time. If the converter is in the Morse mode, the level, or any changes in the level at the RTTY input are completely ignored and vice-versa. In order for there to be any output, there must be appropriate signal level transitions at the appropriate input, depending upon what mode is selected.

Control Signals:

Mode Selection:

The operating mode and speed are selected by connecting to ground one or less of the mode control lines pins: 6, 16, 17, 18, and 19). This is done with the mode switch and operation is determined according to the following table:

grounded pin	mode	(data bit)
none	Morse	-
19	Baudot 60 wpm	4
18	Baudot 66 wpm	5
17	Baudot 75 wpm	6
16	Baudot 100 wpm	7
6	ASCII 110 baud	3

When one of these pins are selected (tied to ground) the voltage at that pin will be 0 volts; when not selected a pull-up device internal to the 3870 will raise the pin voltage to +5 volts.

Under normal conditions no more than one of these lines should be low (none low for Morse operation). If more than one line is held low. the operating mode will be that one corresponding to the lowest data bit value of those held low. For example, if both pins 16 and 19 are held low, selecting both 60 wpm and 100 wpm Baudot, the operating mode will 60 wpm (data bit 4) rather than 100 wpm (data bit 7). If proper operation cannot be obtained in one or more modes, it is advisable to check for the appropriate levels on the mode select pins.

It is important to remember that under some circumstances it is necessary to reset the microprocessor when changing modes. If the converter is operating in the Morse mode, the function switch may be turned to any position or, any or all of the function select lines may be pulled low, and the converter will remain in the Morse mode. In order for the converter to change from the Morse to an RTTY mode the microprocessor must be reset with one of the mode select lines pulled low. Once the converter is in one of the RTTY modes, it may be switched back and forth among any of the RTTY modes by simply changing the setting of the mode switch without requiring a reset. In order to return the Morse mode, however, a reset is required with all of the mode select lines high.

If the converter is in an RTTY mode and all of select lines are high, from the mode switch being in the Morse mode, or between positions, the processors converting operations are suspended until one of the mode select lines are pulled low, resuming RTTY operation, or until the processor is reset, initializing Morse operation.

The reset pin of the 3870 (pin 39) is connected to the reset button of the converter through R95 paralled with C38. This configuration causes a single, very short, low pulse at pin 39 each time the reset button is pressed, as opposed to the several low pulses that would result from the contact bounce in this type of switch. It is important that only one low pulse appear at the 3870 reset pin each time the reset button is pressed because when a reset occurs in an RTTY mode, whether or not a speed readout occurs depends upon the number of reset pulses which occur within a given length of time. If this reset input circuit (R95, C38) does not generate a pulse or a pulse of sufficient pulse width to effect a processor reset it may appear that IC 11 is defective. This may be verified by directly grounding (momentarily) pin 39 of IC 11. If this results in normal operation, the problem is in the reset circuit and not the processor.

There is only one other control that is required for normal operations and that is the external interrupt line at pin 38 of IC 11. This pin must be always high on the M-100E, and will only pulse low briefly on the M-200E. If this line is held low, the processor will cease normal operation during the reset initialization process. On the M-200E this can be caused by a defect in the serial ASCII output circuitry. If this is the case, the UART (IC 12) may be removed and normal video operation will be resumed after another 'reset'. See the section below for servicing the serial ASCII output circuit.

Morse Speed Control Lines:

A portion of the Morse converter program contains a digital low-pass filter which determines the minimum input pulse width, either high or low, at the Morse input pin that the processor will recognize as a valid input transition. This minimum time interval determines the maximum noise pulse input width allowable without performance degradation, and also the maximum receiving speed. The filte timing is set by the level on six of the processor control pins at reset in the Morse mode. These controls are pins 28 through 33 of IC 11. The compliment (opposite level) of the levels on these six pins are read by the processor as a binary number, which is used as a scaling factor for the filter, with the binary weighting shown in the following table:

pin-	28	29	30	31	32	33
weight-	32	16	8	4	2	1

To determine the minimum recognizable pulse width, add the weight values for each pin which is connected to ground, subtract one and multiply the results by 2 ms. Units are shipped from the factory with pins 31, 32, and 33 grounded, giving a time of: $[(4 + 2 + 1) - 1] \times 2$ ms = 12 ms.

To compute maximum speed use the following formula:

$$\text{speed} = \frac{.6}{t}$$

where speed is approximate maximum receiving speed (in wpm) and t is the time computed above, expressed in seconds.

Another control line input to IC 11 (pin 26) determines whether or not the converter will provide the 'unshift-on space' feature when in a Baudot RTTY mode. This function will be provided when the unshift-on-space switch is closed, that is, when the level at pin 26 is 0. The effect of this function is that whenever a 'space' character is received, the converter will change to lower case, just as if both 'space' and 'letters' characters had been received.

There is also a control input at pin 5 of IC 11 which indicates to the processor which type of video module is used on the converter, either 32 X 16 or 72 X 16. Pin 5 should be high for the 72 X 16 format and low for the 32 X 16.

Video display outputs:

There are eight lines connecting the processor to the video display module. These are pins 22 through 25 and 34 through 37, which present a six bit ASCII code, along with data ready and display scroll signals, to the display module. Pin 37 is the video load strobe which will pulse low each time a new character has been received and/or processed and is ready and valid on the six data lines to be loaded to the video display. Pin 25, when low at the same time as a strobe pulse, will cause the video display to scroll up one line.

Serial ASCII Output:

Pins 8 through 15 of IC 11 contain full ASCII code of the character to be output, with pin 7 an active low data ready strobe. IC 12 is a UART (Universal Asynchronous Receiver/Transmitter) with the transmitter section used to convert the parallel ASCII output from the processor to serial ASCII. Again, it is beyond the scope of the manual to describe in detail the operation of a UART. When pin 7 of the 3870 pulls pin 23 of IC 12 low, the data on IC 11's pin 8 through 15 are loaded into the UART, and the serial output begins, appearing at pin 25 of IC 12. Pin 22 of IC 12 signals the processor when it may be loaded with a new character. The clock for the UART which is fed in at pin 40 comes from the square wave output of IC 13, a 555 timer connected as an oscillator. The frequency of this oscillator is determined by the charge/discharge time constant of R97, R98 and R99 and C35. R 99 is adjusted so that the oscillator frequency is 16 times the desired baud rate output. For a more detailed description of the operation of this type of circuit refer to page 3 . The serial output from pin 25 of IC 12 drives a loop keying circuit identical to that for the demodulator loop, and also the inverting input of IC 10A which converts the TTL level output to RS-232 compatible levels.

Morse Signal Waveforms-Figure 6

A series of important waveforms for the Morse detector circuit are shown in figure 6, A-H. The wafeforms are shown for the character "A", which with the timing aligned vertically for those signal dependant upon the input. As a result of this alignment, not all of the individual signals are shown to scale.

Fig A shows the waveforms for the input signal, which should be at least 100 mv p-p. Pin 1 of IC 1A should be the same waveform as the input except that it will be inverted, and its amplitude will be approximately 4 times greater than the input.

The signal at pins 6 and 2 of IC 4 (the local oscillator signal), is shown in fig 8. The level of this signal should be 4 volts p-p (from +4 to +8 volts), at a frequency equal to the local oscillator frequency which should be (F_{567}-F_{in}). The same signal should be at the emitter of Q1, with only slight attenuation and downward level shifting.

At pin 2 of IC 2 this oscillator signal, after passing through the low pass filter, (R18, C7) will take on the apperance of Fig C and will be attenuated (by R19, R15) to a level of only 100 to 150mv p-p, and biased about +6v.

The output at pin 6 of IC 2 is biased at +6 to +8 volts with an AC component dependent upon the input signal. With the carrier properly nulled, and no input signal, there should be less than 50 mv p-p of signal at this output. With an input signal in the proper frequency range, this output will appear as that in Fig D, with the p-p level output proportional to the input signal amplitude. A minimum of 100 mv is required at this point, with normal input signal levels (approx 1 volt p-p) yielding 600-700 mv p-p outputs. The frequency components of this signal are the sum and differance frequencies of the input and local oscillator signals. These are difficult to evaluate using a scope and impossible to determine using a counter. This output is coupled to the active filter IF amplifier.

The output of the active filter at pin 7 of IC 1B will be a waveform similar to that shown in Fig E. with some variation (normally less than 50%) in the p-p output during the on time. The absolute signal level at this point is also a function of the input signal amplitude, with 700 mv p-p being normal for a 1 volt p-p input signal. The frequency of this signal should be the required frequency for a PLL lock (approximately 8500Hz). The output of IC 1B is biased at 0 volts.

The output from IC 1B is fed to the signal input (pin 3) of IC 3 which is internally biased at 2 volts. Fig G. shows the signal at pin 5 of IC 3 which is the square wave signal that switches between 0 and 8 volts to charge and discharge C12 through R27. The frequency of this signal is the PLL internal oscillator frequency. Fig H. shows the charge/discharge waveform of C12 which is applied to pin 6 of IC 3. The charge/discharge range is from + 3 to +5 volts, and the frequency is the same as at pin 5.

Note: When an input signal is present at pin 3, the PLL oscillator frequency will change in attempt to match the input frequency, so during operation it is normal for this frequency to fluctuate.

The internally biased voltage on pins 1 and 2 is between +6 and +7 volts.

When a lock condition occurs in the PLL, pin 8 of IC 3 switches from + 5v to 0 volts as shown in Fig F. It is normal for there to be a brief period of rapid switching between +5 v and 0 each time the PLL locks , before the output stabilizes at 0 volts. This time should not exceed 5 ms.

RTTY Demodulator Waveforms-Figure 7

The waveforms in figure 7 A-J show the normal signals at key points in an operating demodulator. The patterns are shown for space-mark-space transitions with timing aligned vertically. Due to this alignment, and for clarity all signals are not shown to scale.

Fig A. depicts the AFSK input signal switching from high (space) frequency to low (mark) frequency, and back high again.

Fig B. shows the output of the limiter (at pin 6 IC 5) for the same input signal. This output is of the same frequency as the input and will be approximately 20 volts p-p (limited) for any input signal greater than 80 mv (with limiter switch on). This output is biased at 0 volts (adjusted by R35 with limiter on).

The output of the low-pass filter, at the junction of R39, C20 and C21 is shown in fig C. For a limiting signal, the voltage at this point will be approximately 8-10 volts p-p biased at 0 volts.

The outputs of all eight op-amps in IC 6 and 7 and biased at approximately +6 volts.

The response characteristics of the mark and space active filters are shown in fig D. and E. respectively. When the input signal frequency does not correspond to the appropriate filter, there should be little or no signal at the filter output (2 volts p-p or less).

When the input frequency matches the active filter frequency, the filter output will be 7 to 9 volts p-p.

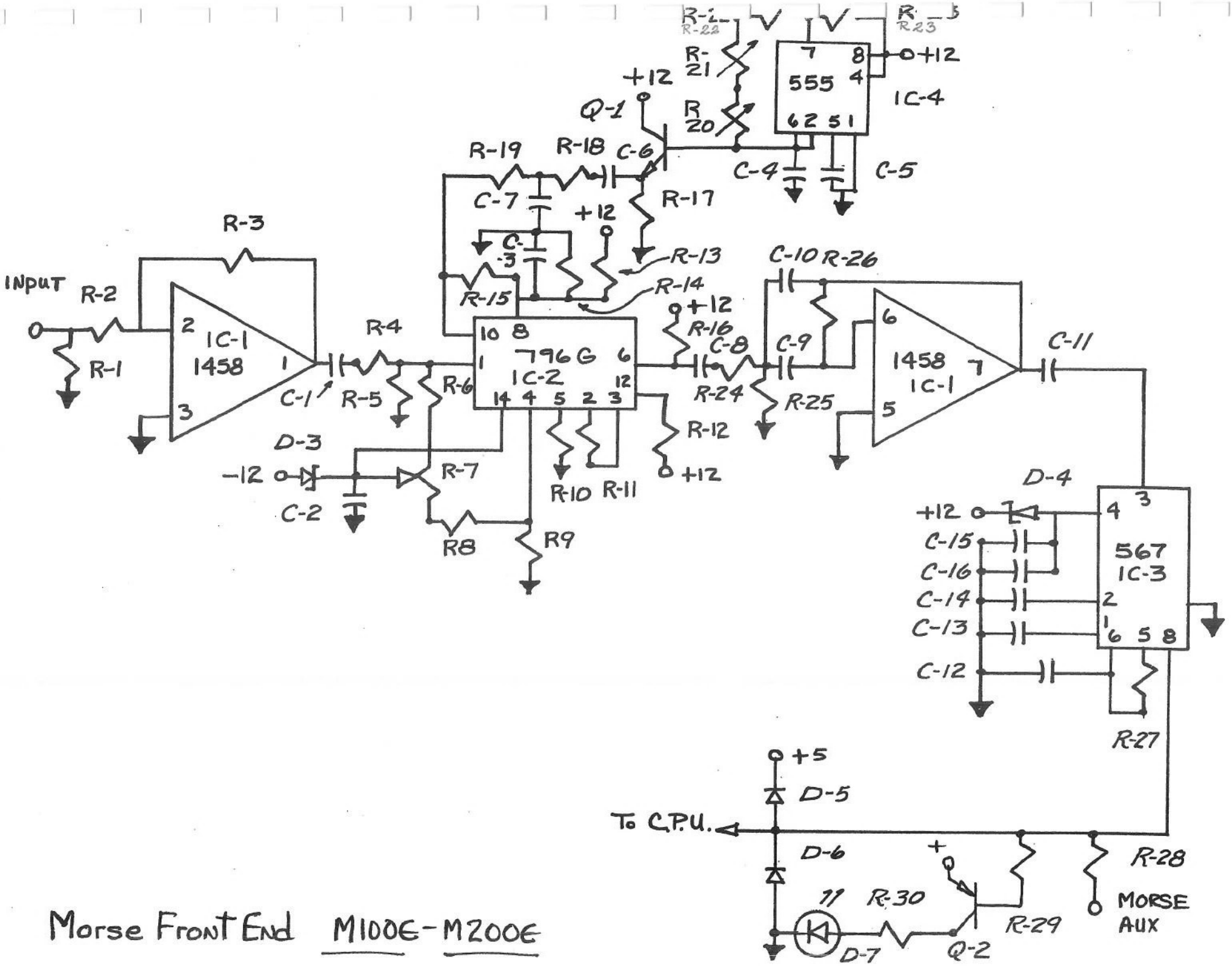
Figure F. shows the positive half wave detector output at the junction of D8 and R73. This signal is biased at 0 volts and pulses to +2 to 3 volts when the mark filter is at full output. Fig G. shows the negative half-wave detector output at the junction of D9 and R74. This point is also biased at 0 volts and pulses to -2 to -3 volts when the selected space filter is at full output.

The output of the mixer/post-detection low-pass filter at pin 1 of IC 8A is biased at 0 volts. With a signal input, it will swing between +10 and -10 volts shown in Fig H.

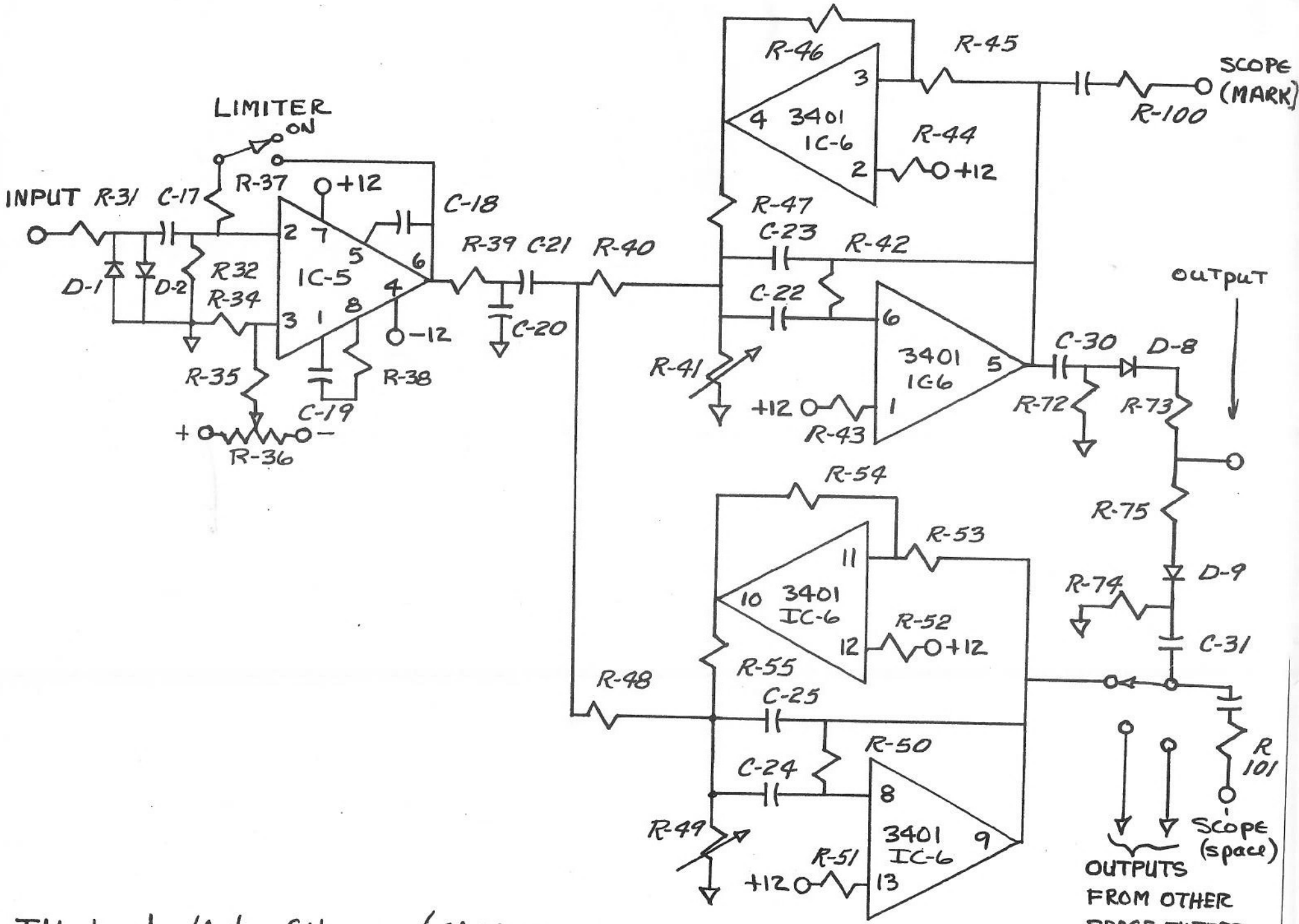
Fig I. shows the slicer/output (pin 7 of IC 9B). Note that the signal is a nearly perfect square-wave that the level transition does not occur until the output of low-pass filter (Fig H.) goes to approximately 2.2 volts of the opposite polarity of the present slicer output. Fig J. shows the inverted slicer output at pin 7 of IC 10B.

Figures 8A through E demonstrated the effect of the ATC circuit on a signal with an uneven and varying mark to space signal strength ratio:

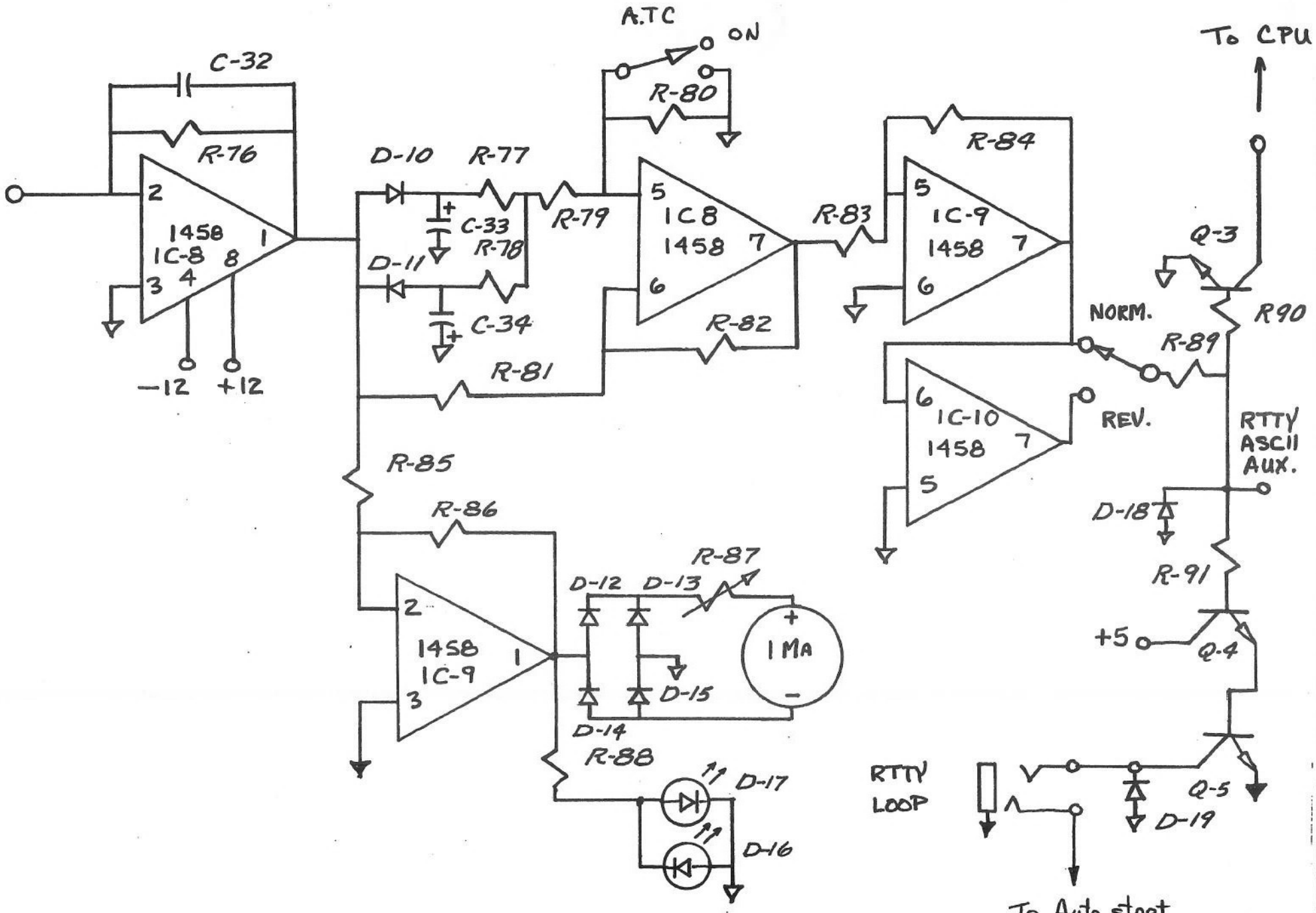
a. Post detection low-pass filter output (pin 1, IC 8A).
b. voltage stored on C33
c. voltage stored on C34
d. ATC correcting bias voltage (junction of R77 and R78).
e. ATC corrected output (pin 7, IC 8B).



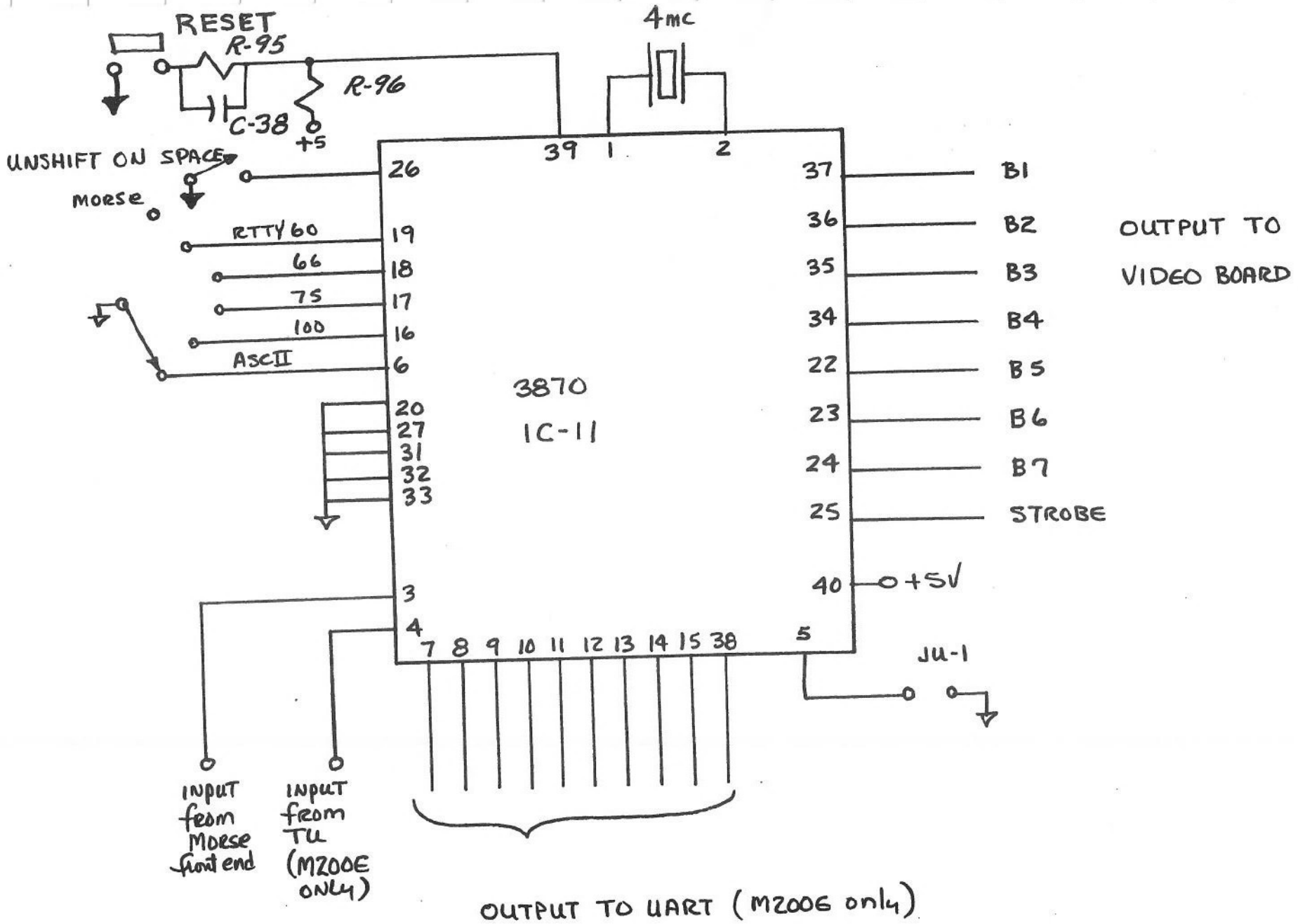
Morse Front End M100E-M200E



T.U. Limiter/Active filters (M200E only)

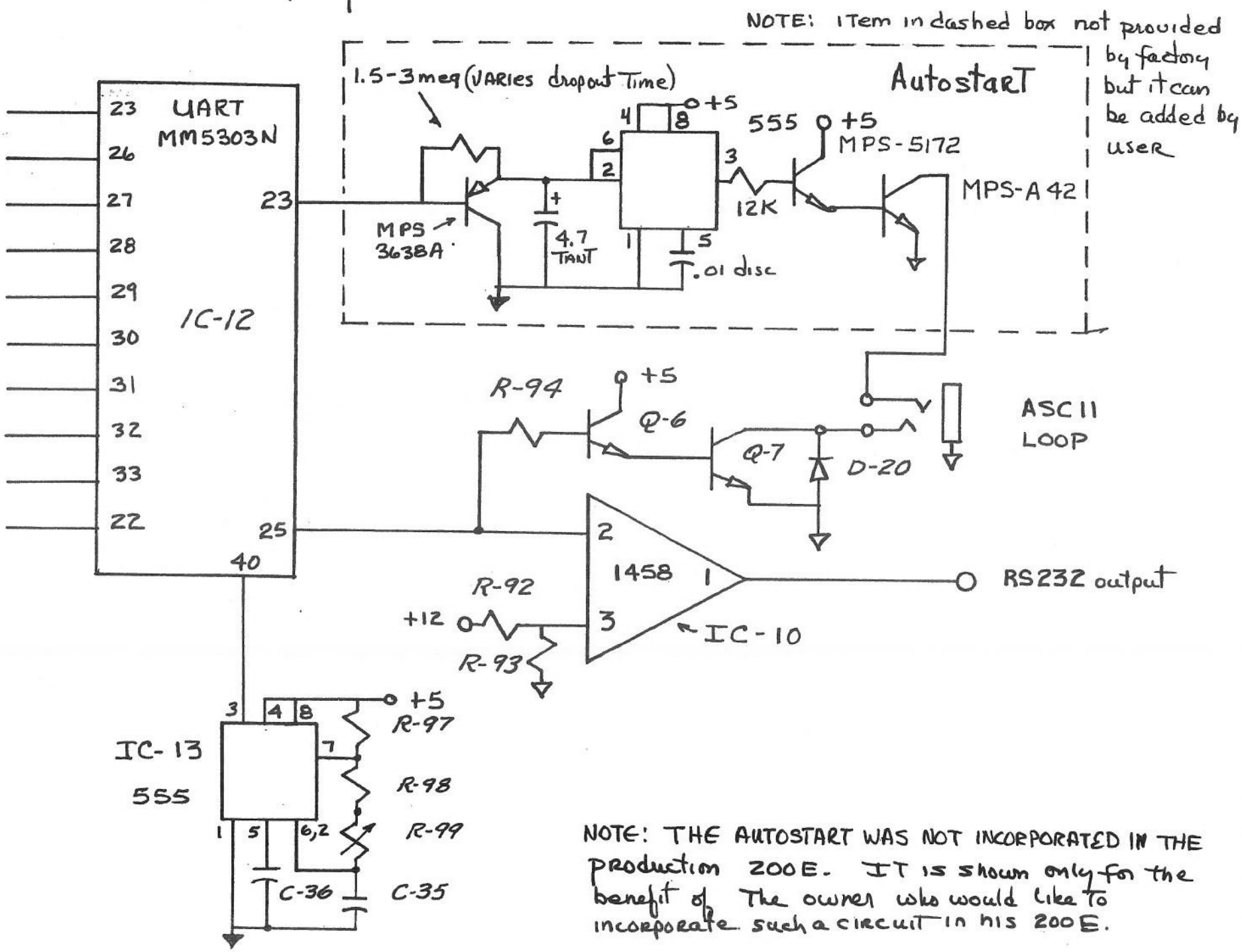


M200E SLICER, ATC, & METER (M200E ONLY)



M100E-M200E CPU

M200E ASCII Output & Autostart Section



NOTE: THE AUTOSTART WAS NOT INCORPORATED IN THE production 200E. IT is shown only for the benefit of the owner who would like to incorporate such a circuit in his 200E.

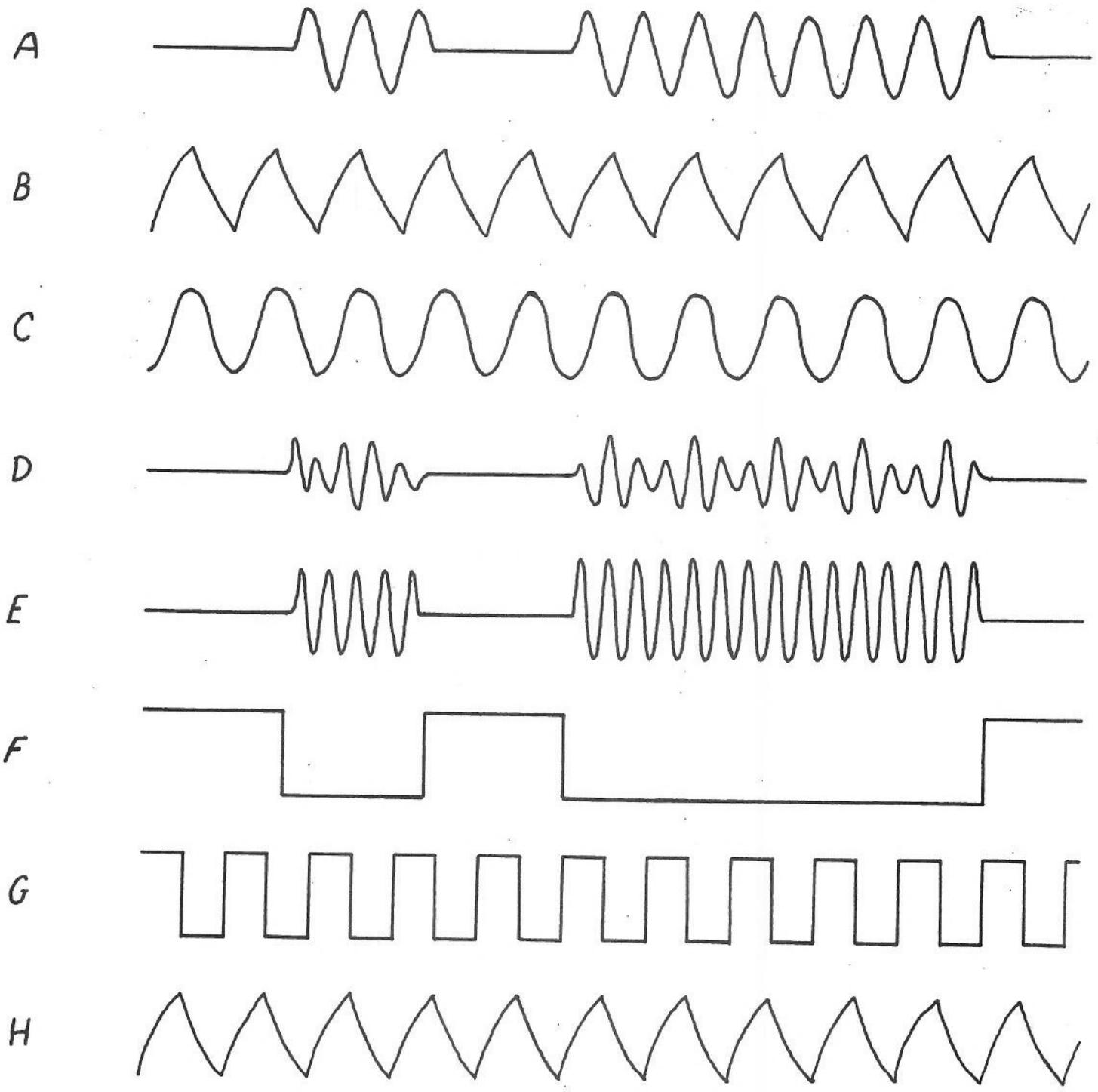


FIG 6

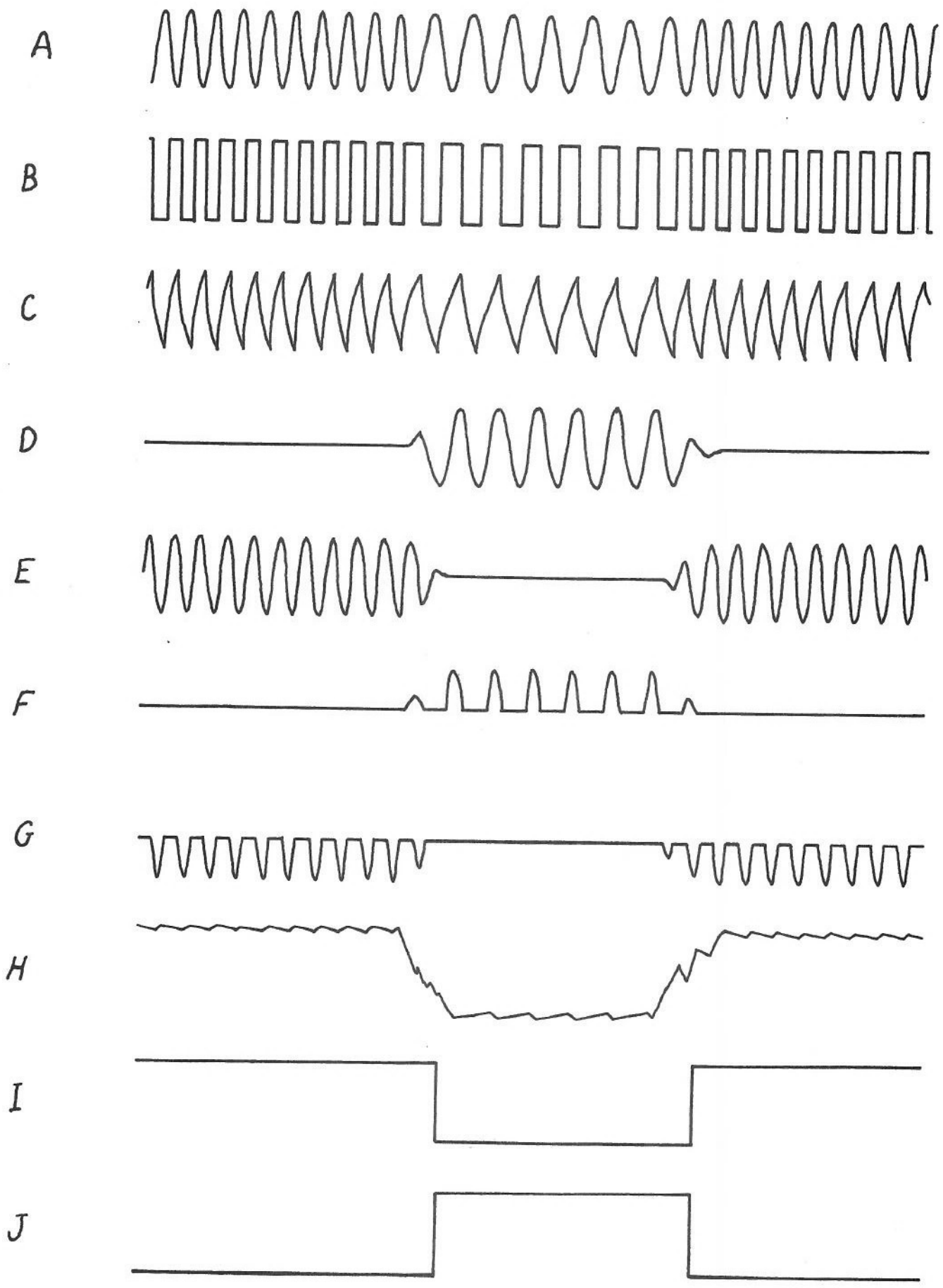


FIG. 7

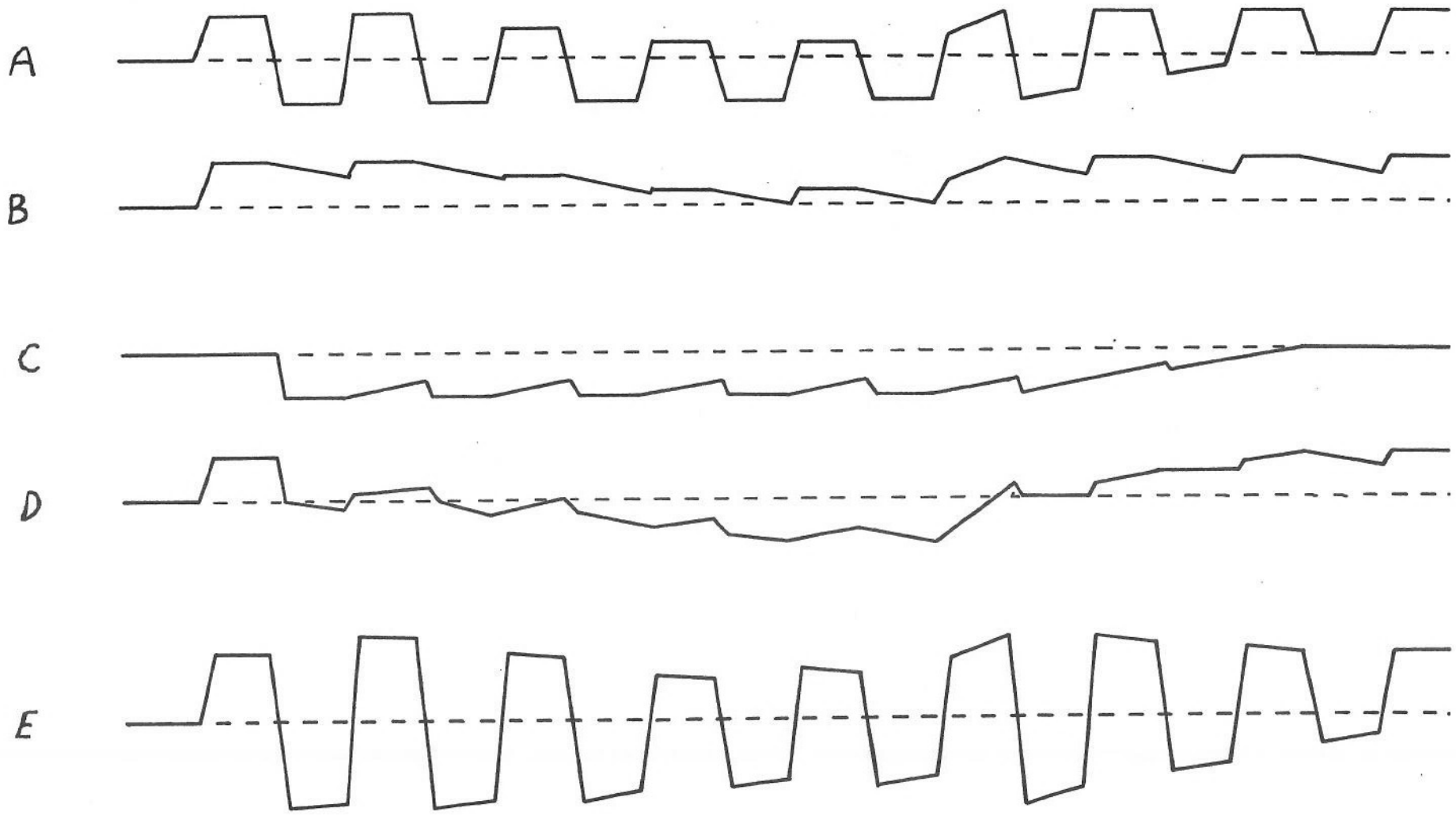


FIG 8