CWR-685E

SERVICE MANUAL

Digitization and editing of text and images by DC7XJ, August 2019

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CWR-685E Operating Instructions

1. **Introduction** (Concept and cautions of troubleshooting)

1) When repairing a trouble in a computer system, it is essential, in the first place, to distinguish whether the trouble is due to software or hardware. When it is found to be a hardware trouble, it is then required to judge whether it is due to inside of the interface device – such as, in this system, PCI (IC28), PIA (IC32), CRTC (IC18), output latch (IC27), signal input ports (IC45, IC46, IC40) – or due to outside of the interface device.

2) Actions of PCI, PIA, CRTC require setting by the software, and they do not operate unless setting is made normally. In a trouble of computer block, display is not made since CRTC does not operate, data reading from keyboard and data output to printer are not done because PIA does not operate, and even control of transmission and reception by SEND-AUTO-RECEIVE switch is impossible because PCI, output latch, and signal input ports do not operate normally.

3) One of possible troubles in the computer block is a defect of the ROMs (IC29, IC30) in which software is written. Therefore, when the Computer does not seem to operate normally, replace the IC29 and IC30 in the first place. (The both ICs are mounted by way of socket. Always replace the two ICs at the same time. If specified tool cannot be used when dismounting, remove with particular care not to bend the lead pins of ICs.)

4) In the description, "H level at TTL level" or merely "H level" refers to DC + 2.4 V to +5 V; "L level at TTL level" or merely "L level" means DC +0.8 V to 0 V.

5) It must be noted, that normal output signal may not be delivered from the IC also due to trouble at the load side.

6) Since the waveform at check point of frequency is often other than 50 % in duty ratio (such as TP-3 on main PCB), it is better to use an oscilloscope of triggered sweep system, rather than frequency counter (However, oscilloscope of synchronized sweep or free-running sweep system is not proper.)

7) In this system, many connectors are used in the connections of the PCBs, switches and other modules in order to facilitate assembly, maintenance, checking and replacement. Accordingly, troubles in these connectors are also probable, such as faulty contact and defective connection between contact pin and vinyl coated wire within connector plug housing (in the case of solderless connection).

   Besides, probable causes of computer troubles may also include faulty contacts of the socket in software ROM (IC29, IC30), and take this point also into consideration when repairing.

8) The IC numbers, part numbers, and connector numbers refer to the numbers on the main PCB (PCB No. 810529-1) unless otherwise noted.

2. General description

2.1 Composition

The block diagram of this System is shown in attached drawing. The program ROM contains a total of 6 k bytes, consisting of 2732 × 1 and 2716 × 1; the RAM has 128 bytes built in the MPU and 2 k bytes of 2114 × 4; the video RAM operates on 2114.

The MPU (micro processing unit) is equivalent to Motorola MC6802 (the machine code is same as MC6800), and clocks at 3.3792 MHz divided to 1/4 from 13.5168 MHz are fed from the EXTAL terminal. Since the clocks are further divided to 1/4 in the MPU, the system finally operates on clocks at 844.8 kHz. This clock at 844.8 kHz is delivered as E signal from pin 37 of MPU, and is given to a peripheral device of this system as a synchronizing signal.

Equally important as E signal are VMA and R/W.

The VMA becomes TTL level H only when address data delivered from the MPU is valid; the R/W becomes TTL level H when the MPU receives data from peripheral device and turns to TTL level L when data is given from the MPU to peripheral device.

These data exchanges are synchronized with the change of E signal from TTL level H to TTL level L when the VMA is at TTL level H.

Since the MC6802 is an eight-bit MPU (CPU), it can exchange data with peripheral device by way of input/output terminals D0 to D7 of 8-bit bidirectional data.

For selection of address, there is an address data output terminal of 16 bits, but since the A15 of higher position is not used in this system, the total address space is 32 kbytes.

For conversion from parallel to serial of sending data of RTTY and conversion from serial to parallel of received data, a USART (universal synchronous/asynchronous receiver/transmitter) equivalent to Intel 8251A is used, so that the transmission and reception may be operated simultaneously.

For data reading from the keyboard and data output to the printer, a PIA (peripheral interface adapter) equivalent to Motorola MC6821 is used, and the data input and output are effected in the parallel system of ASCII codes.

The screen display is controlled by the Hitachi HD46505S CRTC (CRT Controller) equivalent to Motorola MC6845S. The CRTC can set the display format freely according to the command from the CPU. In this system, a format of 32 characters/line by 20 lines is determined.

Since the CRTC, PIA, and USART do not operate unless the action is set immediately after the power source is turned on or reset, the prescribed data is written in the first place in this System.

In the event of trouble in the MPU block, since this setting is not effected, nothing appears on the display screen if the main power switch is turned on.

The method to judge whether the trouble is due to the MPU block or due to one of the devices or input/output units connected to the device is mentioned later.

2.2 Flow of signal

A block diagram is shown in attached sheet. Referring to the block diagram, the flow of signal is explained below.
An audio signal fed from the AF IN (RX or TAPE) terminal of the rear panel when receiving is selected by the RX/TAPE input selector on the front panel, and is delivered to AF OUT terminal in the rear panel, and is, at the same time, fed into AF input (J3-1) on MODEM PCB and AF input (J9-1) on main PCB. Therefore, the AF OUT can be also used as AF input terminal (at this time, however, the AF IN RX and AF IN TAPE must be used as output terminals).

The CW audio signal fed into the main PCB is given to the J9-3 for driving the AGC amplifier for CW and input monitor Speaker, and, after being controlled in the volume by the input slide VR connected between J9-3 and J9-5, drives the Speaker for input sound monitor connected between J9-13 and J9-14 or the EXT SP output terminal.

The CW audio signal given to the AGC amplifier (IC42) passes through the active band pass filter (IC42) at center frequency of 800 Hz, and is converted into a digital signal by the PLL System decoder (IC44) for CW to control the gate of monitor oscillation sound at 800 Hz for CW, and is simultaneously read from the CW signal input port (pin 2 of IC45) in the Computer block, thereby flickering the LED for CW monitor at the same time.

When the CW/RTTY selector on the front panel is set at RTTY side, the CW/RTTY selection signal input (J7-11) on the main PCB is at L level, and is read from the input port (pin 12 of IC40) in the Computer block, and the gate (pin 1 of IC12) becomes L level at the same time. As a result, the output of PLL decoder becomes invalid.

When a key on the keyboard which is connected to the telegraph terminal on the rear panel is pressed, the key operation signal is given to a key signal input (J3-2), and is read from the key signal input port (pin 4 of IC45) to light up the LED for CW monitor, thereby opening the output gate of CW monitor OSC. At the same time, transistor switches TR5, TR8 for keying-out (SW OUT CW) are turned on.

At this time, the computer, in order to turn on the transistor switch TR9 for transmission and reception control of the transmitter, sets the output port (pin 6 of IC27) to TTL level H, and sets the reset delay timer, so that the signal may be set to the initial value again whenever key operations are subsequently made. When the timer expires, the TR9 is cut off. Meanwhile, this timer is not described in the circuit diagram because it is a software timer by the computer.

The CW signal read from the CW signal input port is decoded, and is delivered to the display screen and printer.

The RTTY audio signal fed from J3-1 on MODEM PCB is converted into a digital signal (for details of conversion see the description of performance of MODEM block), and is delivered from J4-7, and is supplied to the INT side of the FSK DEMOD INT/EXT slide switch in the rear panel. At the EXT side, a signal from the FSK TTL IN side is supplied. The digital signal selected by this slide switch is fed again into the J4-8 of MODEM PCB.

The logic circuit composed of IC10, IC12 on the MODEM PCB selects either received demodulated signal (TU/EXT) or sending signal (FSK) depending on the control signal STB or RX/TAPE given from the main PCB, and delivers the selected signal to the FSK OUT (J6-3). The signal delivered from the FSK OUT (J6-3) is fed into the FSK IN (J10-2) in the main PCB, and is given to RXD (pin 3) of RTTY received signal input port (IC28, USART), and is converted from serial to parallel in the IC28 being synchronized with the baud rate of 1/16 of the clock applied to RXC (pin 25) of IC28. The parallel data thus converted is decoded, and is delivered to the display screen and printer.

2.3 Control of SW OUT REMOTE

The SW OUT REMOTE terminal of the rear panel is connected to the REMOTE (J3-4) terminal of main PCB.

This terminal is directly shorted by the contact of the SEND-AUTO-RECEIVE switch when this switch is set to SEND side. When AUTO or RECEIVE position is selected, this terminal is controlled by the TR9 on the main PCB.

This terminal and the SEND-AUTO-RECEIVE switch is so wired that the J8-5 on the main PCB may be connected to GND when the switch is set to SEND position, and that the J8-8 is similarly connected to GND when it is set to RECEIVE side. Thus, this terminal always monitors the state of this switch, and controls the transmission and reception and TR9.

2.4 Flow of signal in transmission

When a key is depressed, an ASCII code of 8-bit parallel positive logic is delivered from the keyboard, and is given from pin 4 to pin 11 of J6 on the main PCB. In succession, a data strobe signal of negative logic is applied to pin 13 of J6, and is converted to a pulse signal by the one-shot multivibrator in IC6 to be fed in pin 40 of IC32.

At this time, according to the initially set format, the IC32 set the IRQB (pin 37) to L level in order to ask the MPU to read data. In consequence, the MPU, immediately or after finishing the process being run at that time, reads the data from the keyboard being applied to PA0 to PA7 in IC32, and returns the IRQB to H level at the same time, and delivers a data reading acknowledgement signal to the CA2 (pin 39) as negative logic pulse signal of 1.183 μs. The ACK signal is not used when feeding from the keyboard, but is used when controlling the system by means of other microcomputer or the like instead of the keyboard. In such a case, the parallel data should not be converted until the response of ACK signal is confirmed.

When the MPU reads the data, a process suited to the state, such as command processing, writing into transmission buffer area, writing into memory area, is effected according to the data.

REFERENCE

- In transmission of CW, the data in the transmission buffer is converted to CW code, and the output of CW output port (pin 2 of IC27) is controlled being synchronized with the clock signal created in IC35 and read in from pin 2 of IC40. This clock frequency may be varied by means of SPEED slide VR in the front panel.

  When the CW output port becomes H level at TTL level, the TR5 and TR8 are turned on, so that a key operation signal can be obtained from the SW OUT CW output terminal in the rear panel connected to J3-6. In CW ID mode at the time of RTTY, the TR10 is turned off by the signal of CW ID output port (pin 9 of IC27) which is operating simultaneously with CW output port, and the signal is shifted to a blank space.

- In transmission of RTTY, when the MPU writes data into USART, they are converted to serial signals in synchronism with the baud rate at 1/16 of the clock given to pin 9 of USART (IC28), and are delivered from TXD (pin 19) of USART, thereby controlling the TTL-OUT (J10-3 terminal) and TR10 as in the case of CW ID. The TTL-OUT (J10-3 terminal) of main PCB is connected to the FSK (J6-2 terminal) on MODEM PCB, and is delivered at TTL level to the FSK TTL OUT terminal in the rear panel from the FSK TTL (J4-9 terminal). The FSK signal is, at the same time, applied also to pin 5 of IC4 as AFSK shift signal. The AFSK signal created here is delivered from J4-3 terminal on MODEM PCS, and is sent to the AFSK

GAIN VR in the rear panel, and is synthesized with the signal of CW monitor OSC at 800 Hz which is delivered from J3-7 on main PCB (in actual operation, either one signal only is given here). After level adjustment at AFSK GAIN VR, the signal is fed again to J4-1 terminal on MODEM PCB, and reappears at J4-4 terminal as AFSK signal having shaped waveform, and is delivered from the AFSK OUT terminal in the rear panel.

The AFSK monitor speaker drive output which is delivered from J3-8 terminal on MODEM PCB is once fed to J10-10 on the main PCB, and is synthesized with the CW monitor speaker drive output, and then delivered to J9-6 terminal. This output signal is applied to the VOLUME slide VR in the front panel to be controlled in the sound volume, and drives the built-in output monitor speaker or PHONE output terminal in the rear panel.

3. Input/output actions

3.1 Actions of switches

RESET PB

Only while it is being depressed, the J7-2 terminal on main PCB is connected to GND.

FILTER

In OFF position, the J7-3 terminal on main PCB is connected to GND.
In ON position, the J7-4 terminal on main PCB is connected to GND.

SPACE NARROW

In NARROW position, the J7-5 terminal on main PCB is connected to GND.

CWIDA/CWIDB

In CWID A position, the J706 terminal on main PCB is connected to GND; in CWID B, the circuit is open.

PAGE PB

While it is being depressed, the J7-8 terminal on main PCB is connected to GND; when it is not pushed, the J7-7 terminal on main PCB is connected to GND.

MODE A/MODE B

In MODE B, the J7-9 terminal on main PCB is connected to GND.

CW/RTTY

In RTTY position, the J7-11 terminal on main PCB is connected to GND; in CW position, the J1-7 terminal on MODEM PCB is connected to GND.

ASCII/BAUDOT

In ASCII position, the J7-12 on main PCB is connected to GND.

LTR PB

Only while it is being pressed down, the J7-14 on main PCB is connected to GND.

FIG PB

Only while it is being pressed down, the J7-13 on main PCB is connected to GND.

LOCK U.O.S.

When turned on, the J7-15 terminal on main PCB is connected to GND.

NOR/REV

In REV position, J1-2 terminal on MODEM PCB is connected to GND.

BAUD 6-position switch

One of the terminals J2-2 to J2-7 on MODEM PCB is connected to GND.

SHIFT 3-position switch

When 425 is turned on, the J1-12 terminal on MODEM PCB is connected to GND.
When 850 is turned on, the J1-11 terminal on MODEM PCB is connected to GND.

TONE LOW

When turned on, the J1-10 terminal on MODEM PCB is connected to GND.

RX/TAPE

In RX position, the AF IN RX terminal and AF OUT terminal in rear panel and J9-1 terminal on main PCB are connected together.
In TAPE position, the AF IN TAPE terminal and AF OUT terminal in rear panel and J9-1 terminal on main PCB are connected together, and the J7-16 terminal on main PCB is connected to GND.

SEND/AUTO/RECEIVE

In SEND position, the SW OUT PHONE terminal in rear panel is connected to GND, and the J8-5 terminal on main PCB is connected also to GND.
In RECEIVE position, the J8-8 terminal on main PCB is connected to GND.

3.2 Actions of external control signal output ports

This paragraph describes the performance of output ports on the main PCB in which outputs vary depending on the setting of each switch or commands. These outputs are controlled by the computer.

J10-5

When RX/TAPE selector is set to RX side, the level becomes H. When the RESET button is being pushed down, the level is L.
That is, when the RESET button is pressed, the level is L, and when the button is released, the level temporarily becomes H, but soon returns to L.
This output controls the J1-1 terminal on MODEM PCB.

Output port

The IC27 is an 8-bit latch IC. The external control signals of this system are mainly delivered from this IC. While the RESET button is kept depressed, this output remains at L level.

Pin 15

An output is delivered to J10-4 terminal. The output becomes H level when sending RTTY. This output controls the J6-1 terminal on MODEM PCB, and opens the AFSK output gate of RTTY when the level is H to delivery an AFSK oscillation signal.

Pin 16

A transmission/reception changeover signal for software control is delivered. When the level is H, the SW OUT REMOTE is turned on, and the reading gate of CW audio demodulated signal is also closed.

Pin 5

During transmission of CWID, the level becomes H in synchronism with CW code. When the level is H, the SW OUT FSK is turned on, and the FSK TTL OUT is set to L level. In CW mode, this pin operates in synchronism with pin 2.

Pin 2

When sending CW, the level becomes H in synchronism with CW code. When the level becomes H, the SW OUT CW is turned on, and the CW LED is lit.

Pin 9

When the level becomes H, the gate of CW monitor OSC is opened, and an 800 Hz monitor sound is delivered to the AFSK OUT and internal monitor Speaker.

Pin 19

When the level is H, the Output of SW OUT FSK is maintained in the mark. However, since this Output port is not used in the present Software, the level always remains at L.

Pin 16

This is designed as an output for changing over the rate of frequency division of IC4. This function, however, is not used in the present Software. Internally, this pin is used as key operation mode memory of telegraph key of CW, the level becomes H when the telegraph key is pushed down.

Pin 12

Though it is designed as a means of control of display screen changeover by Software, this function is not used in the present Software. Therefore, the level is always L.

3.3 Actions of CW audio demodulator

The IC42 is a Norton amplifier having four logic circuits of identical function contained in one package. In this system, two of the four logic circuits are used to compose an AGC amplifier for CW and band pass filter. The other two logic circuits are not used.

The circuit of the AGC amplifier block is identical with that of AGC amplifier for RTTY on the MODEM PCB, whereas the circuit for CW uses 10 µF C14 in order to increase the time constant.

This AGC amplifier is actually responsible for both AGC action and limiter action.

The output of the AGC amplifier is fed to the band pass filter on the next stage by way of coupling capacitor C37.

The resistor R28 is for adjusting the input level to the band pass filter. The waveform at test point TP-5 of the band pass filter output attains the maximum amplitude when the output amplitude from the AGC amplifier becomes 90 % of the maximum value as an 800 Hz signal is fed from the AF IN, and the peak of the waveform is slightly deformed at 100 % input, in normal state. This resistor is varied in the range of 220 to 330 kohms in each manufacturing lot.

If the resistance is too small, a misdecoding may be caused by noise signal where there is no signal.

The variable resistor VR5 is for setting the center frequency of band pass filter. It is adjusted to 800 Hz at the time of manufacture.

The audio signal obtained from the band pass filter passes through the coupling capacitor C38, and is lowered in level by the 1/11 attenuator composed of R15 and R14, then is applied to input pin of PLL decoder IC through C20.

The dividing ratio of R15 and R14 is so set that the PLL decoder IC (IC44) may be locked when the amplitude of TP-5 exceeds 70 % of the maximum value.

The free-running frequency of PLL is set by the resistor and capacitor connected between pin 14 of IC44 and GND. This free-running frequency may be measured by detecting the output of TP-2 with frequency counter.

The capacitor determines the lock range of PLL, and the larger the capacity, the narrower becomes the lock range.

Suppose the free-running frequency of PLL is 800 Hz, when the resistance is 56 kohms or higher, the oscillation stops. Accordingly, the lock range is the maximum when the capacitor is 0.0033 μF and resistor is 56 kohms.

When the capacitor is 0.0068 μF, the lock range is narrow. In such a case, the free-running frequency must be precisely adjusted to 800 Hz by means of semivariable resistor VR2.

When the PLL is locked, pin 6 of IC44 becomes L level.

3.4 Change of CW transmission speed

The transmission speed of CW is determined by the output frequency of clock generator composed of IC35, TR1, TR2.

The SPEED slide VR on the front panel is connected to the J9-8 to J9-10 terminals on main PCB. When the voltage at J9-9 terminal is high (close to J9-10), the oscillation frequency is low, and when the voltage at J9-9 terminal is low (close to J9-8) , the oscillation frequency is high.

The VR-3 is for adjusting the slow speed, and the VR-4 is for controlling the fast speed. At the time of manufacture, the variable range of the speed VR is set within 25 characters/minute to 200 characters/minute (400 Hz to 3200 Hz).

CW monitor sound oscillator

The circuit composed of 3/6 IC21, R45, R46, VR1 and C25 is an 800 Hz monitor sound oscillator of CW. The frequency is precisely adjusted to 800 Hz by the VR1. The oscillation output is buffered by the 1/6 IC21 and 2/6 IC43, and is used to drive the driver (2.6 IC34). When pin 15 of IC34 becomes L level, the oscillation sound is delivered.

Video output

The video signal to the built-in CRT is controlled in the output level (contrast) by the VR6 in the main PCB, and is delivered to the CRT unit from the J4-1 terminal.

The horizontal sync and vertical sync signals are delivered separately from the J4-2 and J4-3 toward the CRT unit.

As video signal for external display, composite sync and video signals are respectively shifted in level by D3 and D4, D5, and applied to the base of TR3, and delivered to the J4-5 as composite vi-

deo signal, which is picked up from the VIDEO OUT terminal in the rear panel. The resistor R8 is inserted so that the output may be 1.0 ±0.2 V when a load of 75 ohms is applied to the VIDEO OUT terminal.

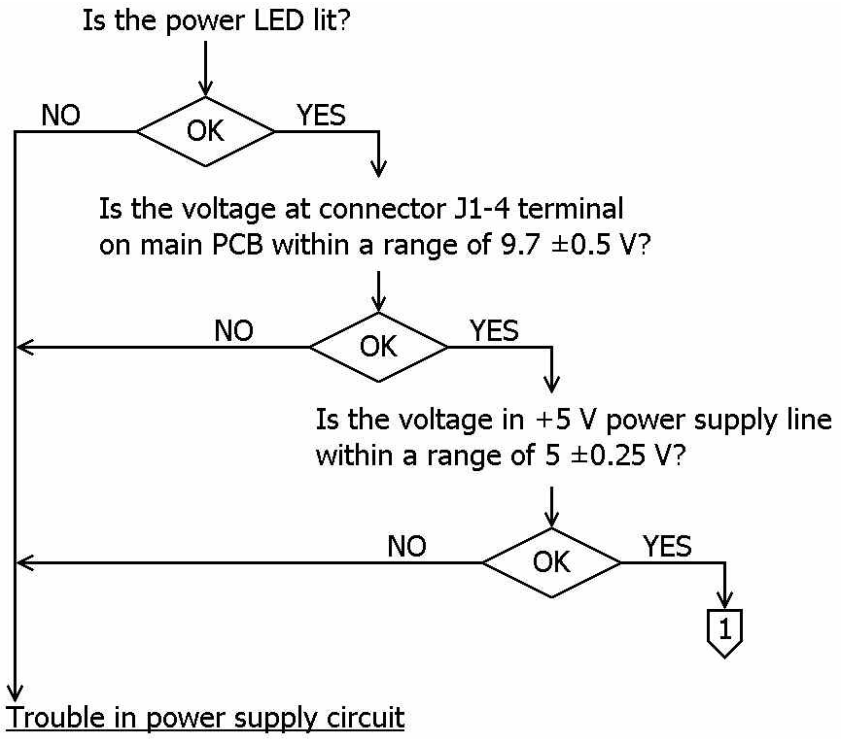
4. Troubleshooting (Troubleshooting flow charts)

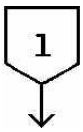
4.1 Trouble of built-in display

(A) No display

The built-in display of this System appears in about ten seconds after the power switch is turned on. If no display appears in more than 15 seconds, check if the brightness control on the back panel is turned to the dark side – in such a case return to the "light" side (turning clockwise).

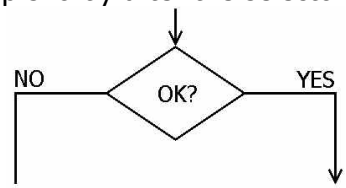
If no display still appears, check as follows:





Set the VOLUME slide VR lever to the highest position. Set the CW/RTTY selector to RTTY side.

After thus setting, is the AFSK monitor sound oscillated when SEND-AUTO-RECEIVE selector is set to SEND and does the oscillation stop shortly after the selector is returned to RECEIVE position?

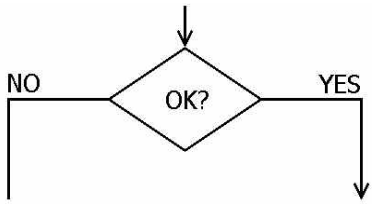


Probable causes are trouble of crystal oscillator or dividing circuit, failure of Computer or wrong setting of CRTC. In the first place, check the crystal oscillator and dividing circuit.

Trouble in CRTC block

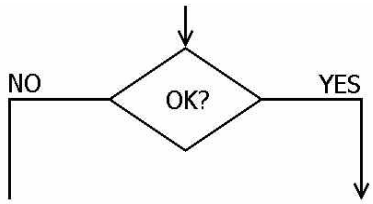
Check the frequency of the following parts in the numerical order (checking of crystal oscillator, dividing circuit):

1. Pin 6 of IC5 (13.5168 MHz)
2. Pin 9 of IC3 (6.7584 MHz)
3. Pin 5 of IC3 (3.3792 MHz)
4. Pin 39 of IC31 (3.3792 MHz)



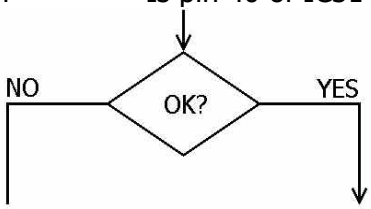
Output has ceased to come out normally; trouble of initially checked part.

Is the output of pin 37 of IC31 844.8 kHz?



IC31 is broken

Is pin 40 of IC31 at H level?



R76 is broken; C32 is shorted; trouble of RESET switch or switch wiring; breakage of IC27, IC18, IC2, IC32, IC31

Computer is not working normally

(B) Fluctuating display

The power source requirements of this System are voltage of DC 12 to 14.5 V and current of not less than 1.65 A.

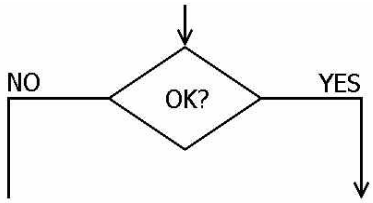
Power source conditions

1. Stabilized power source is not necessarily required. The System can operate on a power source containing slight ripples.
   However, the voltage should not be lower than 12 V at the bottom of ripple. Below 12 V, the performance of built-in display becomes unstable.

2. In the case of power source containing ripples, the average voltage should not be more than 14.5 V.

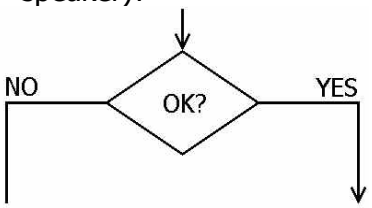
If the display screen still fluctuates though conforming to the requirements above, check as follows:

Is the voltage at connector terminal J1-4 on main PBC within a range of 9.7 ±0.5 V?



ZD1 or IC48 is broken

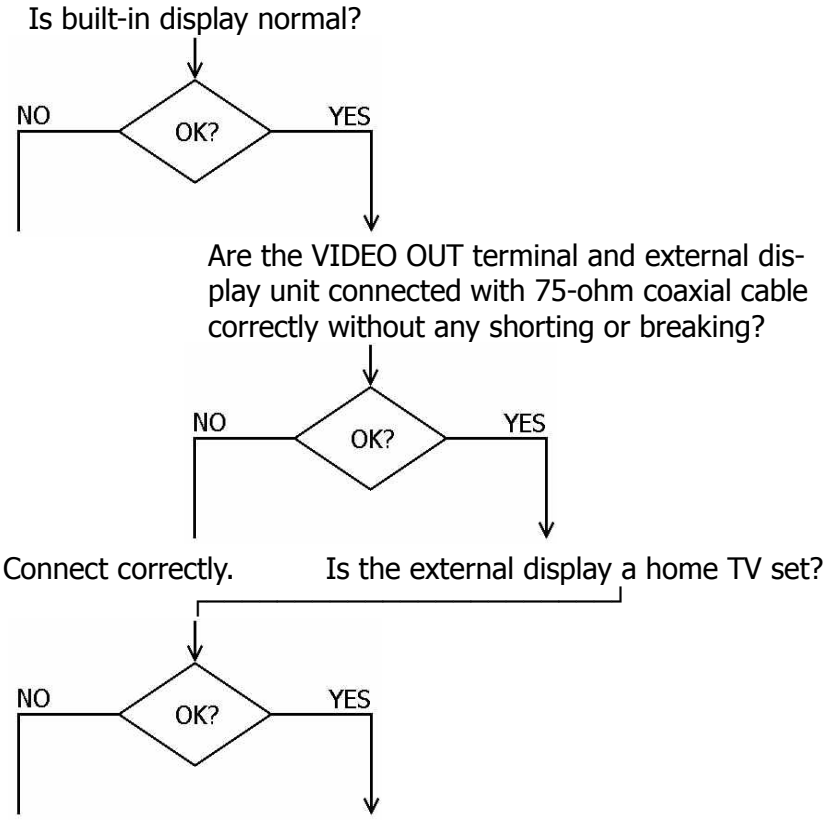
Is there any object emitting lines of magnetic force nearby (such as power transformer and speaker)?



Wrong adjustment of V-HOLD or video center of CRT unit, or CRT unit is defective.

Remove the object.

(C) Abnormal external display



The VIDEO OUT terminal of this system delivers a composite video signal of 1.0 ±0.2 Vpp at 75 ohm load. The sync signal level is 30 % and video signal level 70 %.

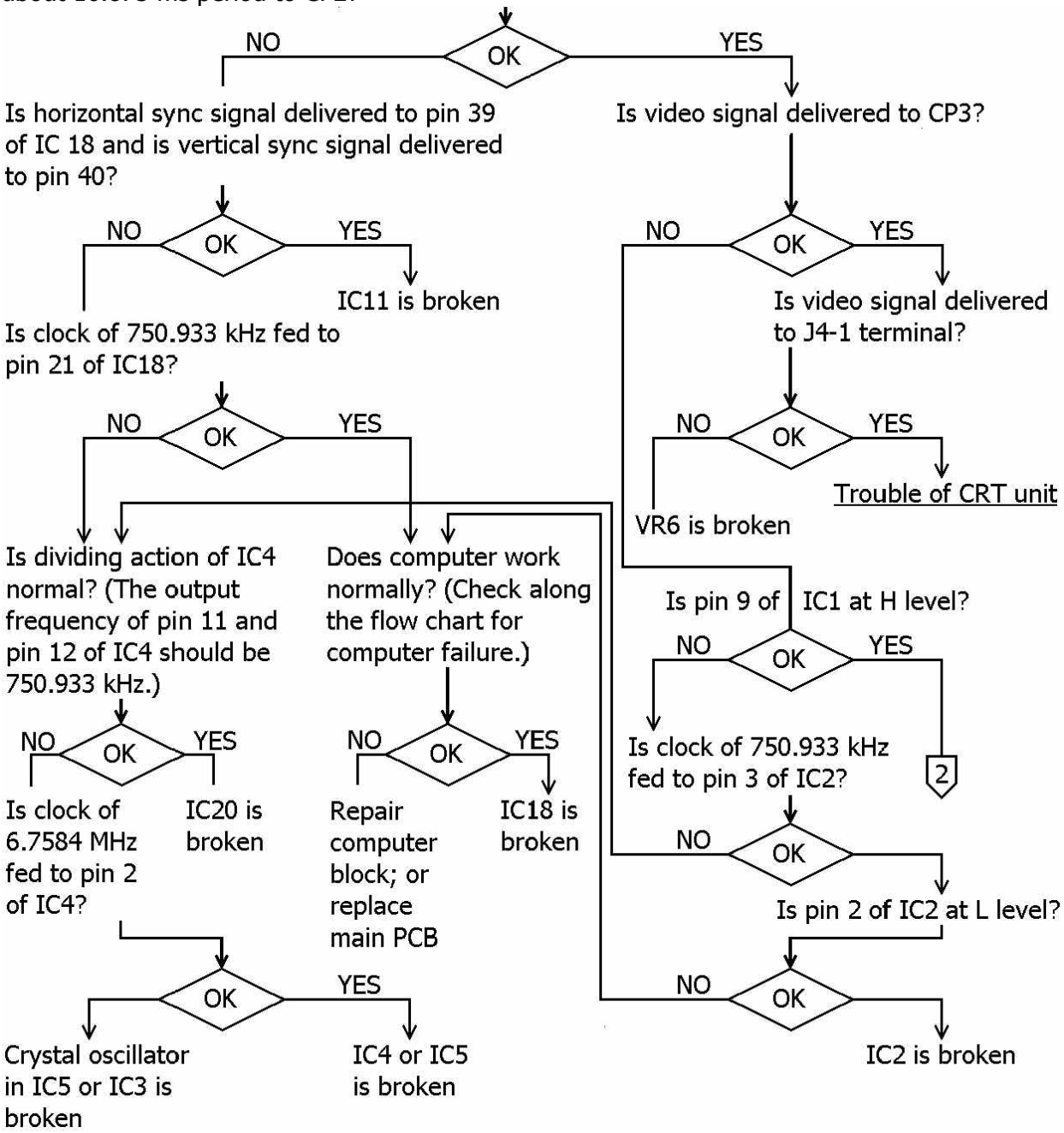
H-SYNC: 15.644 kHz; pulse width 5.32 µs
V-SYNC: 59.26 Hz; pulse width 2.1 ms
Non-interlaced raster scan system
Number of rasters: 264
Horizontal display time: 42.61 µs
Vertical display time: 14.06 ms

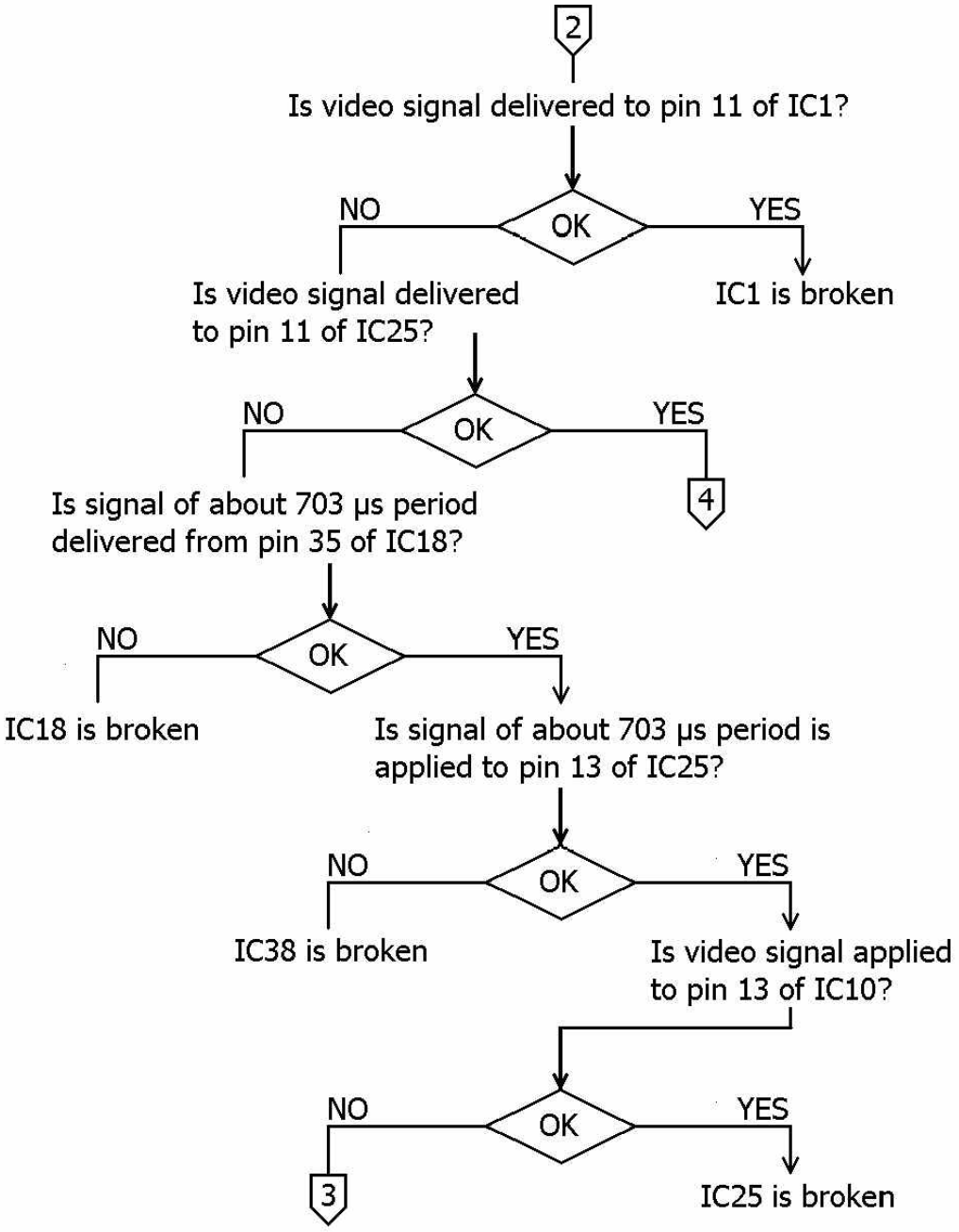
If the display unit does not conform to the conditions above, normal operation is not expected. Usually, however, the V-SYNC and H-HIGH may be adjusted at the monitor TV set side.

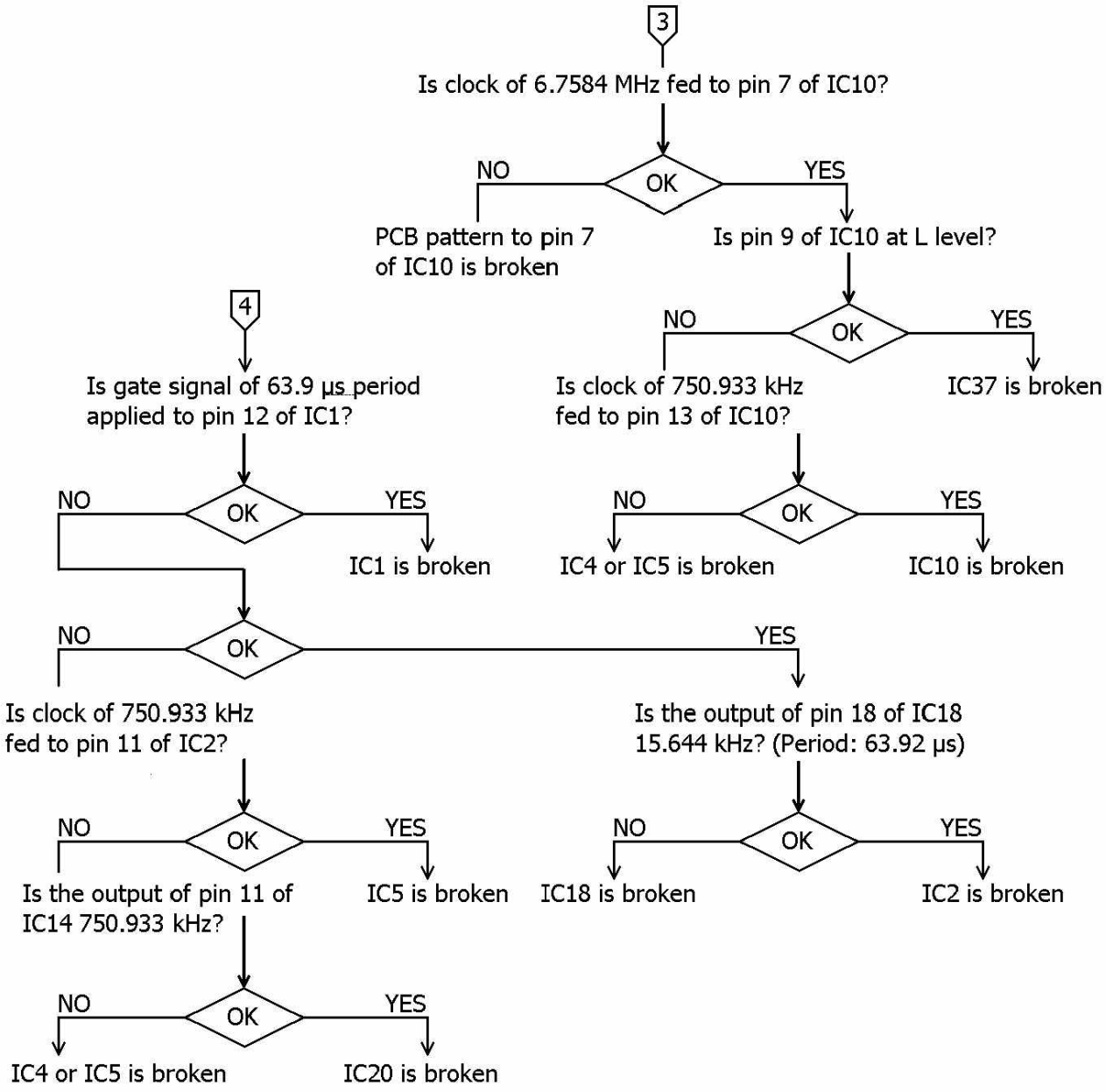
Home TV set cannot be connected to VIDEO OUT terminal. Use video monitor TV set.

4.2 Trouble of the CRTC block

Is horizontal sync signal of about 63.92 μs period delivered to CP1, and is vertical sync signal of about 16.875 ms period to CP2?




2
Is video signal delivered to pin 11 of IC1?
NO
OK
YES
Is video signal delivered to pin 11 of IC25?
IC1 is broken
NO
OK
YES
4
Is signal of about 703 µs period delivered from pin 35 of IC18?
NO
OK
YES
IC18 is broken
Is signal of about 703 µs period is applied to pin 13 of IC25?
NO
OK
YES
IC38 is broken
Is video signal applied to pin 13 of IC10?
NO
OK
YES
3
IC25 is broken


3
Is clock of 6.7584 MHz fed to pin 7 of IC10?
NO
OK
YES
PCB pattern to pin 7 of IC10 is broken
Is pin 9 of IC10 at L level?
NO
OK
YES
IC37 is broken
Is clock of 750.933 kHz fed to pin 13 of IC10?
NO
OK
YES
IC4 or IC5 is broken
IC10 is broken
4
Is gate signal of 63.9 µs period applied to pin 12 of IC1?
NO
OK
YES
IC1 is broken
NO
OK
YES
Is clock of 750.933 kHz fed to pin 11 of IC2?
Is the output of pin 18 of IC18 15.644 kHz? (Period: 63.92 µs)
NO
OK
YES
IC5 is broken
Is the output of pin 11 of IC14 750.933 kHz?
NO
OK
YES
IC18 is broken
IC2 is broken
NO
OK
YES
IC4 or IC5 is broken
IC20 is broken

4.3 Trouble of Computer block

Check whether the Computer block is operating normally or not in the following procedure.

o The output level of pins 2, 4, 5, 6, of IC37 should be always H level as far as the Computer is operating normally. When a pulse waveform of L level is observed on oscilloscope screen, it means that the Computer is running away. Runaway of Computer is almost always accompanied by abnormal oscillation of the monitor sound.

o As far as the system is operating normally, the Computer reads the state of switches, and varies the level of each Output port as follows.

a. When the RX/TAPE selector is set to RX side (since the switch is turned off, pin 4 of IC40 becomes H level), pin 24 of IC28 is set to L level.

b. With the RX/TAPE selector at RX position, when the RESET button is pressed, pin 24 of IC28 is set at H level while the button is being depressed, and it is immediately set to L level when the button is released.

c. When the RX/RAPE selector is set to TAPE side(since the switch is turned off, pin 4 of IC40 becomes L level), pin 24 or IC28 is set to H level.

d. With the RX/TAPE selector at TAPE position, while the RESET button is being pressed down, pin 24 of IC28 is set at H level, and immediately after the button is released, the level is set to L for about 20 ms, and is then set to H again.

e. With the CW/RTTY selector at RTTY, when the SEND-AUTO-RECEIVE selector is set at SEND (the switch is turned on, and pin 14 of IC40 becomes L level}, and pin 15 of IC27 is set to H level, and AFSK monitor sound is delivered. At the same time, pin 6 of IC27 is also set to H level. At this time, when an alphabetical or numerical key is pressed on the keyboard, a corresponding code is sent out immediately, and the frequency of AFSK monitor sound is also varied in tune with the code. In this state, when the selector is set to AUTO or RECEIVE position (the switch is turned off, and pin 14 of IC40 becomes H level), about one second later, both pin 6 and pin 15 of IC27 are set to L level, and the AFSK monitor sound ceases.

f. With the CW/RTTY selector set at CW and SEND-AUTO-RECEIVE selector at SEND position, when an alphabetical or numerical key is pressed on the keyboard, a corresponding code is sent out immediately, and the monitor sound at 800 Hz is intermittently delivered in tune with the code, and the CW LED flickers at the same time.

o Of the ICs on the main PCB, those having high frequency of trouble occurrences (breakages) are the following:

IC19 (SN74LS245)
IC7, ICS, IC9 (SN74LS157)
IC42 (MC3301, LM3900)
IC31 (MC6802, HD46802)
IC29 (2716 type E-PROM ... operation program written in)
IC30 (2732 type E-PROM ... operation program written in)
IC17 (2716 type E-PROM ... character pattern written in)
IC6 (TC4011)

4.4 Trouble in CW transmission

CW transmission is synchronized with CW sending clock.

The CW sending clock is made in IC35, and is fed from CW sending clock input port (pin 2 of IC40) into the Computer block.

When this clock stops oscillation, CW cannot be transmitted.

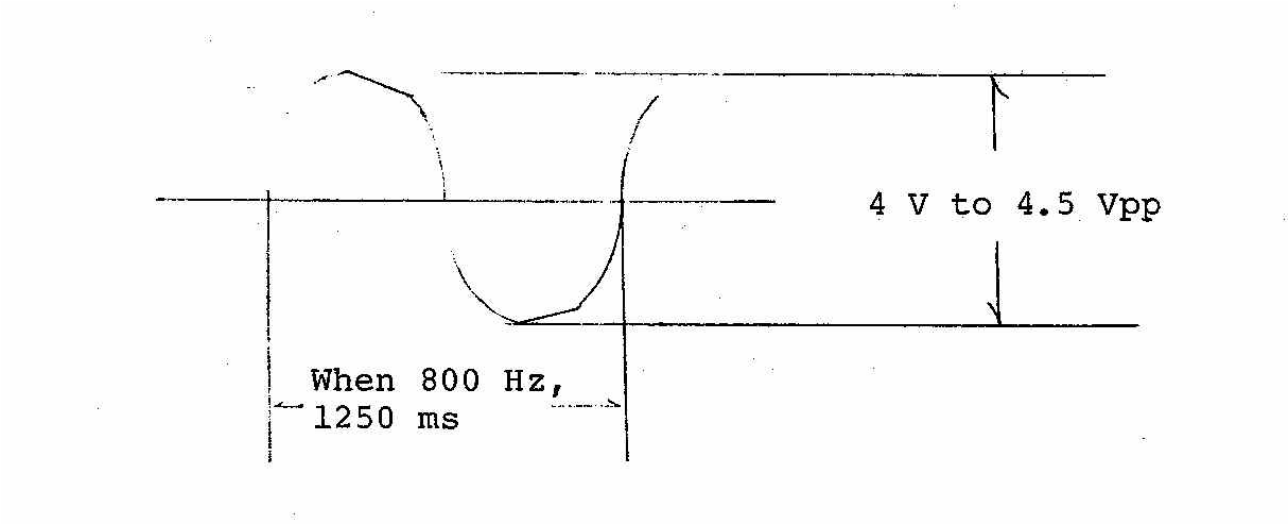
The oscillation waveform at TP-3 is fixed at L level within about 15 to 20 μs, while the duration of H level varies with the position of SPEED slide VR.

Since the monitor sound, CW LED flickering, transceiver transmission/reception selection, and CW key operation are controlled by the output of IC27, when the CW sending clock is normal and other functional part is in trouble, see the actions of external control signal output ports (par. 3.2).

4.5 Trouble in CW reception

When reception of CW is in trouble, check if signal appears at check points of TP-5, TP-2, TP-4.

While referring to the flow of signal (par. 2.2), check for abnormal action. The TP-5 waveform should be normally saturated (see below). About 10 % portion is cut as shown below.



If malfunction often occurs due to noise, vary the resistance of R28. When the resistance is increased, malfunction by noise decreases, whereas the sensitivity drops.

It is also possible to decrease malfunction by noise by adding 0.1 μF to C22 to make a total of 0.3 μF. In this case, however, high speed signals cannot be decoded. Similarly, resistance to noise is increased when C14 is changed to 22 μF, but the response speed of AGC is slowed down, so that the resistance to QSB is weakened.

4.6 Trouble of RTTY

The speed of RTTY transmission and reception is selected by the BAUD six-position switch. Turn on only one of the buttons. If two or more buttons are turned on or all buttons are turned off, the system does not operate normally. When transmitting, do not change over this switch, but change over the baud rate after returning to reception.

When the three-position switch for shift changeover is in OFF position in all buttons, 170 Hz shift is selected.

When the HIGH, LOW switches are both in OFF position, a high tone is selected.

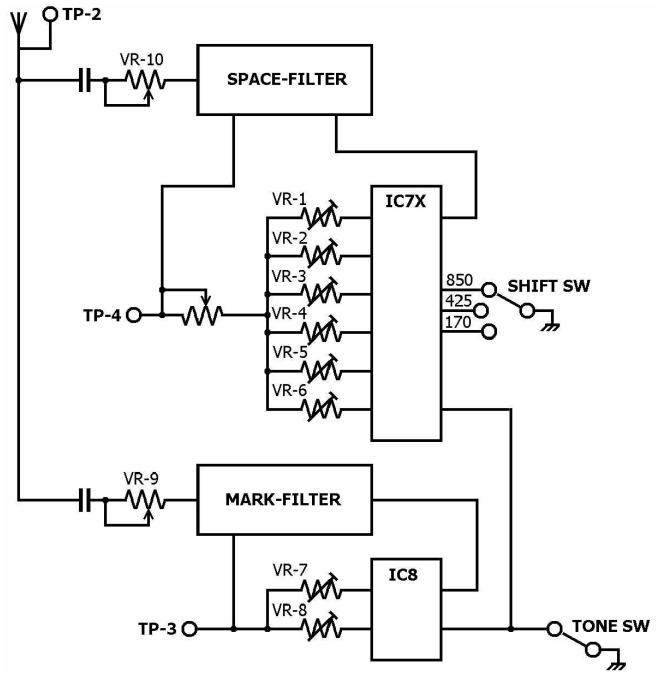
5. Description of MODEM printed circuit board performance

5.1 Demodulator

Signals at 30 mV to 2 Vpp fed from the AF IN terminal are evened out to about 3 Vpp by 1/4 IC3 and TR3. The Outputs can be checked at TP-1.

The evened signals are fed to 2/4 IC2 and passed through band pass filter of 800 Hz to 3,200 Hz, and unnecessary Signal portions are taken out. Then the filtered signals are passed through a limiter 1/4 IC3, and converted to signals stable in vertical direction. The signals can be checked on TP-2.

Then necessary frequency should be selected by the programmable mark and space filters.



		Remarks
VR-1	2295 Hz adj.	High 170 shift
VR-2	2550 Hz adj.	High 425 shift
VR-3	2975 Hz adj.	High 850 shift
VR-4	1445 Hz adj.	Low 170 shift
VR-5	2125 Hz adj.	Low 425 shift
VR-6	1700 Hz adj.	Low 850 shift
VR-7	2125 Hz adj.	High tone mark
VR-8	1275 Hz adj.	Low tone mark

VR 9, VR-10: They are for adjustment output level, but are turned fully to max. input at the time of shipping.

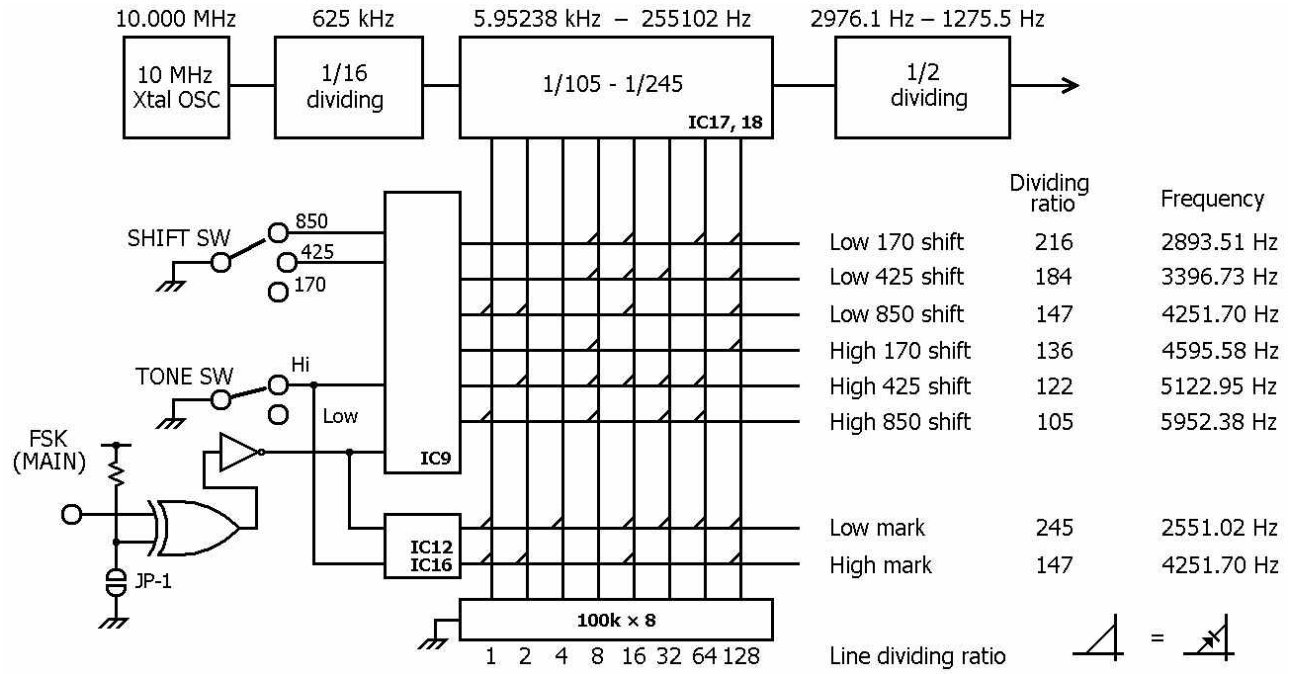
* To obtain state with constant shift alone, adjust so that TP-3 and TP-4 findings may be identical.

The selected frequency can be checked on TP-3 and TP-4. Part of this output is amplified by the LED amplifier, and is used to light up the LEDs of mark and space. Also signals for X, Y oscilloscope of the monitor are taken out from this output.

The space and mark outputs become demodulation outputs by way of slicer, low pass filter, peak detector, and comparator. The waveforms in this process are shown in the attached block diagram.

5.2 Modulator (AFSK)

On the basis of the 10 MHz crystal oscillator, necessary frequencies are divided by dividers and used. The dividing schedule from 10 MHz is as shown below.



The dividing output of IC17, 18 is the total of dividing ratios in all lines where diodes are provided„

Example: Low mark: 1 + 4 + 16 + 32 + 64 + 128 = 245

Input frequency		Dividing ratio		Output frequency
625 kHz	:	245	=	2551.02 Hz

The output divided by the programmable divider is divided again to 1/2, and converted to a necessary frequency of 50 % duty.

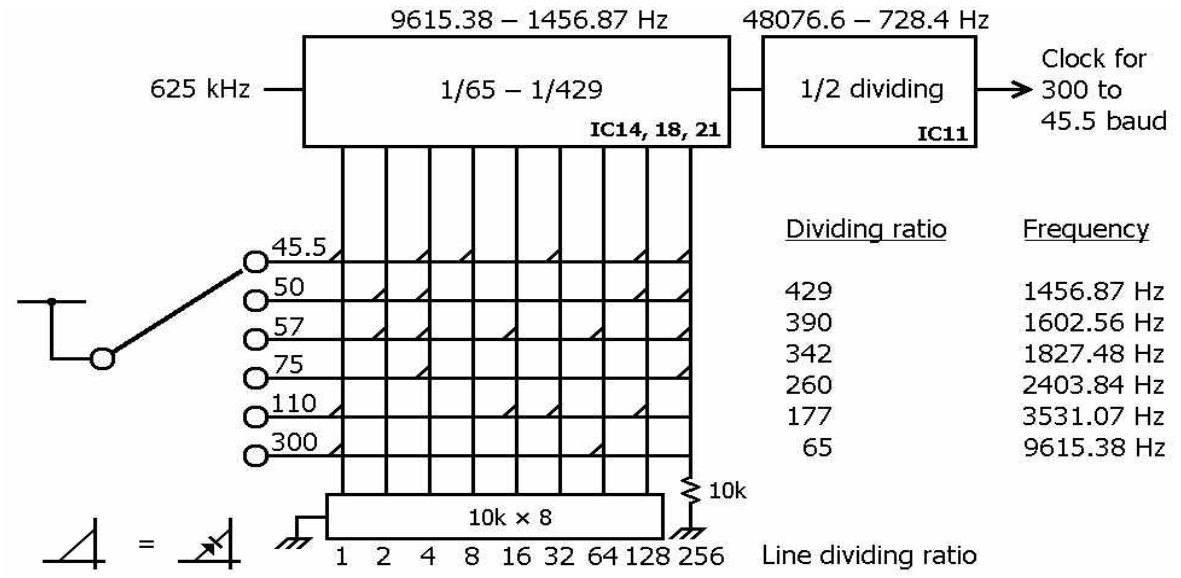
One of the converted outputs is passed through audio amplifiers TR3, TR4 to become a monitor sound output, while the other output runs through the AFSK gain VR and enters the LPF to be corrected in waveform, and becomes an AFSK output.

The AFSK Output can be checked on the TP-9.

5.3 Baud rate clock unit

On the basis of the 10 MHz crystal oscillator in the modulator and the 625 kHz signal being divided to 1/16, signals are divided to necessary frequency to be delivered.

The dividing schedule from 625 kHz is as shown below:

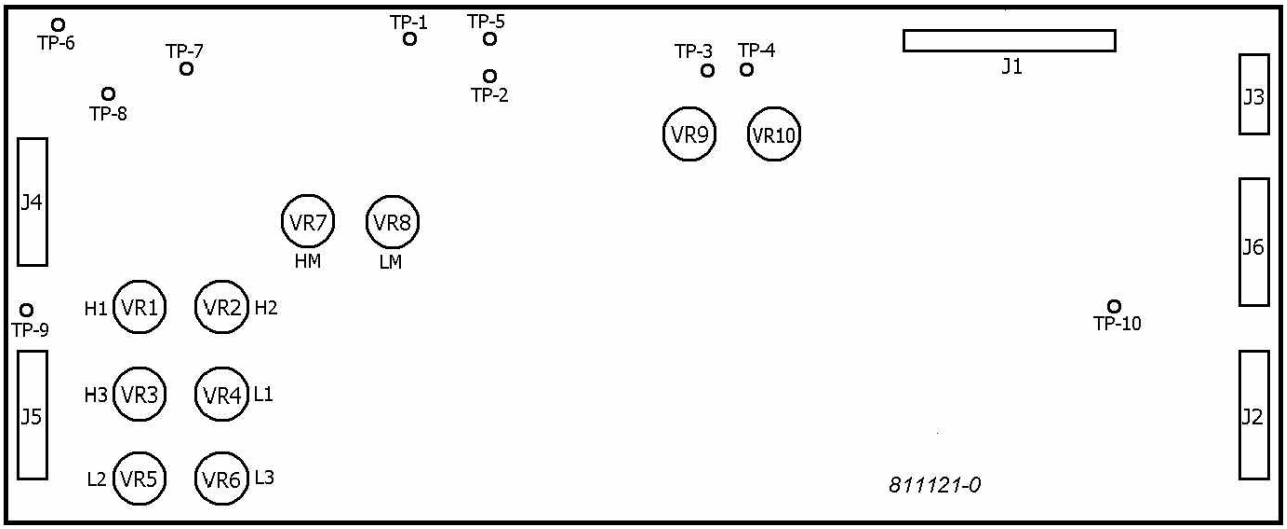


The dividing output of IC14, 18, 21 is the total of dividing ratios in all lines. The output being divided by this divider is divided again to 1/2 and converted to a necessary frequency of 50 % duty to delivered. This output of baud rate clock can be checked on the TP-10.

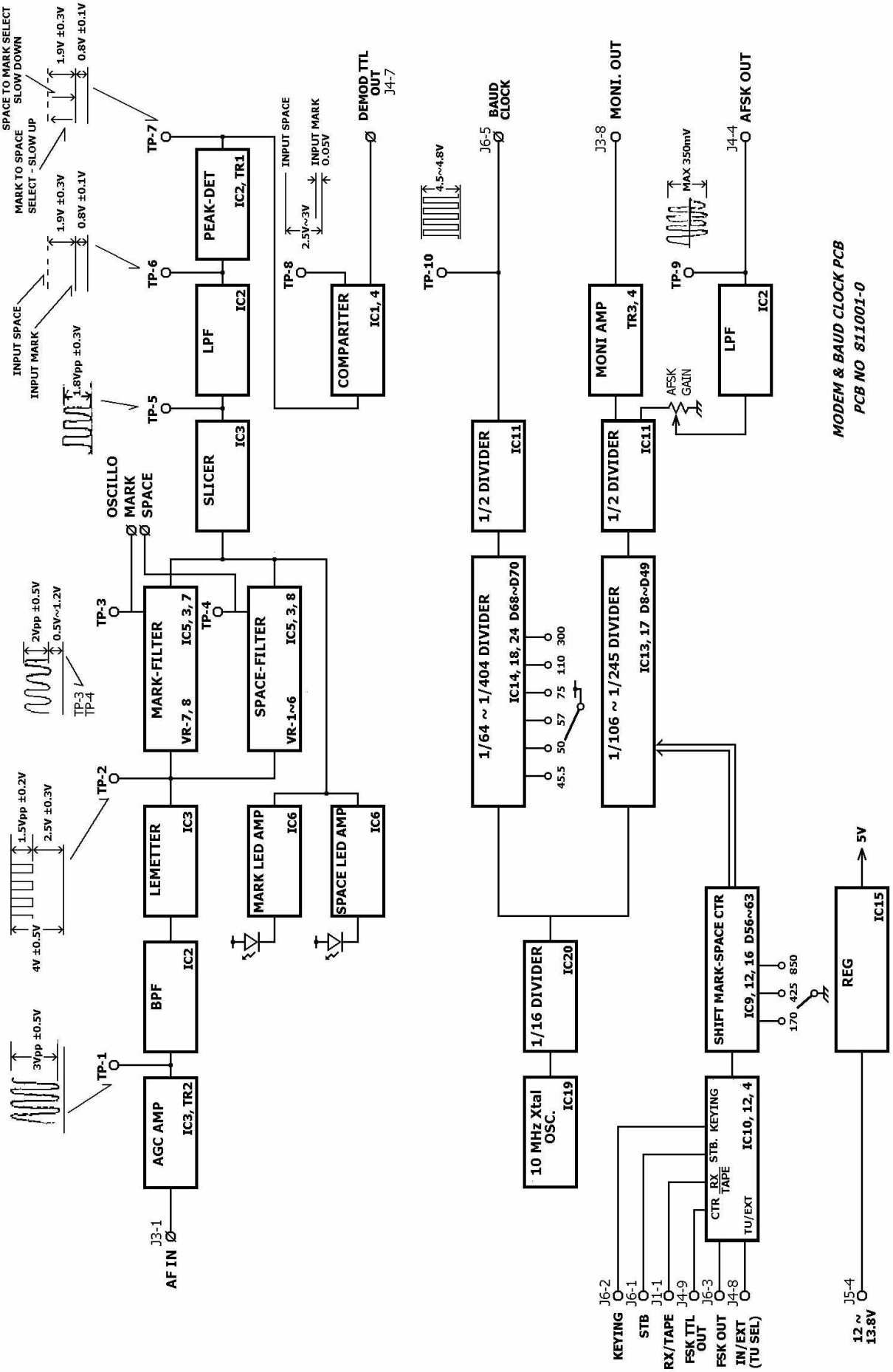
The relation between baud rate and clock frequency is as follows:

Clock frequency = Baud rate × 16

Positions of adjusting VRs and test points on PCB:



5.4 MODEM printed circuit board block diagram



6. Troubleshooting of MODEM printed circuit board

6.1 Demodulator

Preparation

(1) Set the MODEM selector on the back panel to INT side.

(2) Connect AFSK OUT TX and AF OUT on back panel.

(3) Set RX/TAPE selector on front panel to RX position.

(4) Set the other switches on the front panel to be ready to send and receive in RTTY mode.

(5) Feed CTR+E from keyboard, and set in echo-back mode.

(6) Transmit RYRYRY from keyboard.

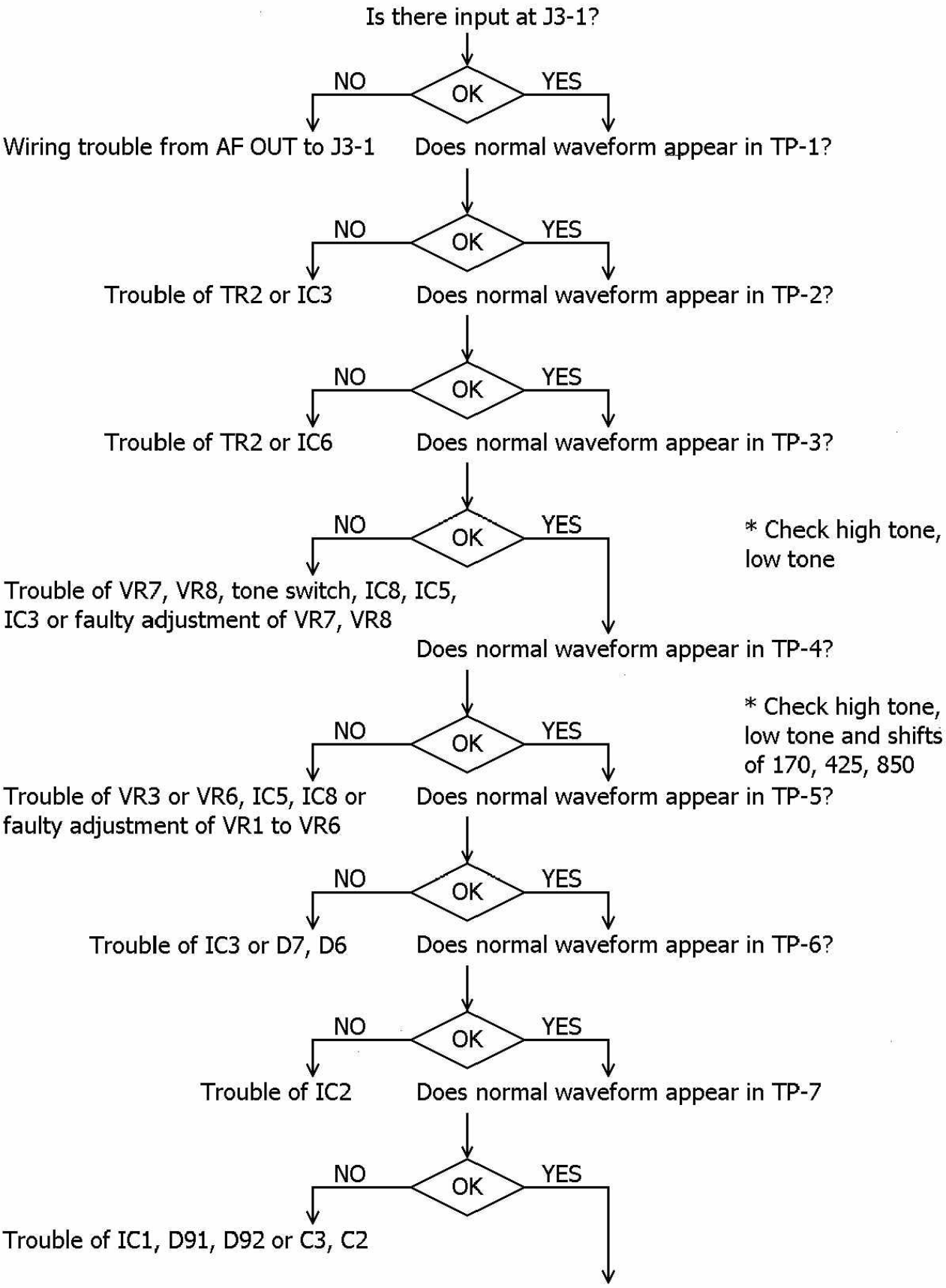
In this operation, a self-diagnosis loop is made.

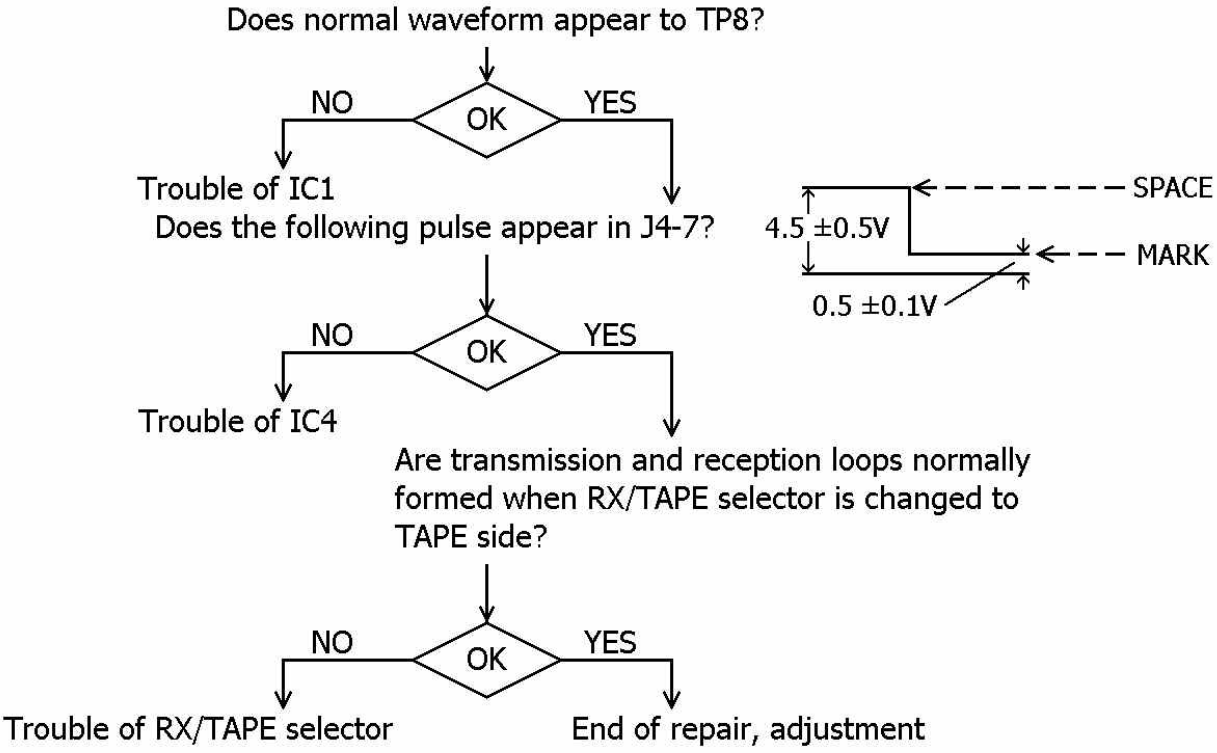
In normal state

Regardless of the selected position of RX/TAPE selector on the front panel, transmission and reception are formed in loop, and RY signals are sent and received. (However, it is all right if 300-baud signal is not formed in normal loop in TAPE position.)

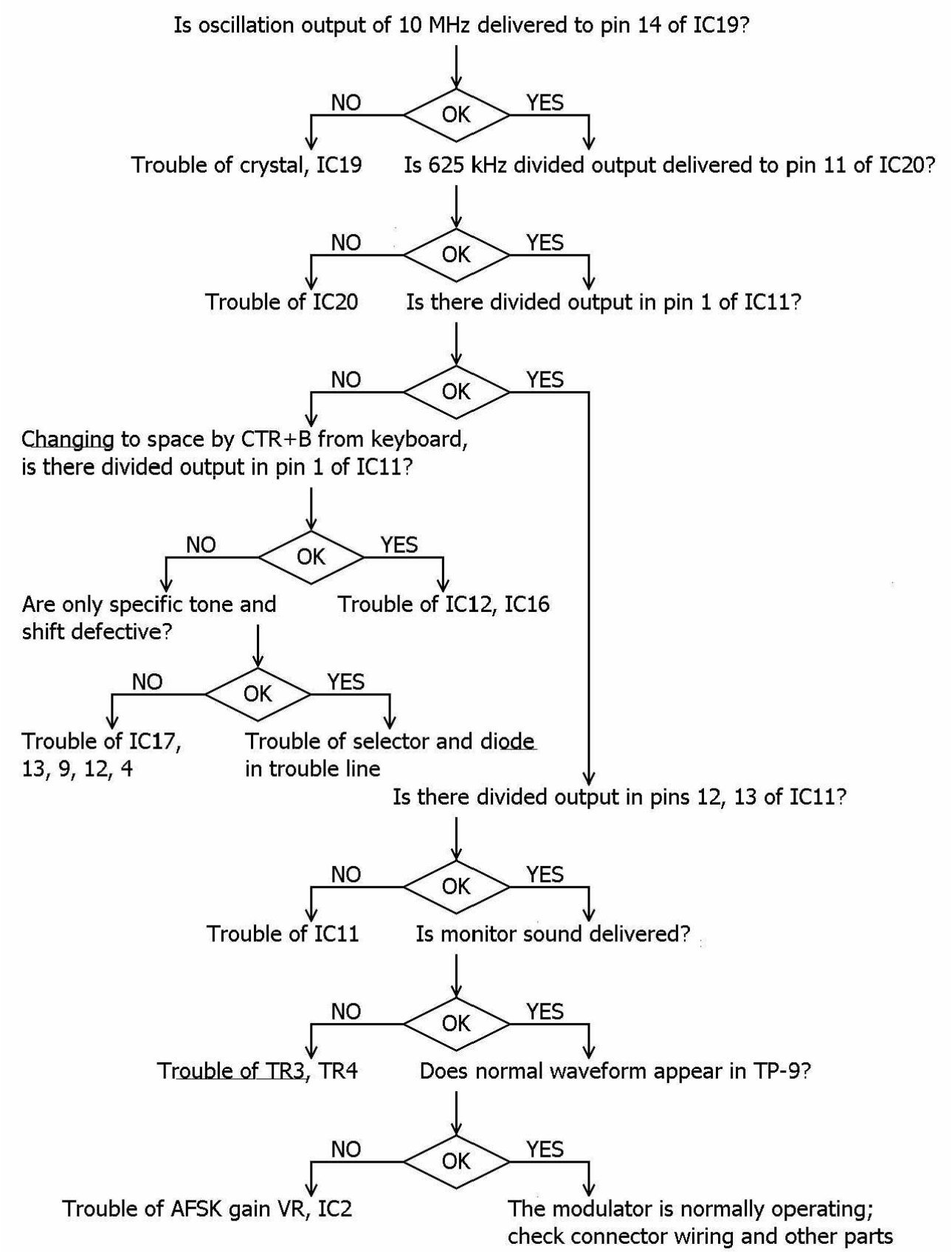
In MODEM board trouble

When the RX/TAPE selector on the front panel is at RX, a normal loop is formed, but when at TAPE side, normal loop is not made.

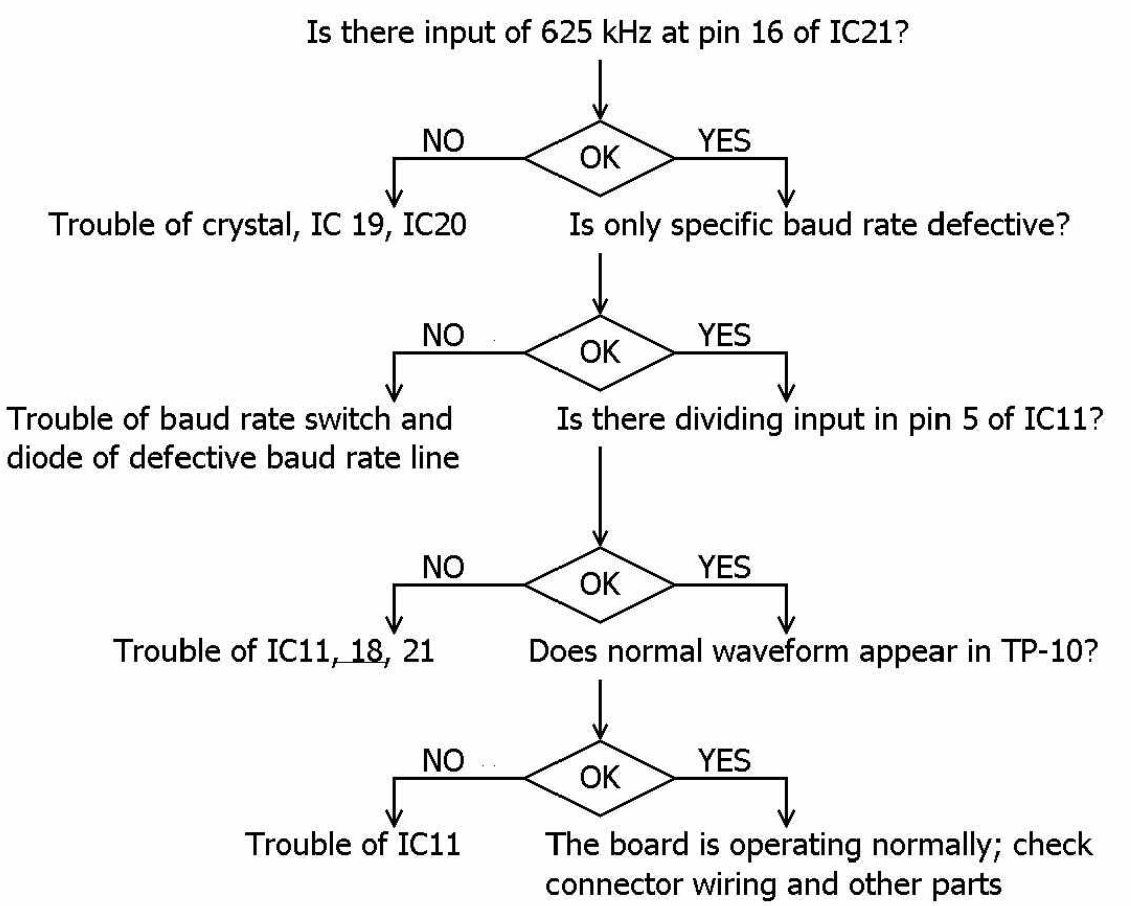

Is there input at J3-1?
NO
OK
YES
Wiring trouble from AF OUT to J3-1
Does normal waveform appear in TP-1?
NO
OK
YES
Trouble of TR2 or IC3
Does normal waveform appear in TP-2?
NO
OK
YES
Trouble of TR2 or IC6
Does normal waveform appear in TP-3?
NO
OK
YES
* Check high tone, low tone
Trouble of VR7, VR8, tone switch, IC8, IC5, IC3 or faulty adjustment of VR7, VR8
Does normal waveform appear in TP-4?
NO
OK
YES
* Check high tone, low tone and shifts of 170, 425, 850
Trouble of VR3 or VR6, IC5, IC8 or faulty adjustment of VR1 to VR6
Does normal waveform appear in TP-5?
NO
OK
YES
Trouble of IC3 or D7, D6
Does normal waveform appear in TP-6?
NO
OK
YES
Trouble of IC2
Does normal waveform appear in TP-7
NO
OK
YES
Trouble of IC1, D91, D92 or C3, C2


Does normal waveform appear to TP8?
NO
OK
YES
Trouble of IC1
Does the following pulse appear in J4-7?
SPACE
4.5 ±0.5V
MARK
0.5 ±0.1V
NO
OK
YES
Trouble of IC4
Are transmission and reception loops normally formed when RX/TAPE selector is changed to TAPE side?
NO
OK
YES
Trouble of RX/TAPE selector
End of repair, adjustment

6.2 Modulator (AFSK)



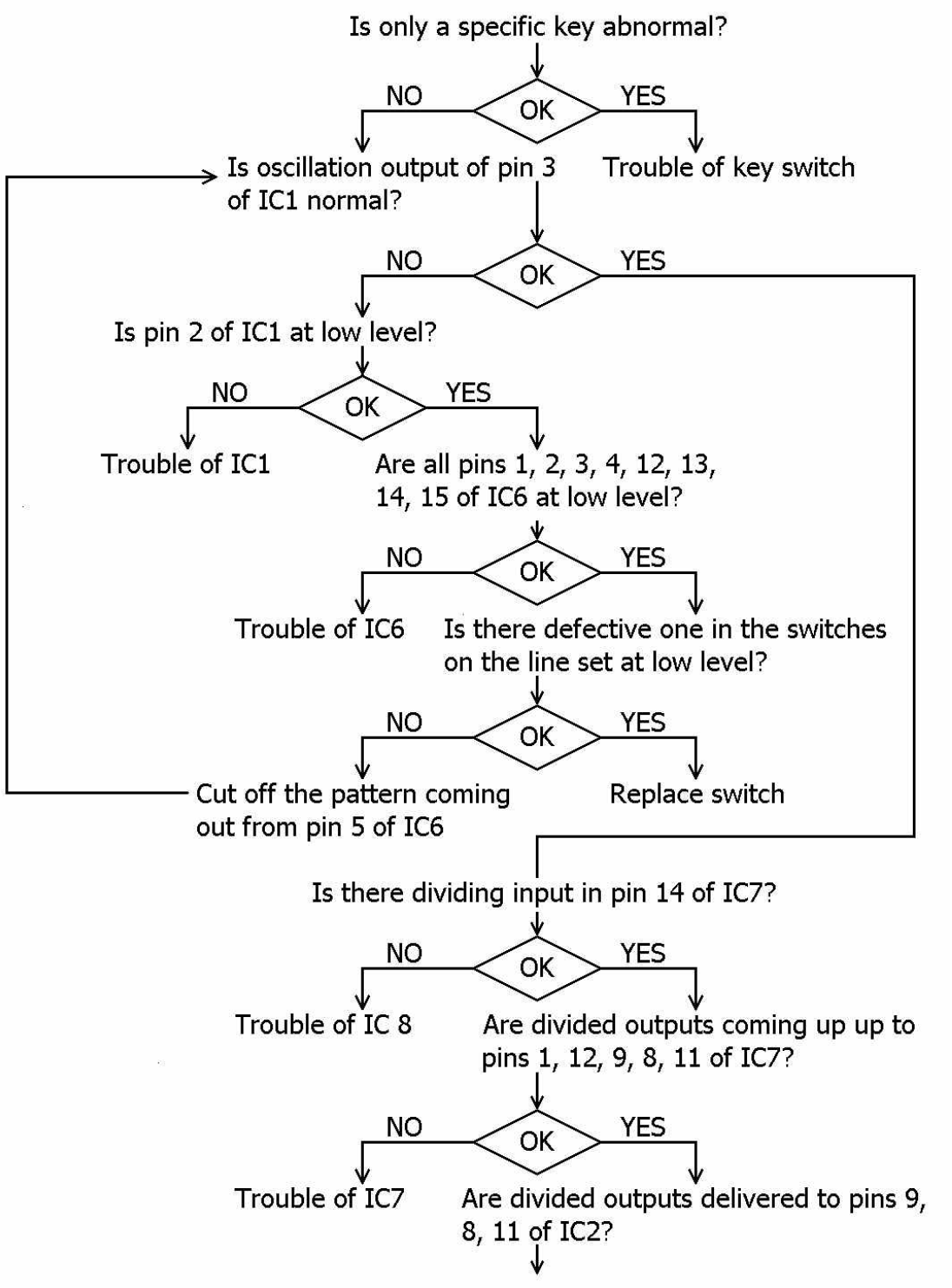
6.3 Baud rate clock unit

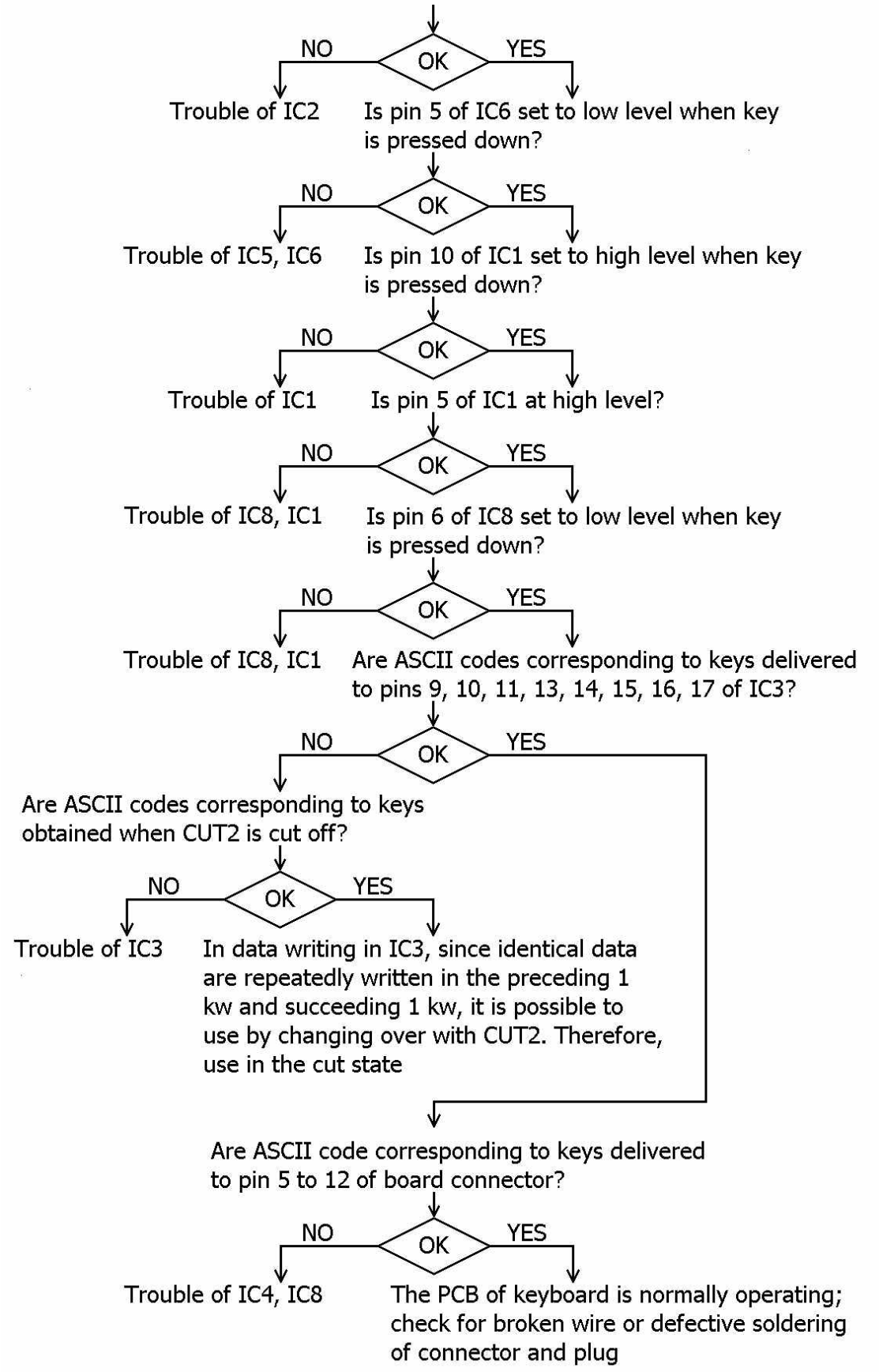


7. Keyboard troubleshooting (KB-685E, KB-6850

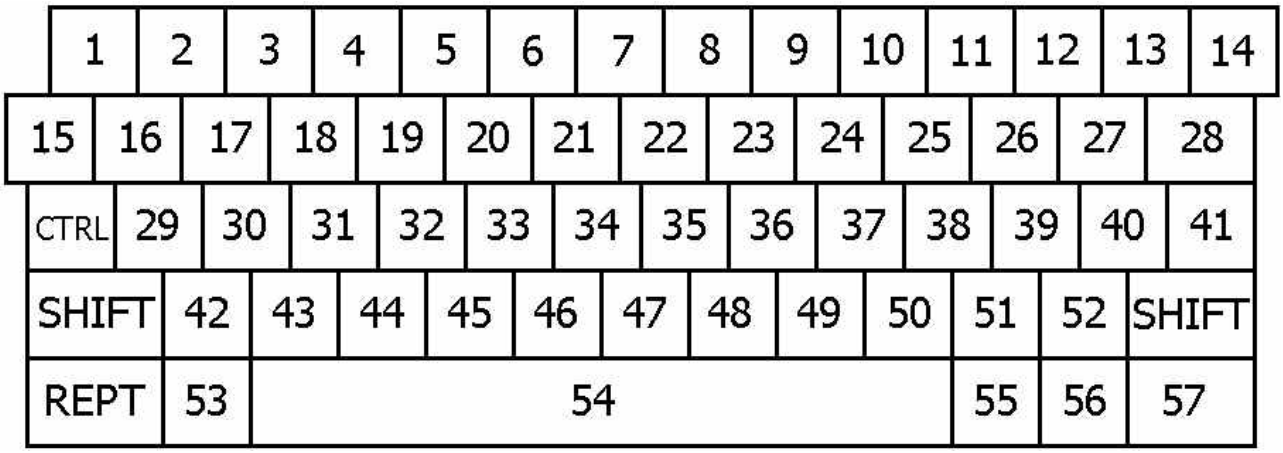
7.1 Troubleshooting flow chart of keyboard (PCB No. 820226-1)

Referring to the attached wiring diagram, check the keyboard in connected state.




OK
NO
YES
Trouble of IC2
Is pin 5 of IC6 set to low level when key is pressed down?
OK
NO
YES
Trouble of IC5, IC6
Is pin 10 of IC1 set to high level when key is pressed down?
OK
NO
YES
Trouble of IC1
Is pin 5 of IC1 at high level?
OK
NO
YES
Trouble of IC8, IC1
Is pin 6 of IC8 set to low level when key is pressed down?
OK
NO
YES
Trouble of IC8, IC1
Are ASCII codes corresponding to keys delivered to pins 9, 10, 11, 13, 14, 15, 16, 17 of IC3?
OK
NO
YES
Are ASCII codes corresponding to keys obtained when CUT2 is cut off?
OK
NO
YES
Trouble of IC3
In data writing in IC3, since identical data are repeatedly written in the preceding 1 kw and succeeding 1 kw, it is possible to use by changing over with CUT2. Therefore, use in the cut state
Are ASCII code corresponding to keys delivered to pin 5 to 12 of board connector?
OK
NO
YES
Trouble of IC4, IC8
The PCB of keyboard is normally operating; check for broken wire or defective soldering of connector and plug

7.2 List of keyboard output codes



	NORMAL	SHIFT	CTRL	CTRL-SHIFT
1	1	!		
2	2	"		
3	3	#		
4	4	$		
5	5	%		
6	6	&		
7	7	'		
8	8	(		
9	9	)		
10	0	NUL		
11	-	=	(-)	(=)
12	^	~	RS	(^)
13	\	|	FS	(\)
14	(BS)	(ETB)	BS	(CAN)
15	(ESC)	(SUB)	(DLE)	CAN
16	q	Q	DCI	(Q)
17	w	W	ETB	(W)
18	e	E	ENQ	(E)
19	r	R	DC2	(R)
20	t	T	DC4	(T)
21	y	Y	EM	(Y)
22	u	U	NAK	(U)
23	i	I	HT	(I)
24	o	O	SI	(O)
25	p	P	DLE	(P)
26	@	`	NUL	(@)
27	[	{	ESC	([)
28	(CR)	CR	CR	CR
29	a	A	SOH	(A)
30	s	S	DC3	(S)

	NORMAL	SHIFT	CTRL	CTRL-SHIFT
31	d	D	EOT	(D)
32	f	F	ACK	(F)
33	g	G	BEL	(G)
34	h	H	BS	(H)
35	j	J	LF	(J)
36	k	K	VT	(K)
37	l	L	FF	(L)
38	;	+	(;)	(+)
39	:	*	(:)	(*)
40	]	}	GS	(])
41	LF	LF	LF	LF
42	z	Z	SUB	(Z)
43	x	X	CAN	(X)
44	c	C	ETX	(C)
45	v	V	SYN	(V)
46	b	B	STX	(B)
47	n	N	SO	(N)
48	m	M	CR	(M)
49	,	<	(,)	(<)
50	.	>	(.)	(>)
51	/	?	(/)	(?)
52	BEL	_	US	(DEL)
53	(HT)	(VT)	(FF)	(SHO)
54	SP	(SP)	(FS)	(GS)
55	(SI)	SI	SI	SI
56	(SO)	SO	SO	SO
57	(DEL)	ENQ	(ACK)	DEL

8. Description of former MODEM board

In models from lot numbers 21xxxx to 23xxxx, the type of MODEM board differs. The board for repair is 811001-0 only, which can be replaced without modification.

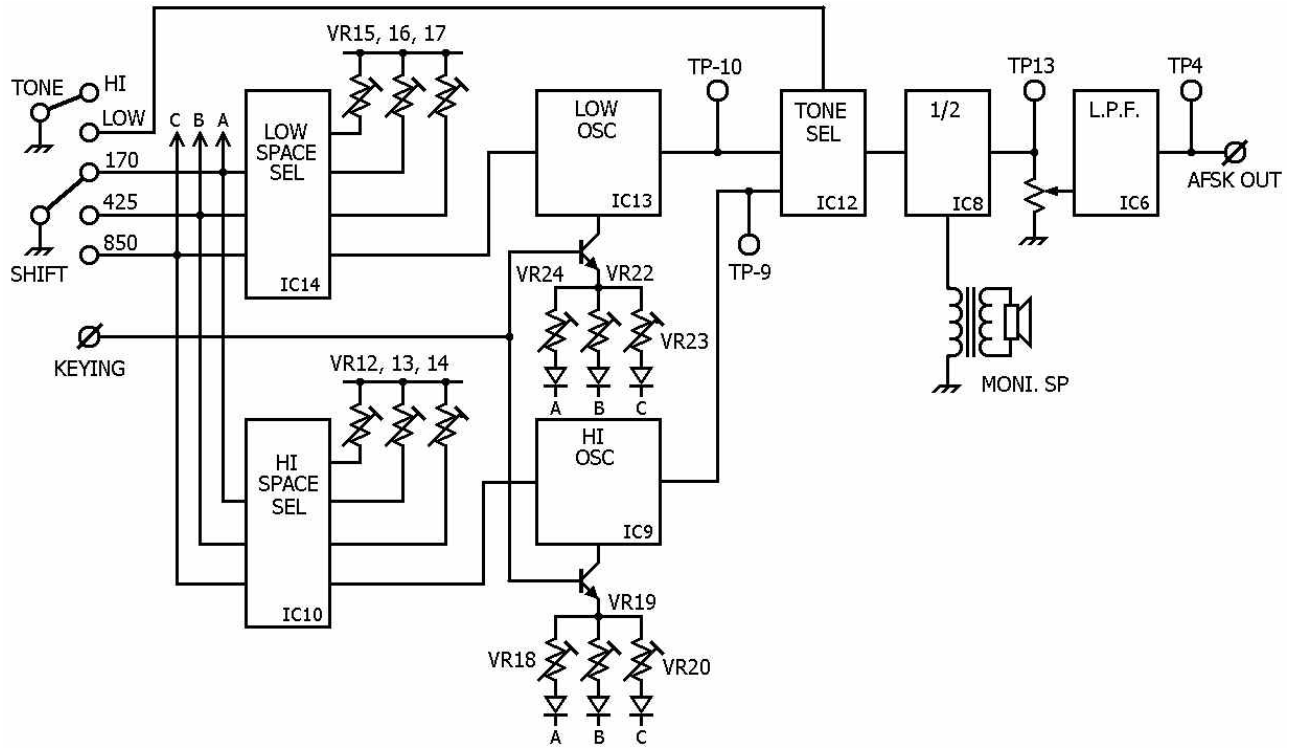
The demodulator is same as 811001-0, but since the IC numbers and VR numbers differ, refer to the wiring diagram.

The correspondence of VR numbers is as follows:

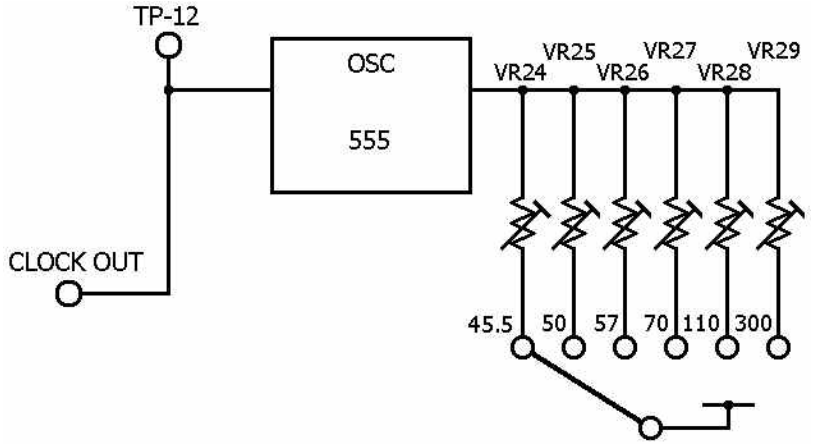
801230-0	811001-1	Frequency
VR-4	VR-2	2550 Hz
VR-5	VR-3	2975 Hz
VR-6	VR-1	2295 Hz
VR-7	VR-6	1700 Hz
VR-8	VR-5	2125 Hz
VR-9	VR-4	1445 Hz
VR-10	VR-7	2125 Hz
VR-11	VR-8	1275 Hz

Modulator (AFSK)

In the modulation system using timer IC, two sets of AFSK are changed over for each tone.



Baud rate clock



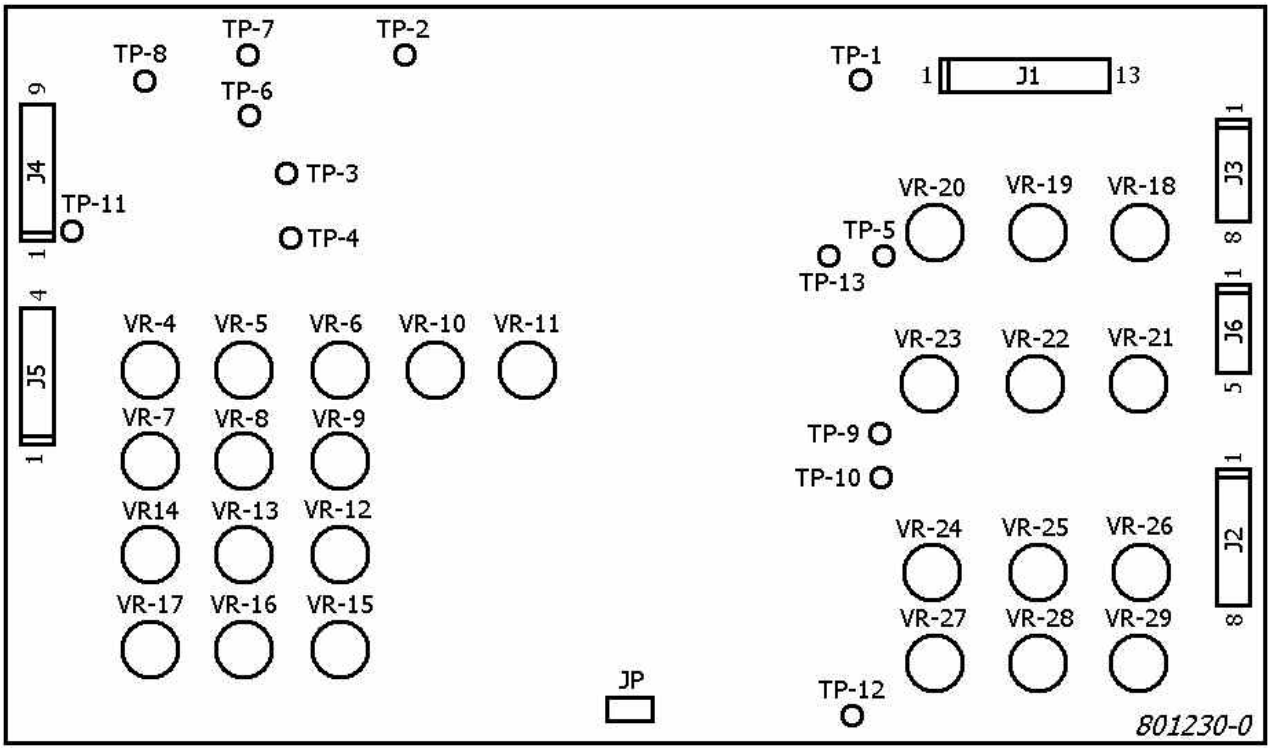
The baud rate clock adjusts the voltage applied to pin 7 of timer IC, and necessary frequencies are picked up.

For readjustment, adjust the VRs by connecting oscilloscope to the TP-12.

The relation between the baud rate, frequency, and time is as follows:

Baud rate	Frequency (f) Hz	Time (T) ms
45.5	728	1.37
50	800	1.25
57 (56.92)	910.7	1.1
75 (74.2)	1187.2	0.842
110	1760	0.568
300	4800	0.208

Layout of adjusting VRs and test points



9. Parts list

Semiconductor Parts List (1)

1. Main PCB (No. 810529-1)

Code No.	Name	Type	Maker	Part No.
IC1	IC	LS. TTL	Hi	HD74LS00 or equivalent
IC2	IC	LS., TTL	Hi	HD74LS74 "
IC3	IC	LS. TTL	Hi	HD74LS74 "
IC4	IC	LS . TTL	Hi	HD74LS163 "
IC5	IC	LS . TTL	Hi	HD74LS04 "
IC6	IC	CMOS	To	TC4011 "
IC7	IC	LS . TTL	Hi	HD74LS157 "
IC8	IC	"	"	" "
IC9	IC	"	"	" "
IC10	IC	LS . TTL	Hi	HD74LS166 "
IC11	IC	LS . TTL	Hi	HD74LS86 "
IC12	IC	LS . TTL	Hi	HD74LS00 "
IC13	IC	RAM	Na	MN2114-3 "
IC14	IC	RAM	"	" "
IC15	IC	RAM	"	" "
IC16	IC	RAM	"	" "
IC17	IC	ROM	Hi	HN462716-G "
IC18	IC	CRTC	Hi	HD46505SP "
IC19	IC	LS . TTL	Hi	HD74LS249 "
IC20	IC	LS . TTL	Hi	HD74LS32 "
IC21	IC	CMOS	To	TC4069 "
IC22	IC	LS . TTL	Hi	HD74LS04 "
IC23	IC	LS . TTL	Hi	HD74LS08 "
IC24	IC	LS . TTL	Hi	HD74LS32 "
IC25	IC	LS . TTL	Hi	HD74LS08 "
IC26	IC	LS . TTL	Hi	HD74LS86 "
IC27	IC	LS . TTL	Hi	HD74LS273 "
IC28	IC	PCI	NEC	D8251AC(P) "
IC29	IC	ROM	Hi	HN462716G "
IC30	IC	ROM	Hi	HN462732G "
IC31	IC	CPU	Hi	HD46802P "
IC32	IC	PIA	Hi	HD46821P "
IC33	IC	LS . TTL	Hi	HD74LS04 "
IC34	IC	LS . TTL	Hi	HD74LS367 "
IC35	IC	TIM	Hi	HA17555PS or NSNE555
IC36	IC	LS . TTL	Hi	HD74LS42 or equivalent
IC37	IC	LS . TTL	Hi	" "
IC38	IC	LS . TTL	Hi	HD74LS04 "
IC39	IC	LS . TTL	Hi	HD74LS00 "
IC40	IC	LS . TTL	Hi	HD74LS367 "
IC41	IC	LS . TTL	Hi	HD74LS00 or equivalent
IC42	IC	OP. AMP	M	MC3301 or M LM-3900
IC43	IC	CMOS	To	TC4050 or equivalent
IC44	IC	PLL	To	TA7157AP
IC45	IC	LS. TTL	Hi	HD74LS307 or equivalent
IC46	IC	LS . TTL	Hi	HD74LS367 "
IC47	IC	REG		HA17805P "
IC48	IC	REG	Hi	HA17805P "
D1	Di	R	Hi	V06C "
D2-D9	Di	SW	To	IS1588 "
D10-D12	Di	R	Hi	V06C "

D13-D14	Di	SW	To	IS15S3	"
D15	Di	R	Hi	V06C	"
D16-D19	Di	SW	To	IS1588	"
D20-D26	Di	R	Hi	V06C	"
D27	Di	SW	To	IS1588	"
R3	Di	ZD	NEC	RD4.7A	"
TR1	TR	RF.SW	To	2SA495	-50 V -150 mA
TR2	TR	RF.SW	To	2SA495	-50 V -150 mA
TR3	TR	AF	To	2SC1815	60 V 150 mA
TR4	TR	AF	To	2SC1815	60 V 150 mA
TR5	TR	PA	Hi	2SB649C	-180 V -1.5 A
TR6	TR	SW	Hi	2SC1515	200 V 50 mA
TR7	TR	SW	Hi	2SC1515	200 V 50 mA
TR8	TR	PA	Hi	2SD669	180 V 1.5 A
TR9	TR	PA	Na	2SC1384C	60 V 1 A
TR10	TR	RF	Hi	2SC2610	300 V 100 mA

Semiconductor Parts List (2)

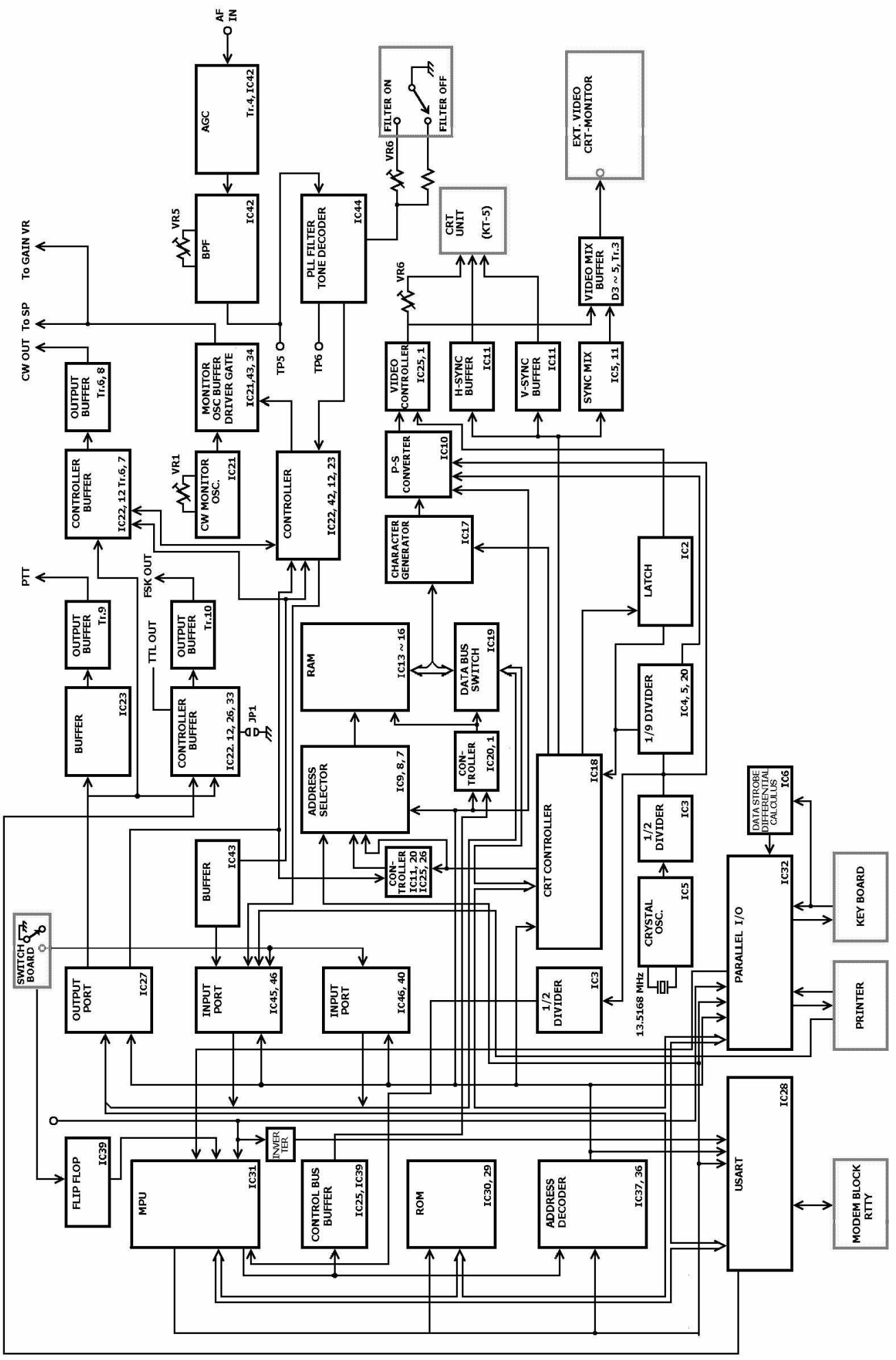
2. MODEM PCB (811001-0)

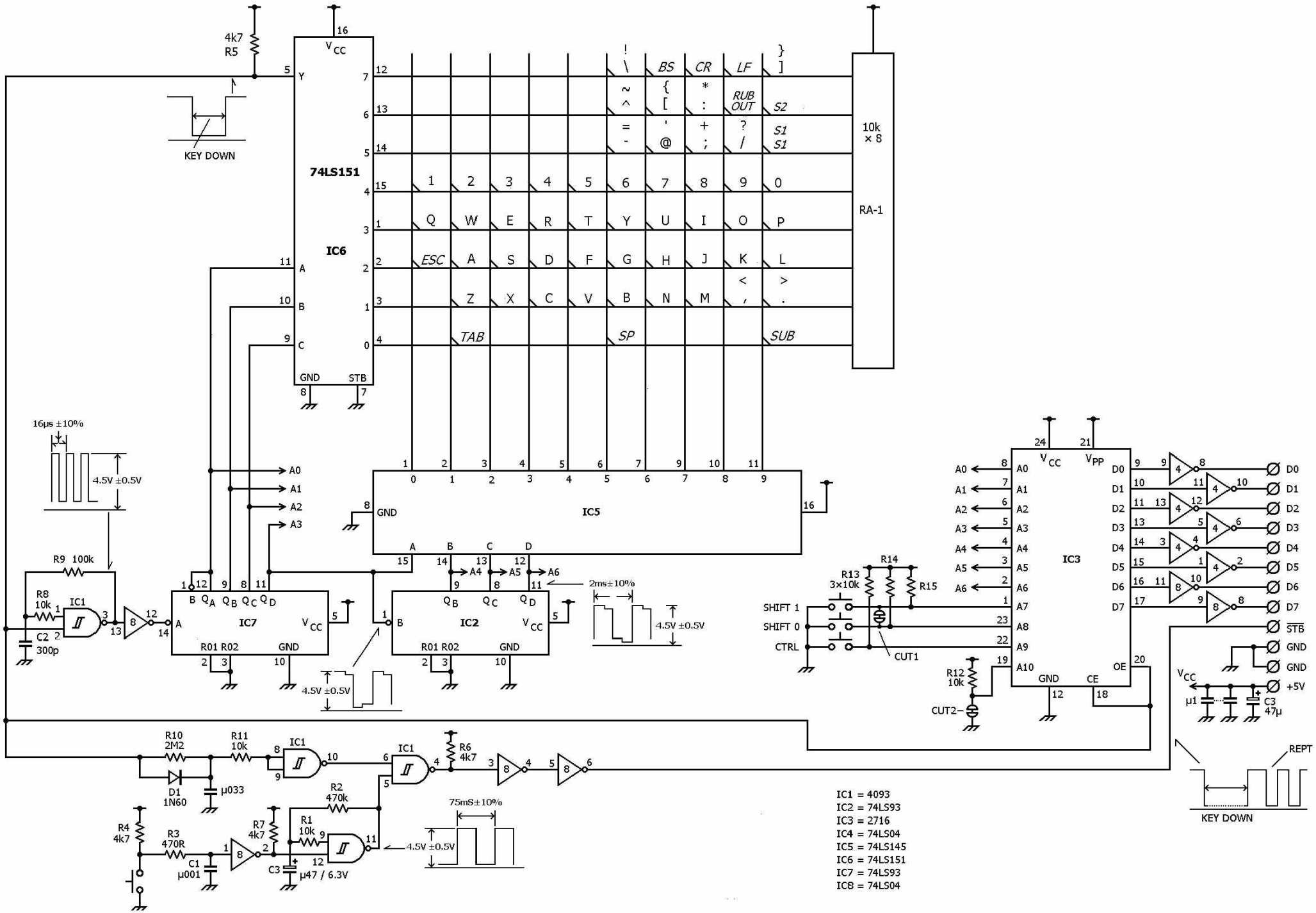
Code No.	Name	Type	Maker	Part No.	
IC1	IC	OP. AMP	M	MC3302 or equivalent	
IC2	IC	OP. AMP	M	MC3403	"
IC3	IC	OP. AMP	M	MC3301	"
IC4	IC	LS. TTL	Hi	HD74LS86	"
IC5	IC	OP. AMP	M	MC3301	"
IC6	IC	OP. AMP	M	MC3302	"
IC7	IC	CMOS	To	TC4051	"
IC8	IC	CMOS	To	TC4053	"
IC9	IC	CMOS	To	TC4051	"
IC10	IC	LS. TTL	Hi	HD74LS00	"
IC11	IC	LS. TTL	Hi	HD74LS73	"
IC12	IC	CMOS	To	TC4069	"
IC13	IC	CMOS	To	TC4526	"
IC14	IC	CMOS	To	TC4526	"
IC15	IC	REG	Hi	HA17805P	"
IC16	IC	CMOS	To	TC4081	"
IC17	IC	CMOS	To	TC4526	"
IC18	IC	CMOS	To	TC4526	"
IC19	IC	LS. TTL	Hi	74LS04	"
IC20	IC	LS. TTL	Hi	74LS93	"
IC21	IC	CMOS	To	TC4526	"
TR1	TR	AF	To	2SC1815	60 V 150 mA
TR2	TR	AF	To	2SC1815	60 V 150 mA
TR3	TR	PA	Na	2SC1318	60 V 500 mA
TR4	TR	PA	Na	2SA720S	-50 V -500 mA
D1-D4	Di	SW	To	IS1588	
D5	Di	R	Hi	V06C	
D6, D7	Di	Ge , SW	Na	OA95	
D8-D92	Di	SW	To	IS1588	

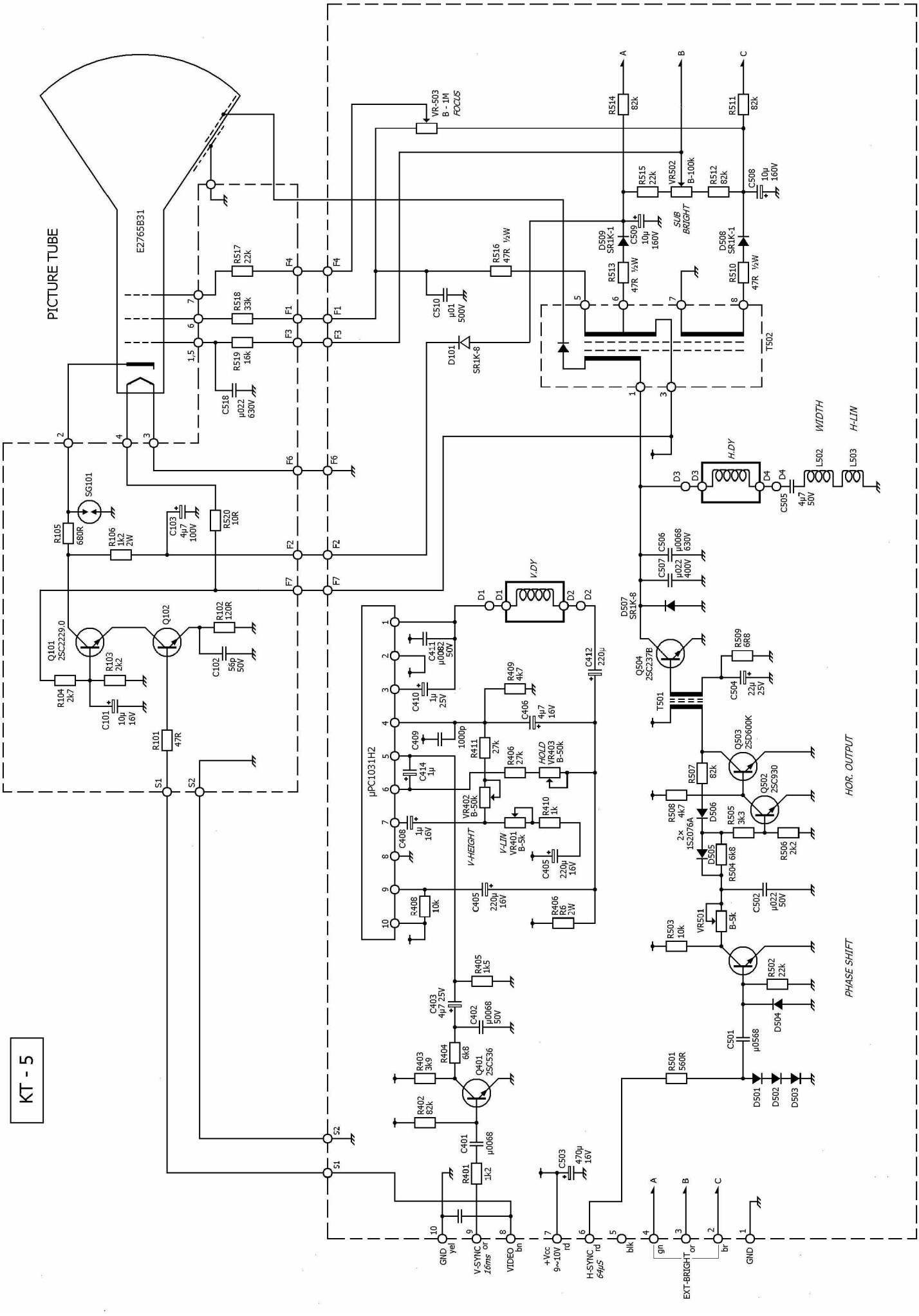
3. Modem PCB (801230-0)

Code No.	Name	Type	Maker	Part No.
IC1	IC	OP. AMP	M	LM339 or equivalent
IC2	IC	OP. AMP	M	LM339 "
IC3	IC	OP. AMP	M	MC3301 "
IC4	IC	CMOS	To	TC4051 "
IC5	IC	OP. AMP	M	MC3301 "
IC6	IC	OP. AMP		LM324 "
IC7	IC			HD14053 "
IC8	IC	TTL		HD7473 "
IC9	IC		Hi	HA17555 "
IC10	IC	CMOS	To	TC4051 "
IC11	IC	LS TTL	Hi	HD74LS00 "
IC12	IC	LS TTL	Hi	HD74LS00 "
IC13	IC			HA17555 "
IC14	IC	CMOS	To	TC4051 "
IC15	IC	LS TTL		SN74LS86 "
IC16	IC			555JRC1015 "

BLOCK DIAGRAM




4k7
R5
KEY DOWN
74LS151
IC6
10k
× 8
RA-1
BS
CR
LF
RUB
OUT
S2
S1
S1
TAB
SP
SUB
ESC
16µs ±10%
4.5V ±0.5V
R9 100k
R8
10k
C2
300p
IC1
IC7
IC5
IC2
A0
A1
A2
A3
A4
A5
A6
2ms±10%
4.5V ±0.5V
SHIFT 1
SHIFT 0
CTRL
R13
3×10k
R14
R15
CUT1
CUT2
R12
10k
IC3
D0
D1
D2
D3
D4
D5
D6
D7
STB
GND
+5V
C3
47µ
R10
2M2
R11
10k
D1
1N60
µ033
R6
4k7
R2
470k
R1
10k
R4
4k7
R3
470R
R7
4k7
C1
µ001
C3
µ47 / 6.3V
75mS±10%
REPT
IC1 = 4093
IC2 = 74LS93
IC3 = 2716
IC4 = 74LS04
IC5 = 74LS145
IC6 = 74LS151
IC7 = 74LS93
IC8 = 74LS04


KT - 5
PICTURE TUBE
E2765B31
VR-503 B - 1M FOCUS
SG101
Q101 2SC2229-0
Q102
µPC1031H2
V-DY
H-DY
WIDTH
H-LIN
V-HEIGHT
V-LIN
HOLD
SUB BRIGHT
HOR. OUTPUT
PHASE SHIFT
D101 SR1K-8
D507 SR1K-8
D508 SR1K-1
D509 SR1K-1
T501
T502
Q503 2SD600K
Q502 2SC930
Q504 2SC237B
Q401 2SC536
VR402 B-50k
VR403 B-50k
VR401 B-5k
VR501 B-5k
VR502 B-100k
GND yel
V-SYNC or 16ms
VIDEO bn
+Vcc 9~10V rd
H-SYNC rd 64µS
blk
EXT-BRIGHT or
br
GND