

Grounding pin 14 (CKE output) at pin 8 (ground) on the rear panel accessory connector will extend the frequency ranges to:

Band - Extended coverage - Factory coverage

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160m - 1.0 - 3.0 MHz      - 1.8 - 2.0 MHz  
80m  - 3.0 - 5.0 MHz      - 3.5 - 4.0 MHz  
40m  - 7.0 - 9.0 MHz      - 7.0 - 7.5 MHz  
                                7.3 - 7.5 MHz Receive Only  
20m  - 14.0 - 16.0 MHz    - 14.0 - 15.2 MHz  
                                14.35 - 15.2 MHz Receive Only  
15m  - 21.0 - 22.0 MHz    - 21.0 - 21.5 MHz  
10m  - 28.0 - 30.0 MHz    - 28.0 - 30.0 MHz  
                                29.7 - 30.0 MHz Receive Only
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Attention: on IC-710, IC-701 japanese market version no accessory connector. With the IC-701 schematic, connecte CKE output pin 2 on ground of connector P6 inside of IC-710.

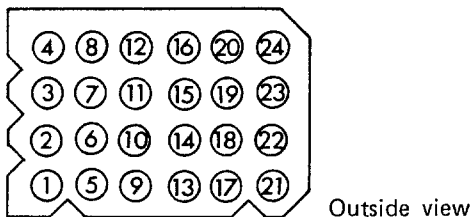
The ICOM IC-701 originally has no 11 meter band on it. The conversion mentioned below will also change the display to 27MHz instead of 28MHz. First locate the crystal X6 inside the PLL case which has label 40.625MHz and replace it with frequency 40.125MHz with the same crystal characteristic. Slightly adjust the tuning slug for 27MHz on the PLL case.

Cut diode D34 and D35 on matrix board behind the front panel to show 27MHz on the display.

For information, crystal X3 with frequency 30.125MHz is for 7MHz band, X4 33.625MHz is for 14MHz band, X6 40.625 is for 28MHz band.

5-5-8 CONNECTION OF ACCESSORY SOCKET

Various adapters can be used through terminals in this SOCKET for frequency control input, modulation output, receiver output, T/R change-over control and so on. The table below shows terminal connections of this connector. Care should be taken not to apply voltages other than -0.5 V to $+5$ V to terminals between No. 14 and No. 24 as they are connected with the C-MOS IC.



ACC SOCKET CONNECTIONS

PIN No.	FUNCTION
1.	NC (no connection)
2.	13.8 Volts DC in conjunction with the power switch operation.
3.	Connected to Push-to-talk, T/R change-over switch. When grounded, the set operates in the transmit mode.
4.	Output from the receiver detector stage. Fixed output regardless of AF output or AF gain.

PIN No.	FUNCTION
5.	Output from Transmitter MIC amplifier stage.
6.	8 Volts DC available when transmitting. (relay can not be directly actuated.)
7.	Input for external ALC voltage.
8.	Ground
9.	Input for RTTY keying (MARK: HIGH level, SPACE: LOW level).
10.	8 Volts DC available when the 28MHz band is selected.
11.	Input for TRANSVERTER control. When 8 Volts DC is applied, set can operate with a transverter.
12.	Output reference voltage for band switching.
13.	INPUT/OUTPUT for external band switching.
14.	CKE Output HIGH level at band edge.
15.	LOCK Input to lock dial externally.
16.	UDC Input to control Up/Down counter externally.
17.	SCAN Input to scan frequency.
18.	CL Input to clear frequency.
19.	FCL Input to clear counter in specified digit and input for MSB data.
20.	K0 Input for frequency control data.
21.	K1 Input for frequency control data.
22.	K2 Input for frequency control data.
23.	K4 Input for frequency control data.
24.	K8 Input for frequency control data.

SECTION 6 THEORY

OUT LINE

The IC-701 employs a digital phase locked loop (PLL) circuit as the local oscillator for both transmit and receive. The output of the PLL circuit is approximately 9MHz above the receive frequency, thereby spurious is kept to a minimum.

The frequency is determined as follows. A pulse generated by the optical chopper circuit, located at the tuning knob, is digitalized by the up/down counter in the LSI (ICOM's custom developed Large Scale Integrated circuit) and used to control a programmable divider, also located inside the LSI chip. The programmable divider controls the PLL circuit which determines the output frequency of the VCO (Voltage Controlled Oscillator).

In the receiver section, signals from the antenna are mixed with the local oscillator output from the PLL circuit. After passing through the pass band tuning circuit, the signals are amplified then detected to become audio signals, amplified again and sent to the speaker.

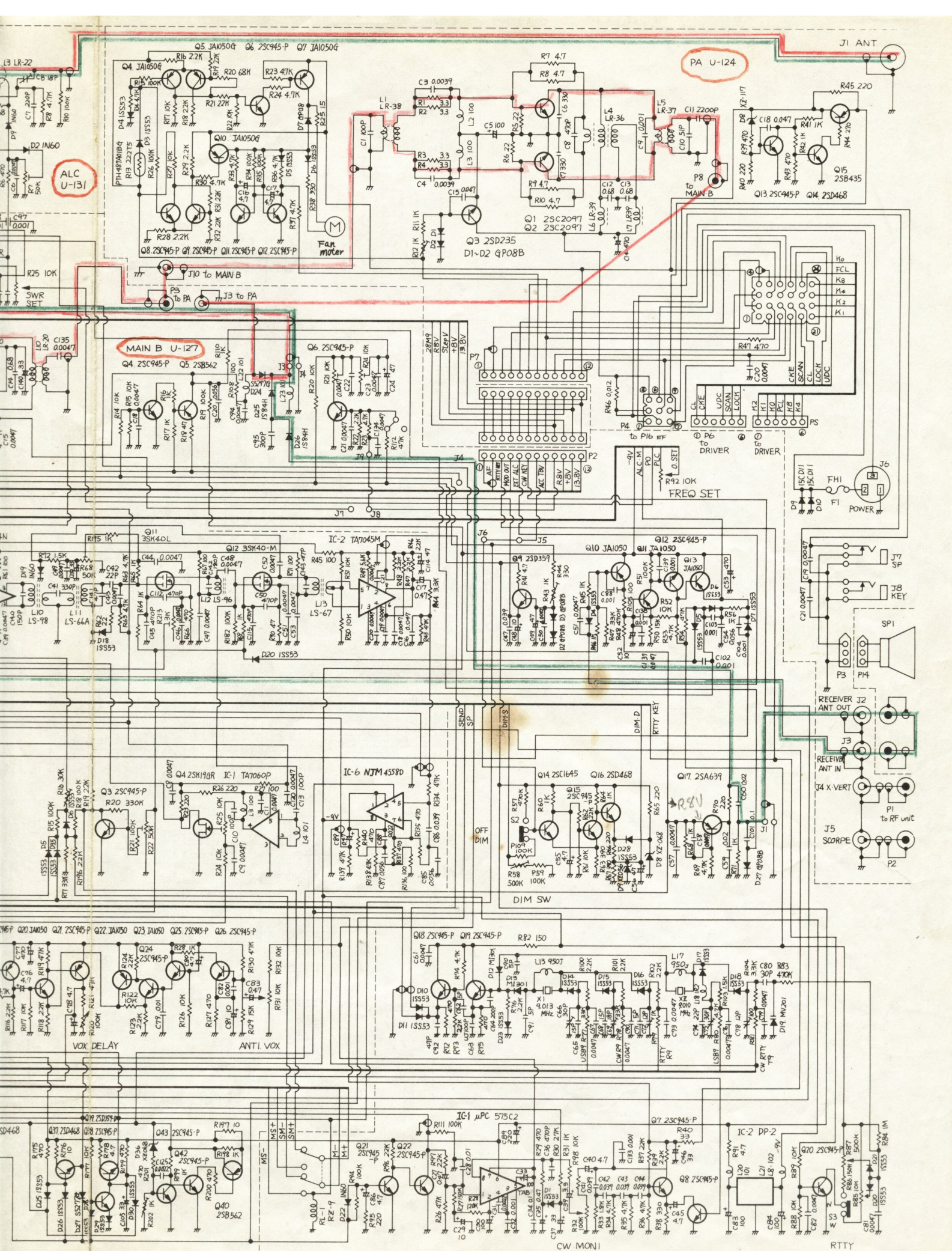
The transmitter uses a carrier of 9.013MHz for USB and 9.010MHz for LSB. The carrier and the voice signal are sent to a balanced modulator where the DSB suppressed

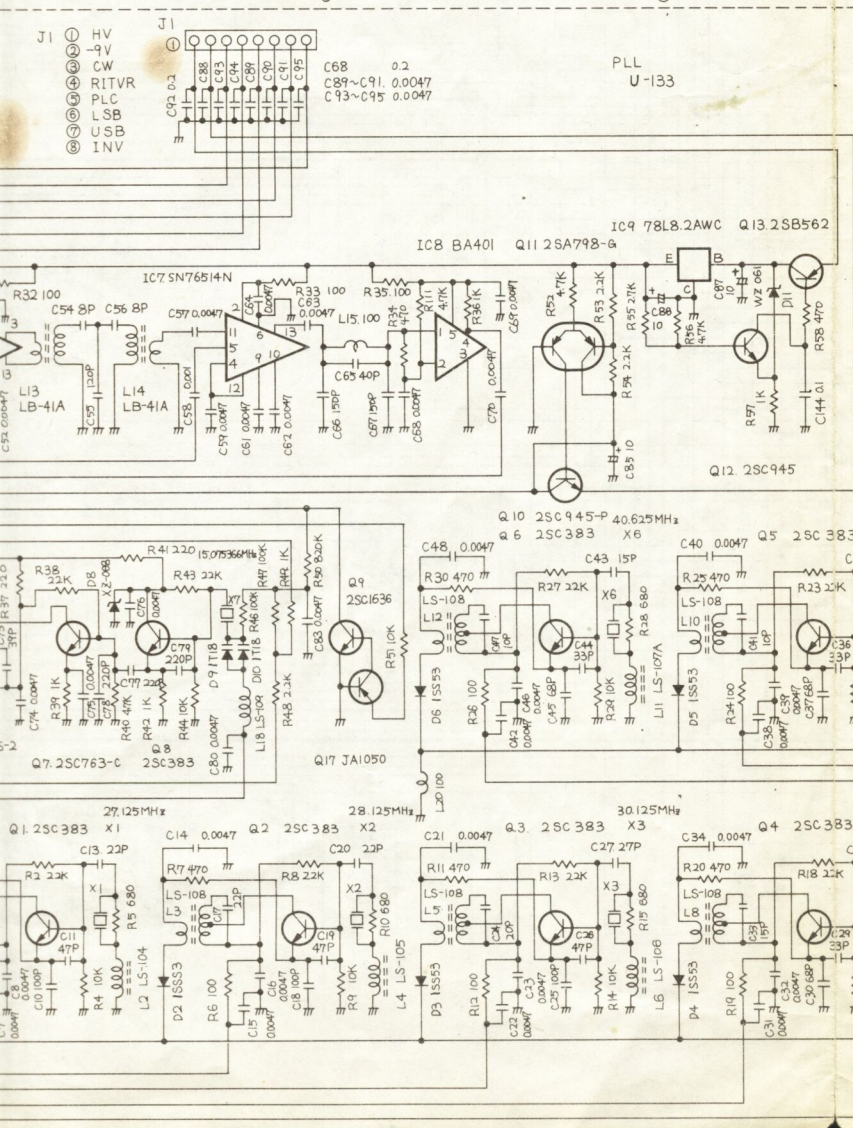
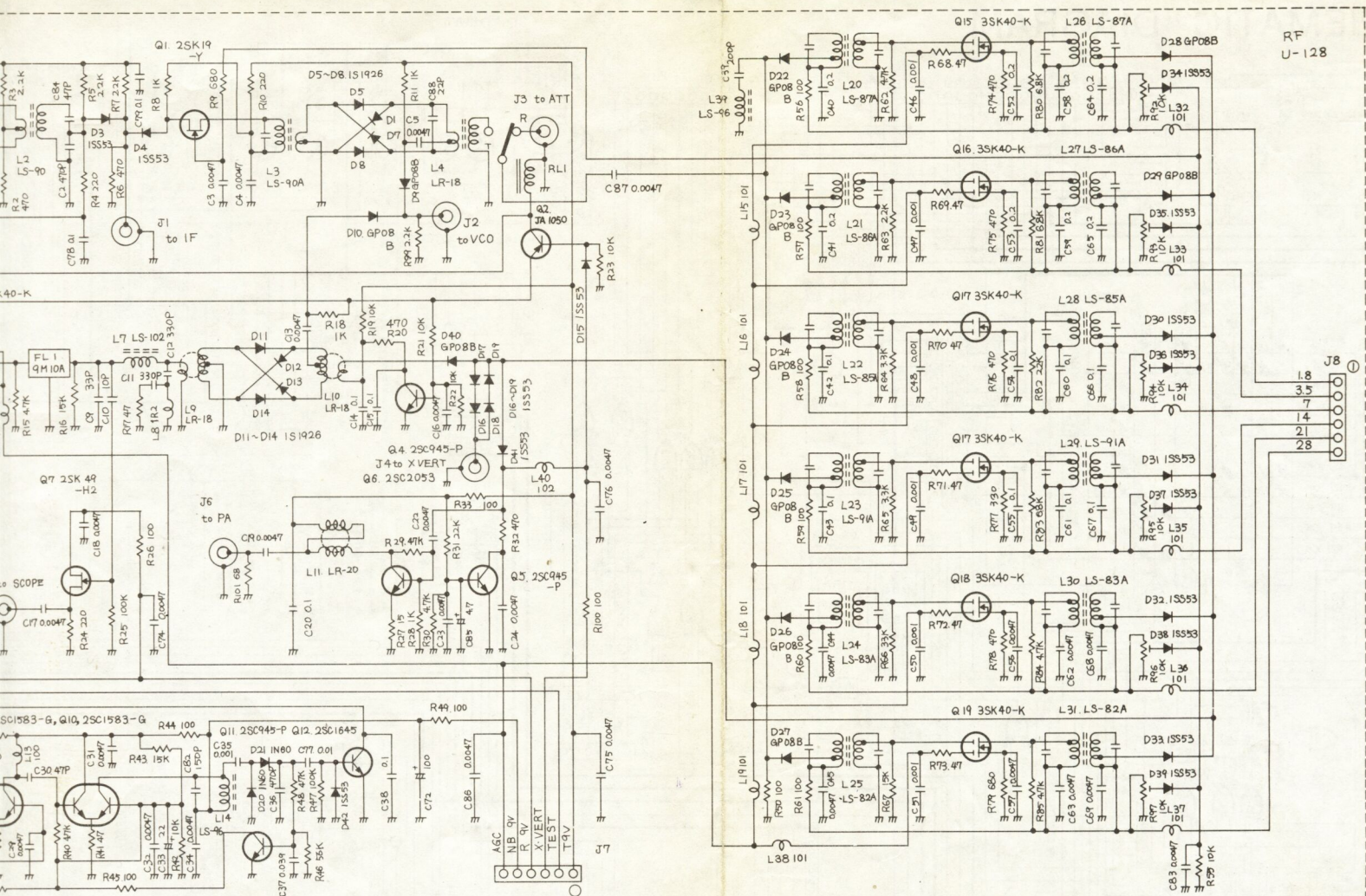
carrier signal is generated. The unwanted sideband is removed by a crystal filter, and an SSB signal of 9.0115MHz is obtained. This SSB signal is mixed with the local oscillator output from the PLL circuit, which is the same as that of the receiver section, and then amplified, filtered, and sent to the antenna.

6-1 RECEIVER

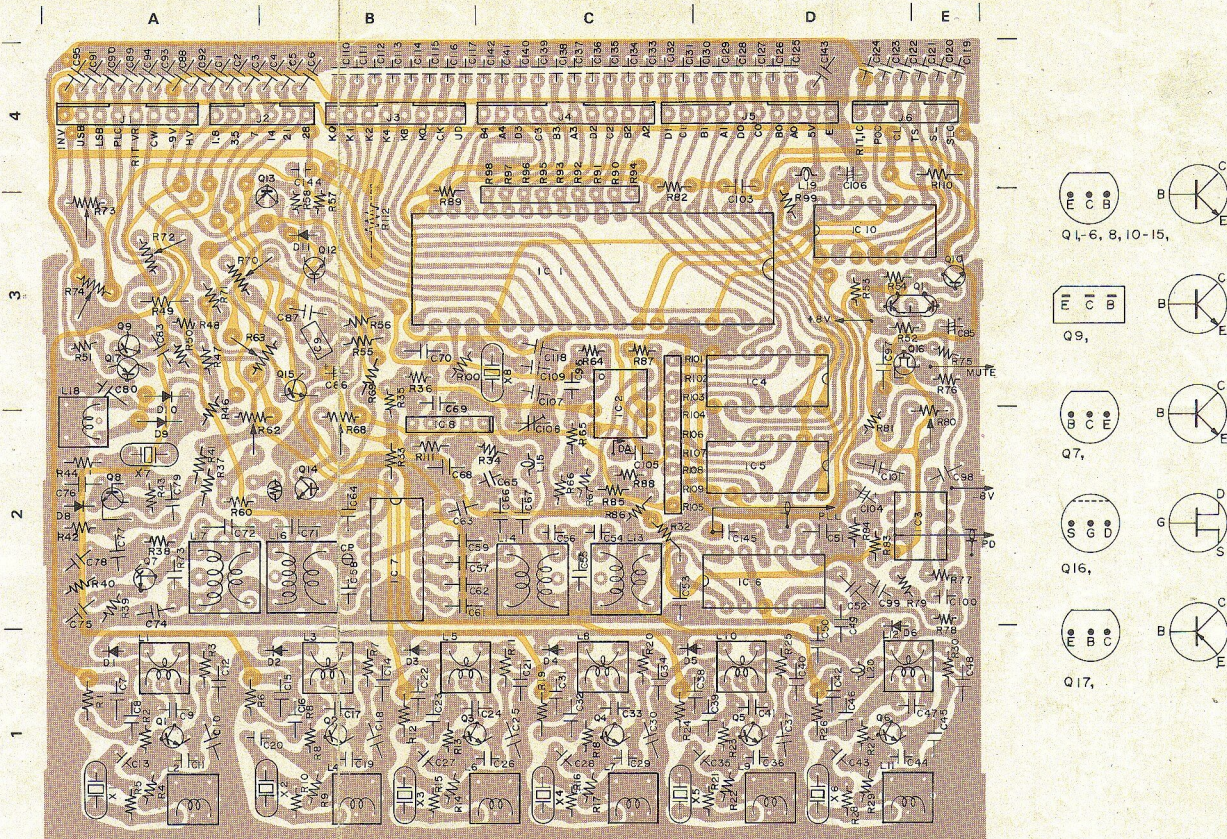
6-1-1 RF AMPLIFIER AND MIXER CIRCUIT

A signal from the antenna is passed through the ALC and filter units and applied to the antenna switching circuit located on unit "B". During reception, Q17, the antenna switching transistor, is ON, thus forward biasing D25 and D26. The incoming signal passes through these diodes, through the external receive antenna jumper, and is fed to the attenuator circuit. If the attenuator switch on the front panel is in the ON position, the signal passes through the attenuator and is attenuated 10dB. The signal is then fed to the RF unit through J3. If the attenuator switch is in the OFF position, the signal is fed directly to J3. D22 through D33 are switching diodes for the input and output signals through their respective RF circuits depending on the band selected. Q15 through Q20 are dual gate MOS FET amplifiers. The incoming signal is fed to the first

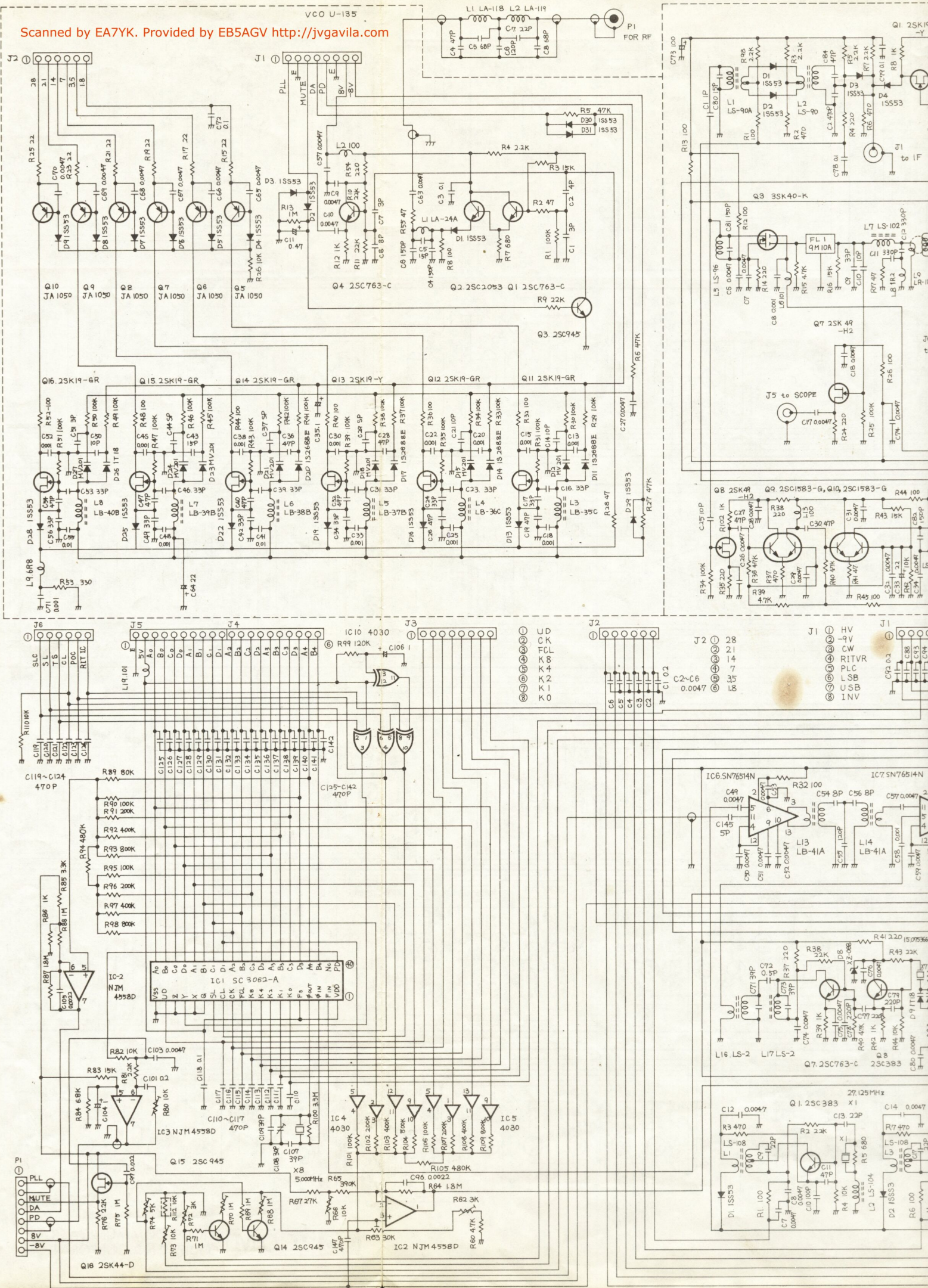




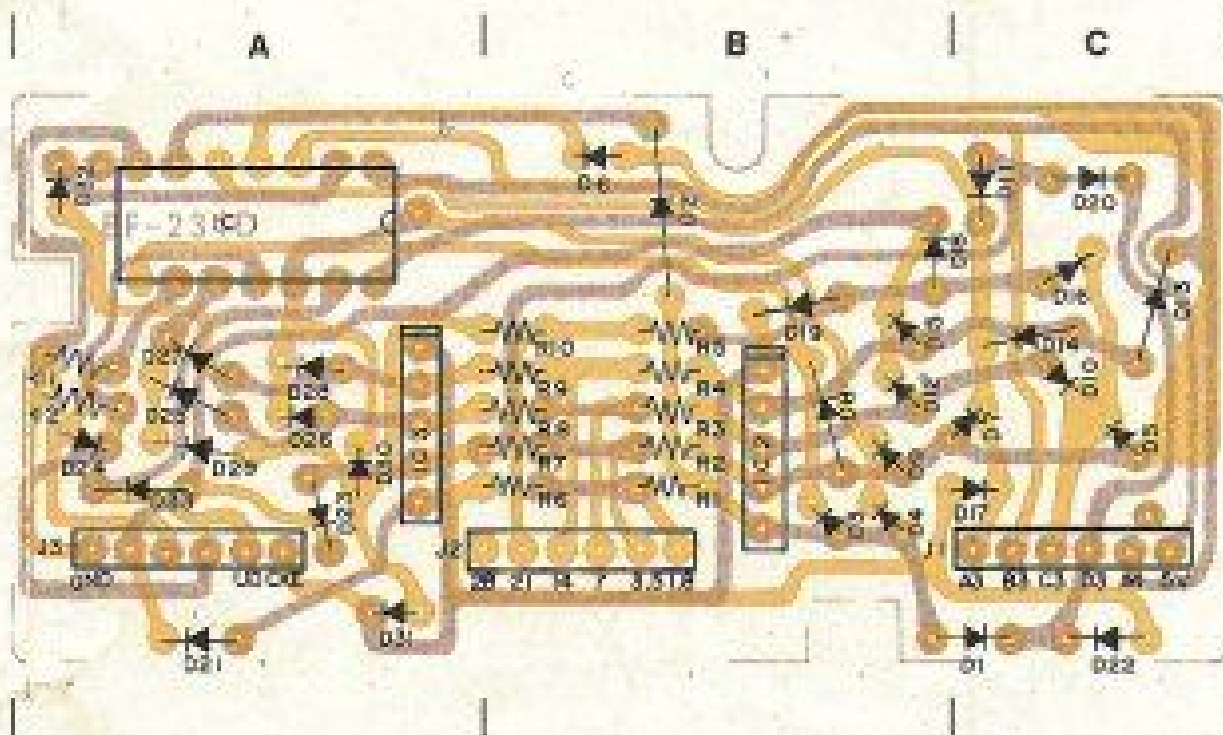
PLL UNIT



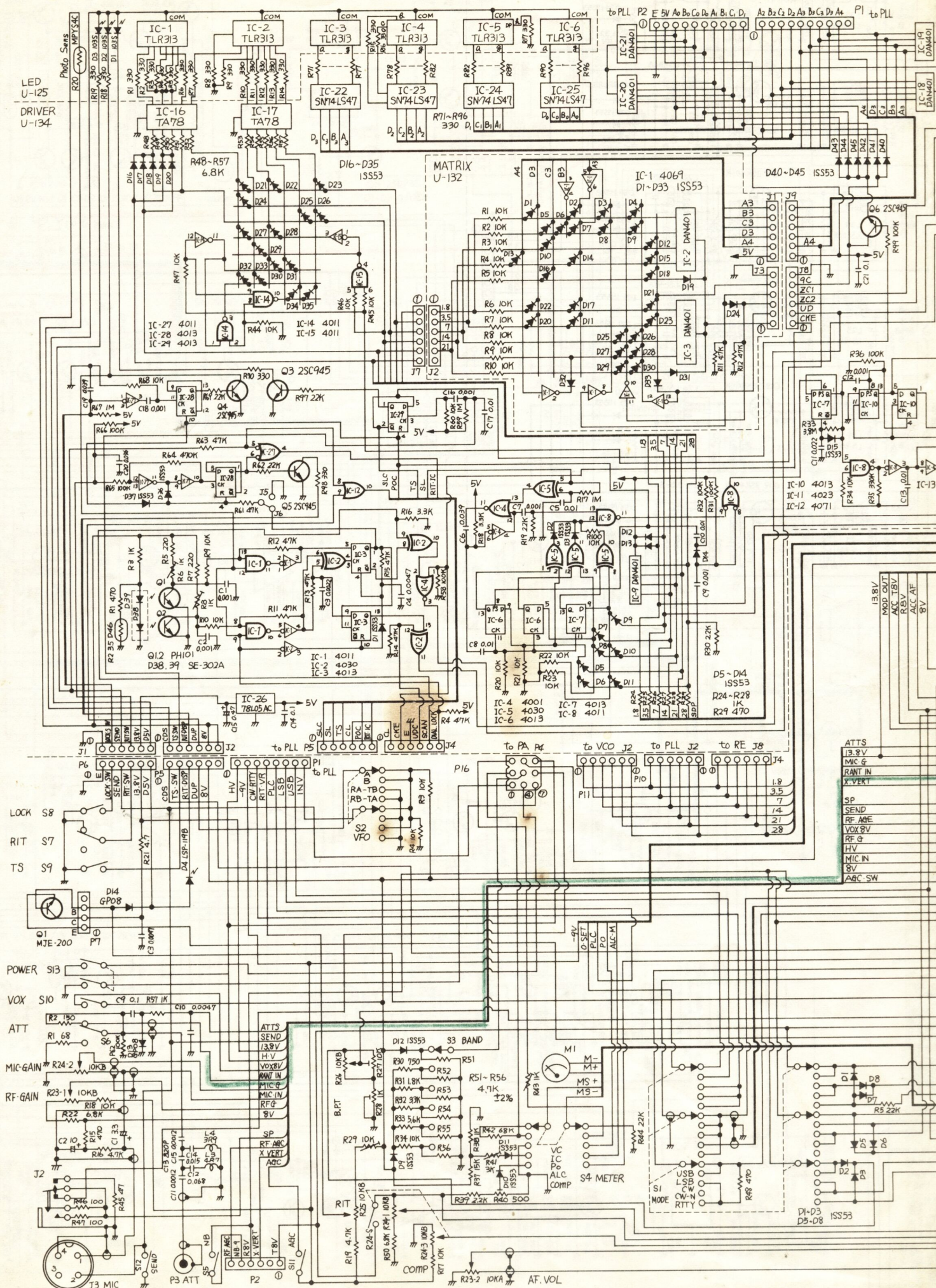
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MATRIX BOARD



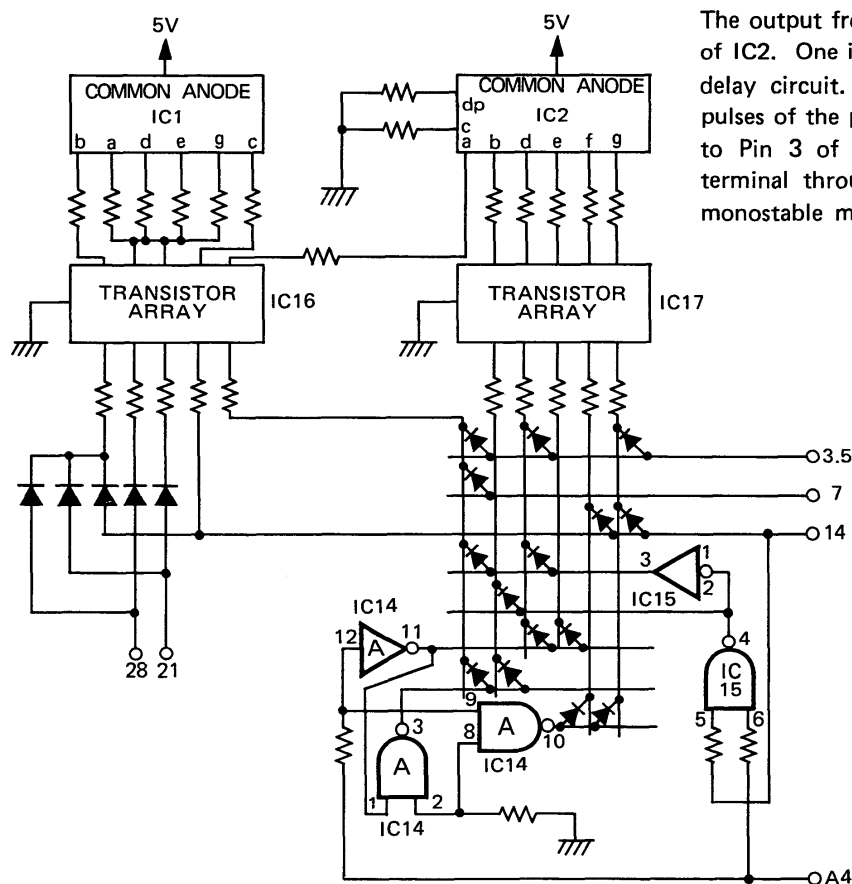
IC-701 SCHEMATIC DIAGRAM



Q9 and Q17 make up the RIT ON/OFF control circuit. The voltage of the RIT IC terminal of J6 is fed to the emitter of Q17 through R51. The terminal is 0 Volts when the RIT is ON and 5 Volts when it is OFF. Q17 prevents the reverse flow from the base of Q9. The collector of Q9 is fed voltage from the RIT control and shunt to ground when the RIT is OFF.

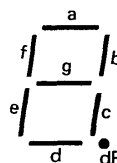
6-4-1 FREQUENCY DISPLAY

10MHz · 1MHz DIGITS DISPLAY SCHEMATIC DIAGRAM



IC14 is switched ON in 28MHz band.

BAND MHz	BAND DATA						10MHz DIGIT						1MHz DIGIT					
	3.5	7	14	21	28	A4	a	b	c	d	e	g	a	b	d	e	f	g
1.8	L	L	L	L	L	L	—	—	—	—	—	—	—	ON	—	—	—	—
3.5	H	L	L	L	L	L	—	—	—	—	—	—	ON	ON	ON	—	—	ON
7	L	H	L	L	L	L	—	—	—	—	—	—	ON	ON	—	—	—	—
14	L	L	H	L	L	L	—	ON	ON	—	—	—	—	ON	—	—	ON	ON
15	L	L	H	L	L	H	—	ON	ON	—	—	—	ON	—	ON	—	ON	ON
21	L	L	L	H	L	L	ON	ON	—	ON	ON	ON	—	ON	—	—	—	—
28	L	L	L	L	H	L	ON	ON	—	ON	ON	ON	ON	ON	ON	ON	ON	ON
29	L	L	L	L	H	H	ON	ON	—	ON	ON	ON	ON	ON	—	—	ON	ON



The segments "dp" and "c" of 1MHz digit are turned on in any band.

display. IC3-IC6 are driven by IC22-IC25. The input for the drivers is taken from the BCD output of IC1, A0-D3 in the PLL.

IC1 and IC2 are driven by IC16 and IC17. The input of each band is decoded by IC14 and IC15 and D21-D35 to indicate the MHz and 10MHz digits.

6 - 4 - 2 PHOTO-CHOPPER CIRCUIT

D38 and D39 are infrared LED diodes and Q1 and Q2 are the photo transistors. D38 sends a continuous light source to Q1 and D39 sends it to Q2. Between the diodes and the transistors is a windowed chopper disk which is connected directly to the shaft of the tuning knob. The diodes and photo transistors are set up so that the phase difference of 90 degrees results when the disc revolves. The signal from Q1 and Q2 is fed to IC1 on the driver unit. Pin 3 of IC1 is connected to the data input pin (Pin 5) of flip-flop IC3. The output from Pin 4 is divided, and fed to Pins 5 and 6 of IC2. One is fed directly and the other is fed through a delay circuit. IC2 is an exclusive OR gate IC, and both pulses of the positive edge and the negative edge are added to Pin 3 of IC3 and Q output is added to IC3's reset terminal through the delay circuit so IC3 operates as a monostable multivibrator. Q is fed to Pin 8 of IC2, the

6 - 3 PLL (Phase Locked Loop) UNIT

6 - 3 - 1 LOCAL OSCILLATOR CIRCUIT

Q1-Q6 are local oscillator circuits for the conversion type PLL. Each circuit, Q1-Q6 is functional for each band respectively; for example, Q1 is for the 1.8MHz band and Q6 is for the 28MHz band. Each oscillator circuit is basically the same, being a doubler with 3rd overtone crystals.

BAND	XTAL FREQUENCY	OUTPUT FREQUENCY
1.8MHz	27.125MHz	54.25MHz
3.5MHz	28.125MHz	56.25MHz
7 MHz	30.125MHz	60.25MHz
14 MHz	33.625MHz	67.25MHz
21 MHz	37.125MHz	74.25MHz
28 MHz	40.625MHz	81.25MHz

For example, X1 of the 1.8MHz oscillator is a 3rd overtone crystal (27.125MHz) and has L2 in series, which is for the X1 oscillating frequency adjustment. The output tuning circuit connected to the Q1 collector is tuned for 54.25 MHz, which is double the frequency of the fundamental crystal oscillator frequency. The operation of Q2-Q6 is exactly the same as that of Q1, except the output frequencies are different.

6 - 3 - 2 Vxo (Variable Frequency Crystal Oscillator) CIRCUIT

This circuit is for the oscillation, by 100Hz steps, of the lowest two digits (0.0 - 9.9KHz) of the VCO output frequency of the PLL circuit. The VXO circuit consists of

Q7, Q8, D9, X7, L18, etc. Q8 oscillates on the 15MHz range using X7, D9, D10, and L18, and the oscillating frequency is altered in 100Hz steps by the voltage supplied from the D/A (Digital to Analog) converter.

Q7 triples the output signal from Q8 and supplies about 45MHz signal to the mixer circuit of IC7.

6-3-3 MIXER AND AMPLIFIER CIRCUIT

The local oscillator output and VCO output are mixed by IC6 and the mixed signal is taken from Pins 3 and 13 of IC6. The output signal is filtered by L13 and L14, tuned for 42-44Hz, to supply the signal to IC7. The output signal of the VXO circuit is also supplied to IC7 to be mixed with the signal from IC6. The difference of these two signals (1MHz - 3MHz) is filtered by a low-pass filter and is amplified by IC8 up to the level of more than 1.6Vp-p.

6 - 3 - 4 PLL LSI CIRCUIT

The output from IC8 is the input to the LSI, Pin 2. The LSI contains PLL and control circuits. To drive the reference frequency of the PLL, a 5MHz crystal oscillator is connected to Pins 3 and 4. This frequency is divided into 1/500 by the fixed frequency divider in the LSI and becomes the accurate frequency of 10KHz. The input from Pin 2 is divided by the Programmable divider in the LSI from 1/100-1/299 which is decided by the controller, fed into the phase frequency detector with the reference frequency of 10KHz. The output is taken from Pin 40 in the form of a pulse from the phase detector according to these two input's difference of phase. The controller circuit consists of two sets of a 4-1/2 digit BCD up-down

