

# R2A20178NP

8-bit 8ch Multiplying D/A Converter with Buffer Amplifiers

R03DS0021EJ0100

Rev.1.00

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## Description

The R2A20178 is a CMOS 8-bit 8ch D/A converter having a multiplying function and output buffer amplifiers. It has a serial data input and can easily communicate with a microcontroller by simple three-wiring method (DI, CLK, LD), and it is suitable for a use in automatic adjustment applications in conjunction with a MCU. The reference voltage terminals ( $V_{DAREF1}$ ,  $V_{DAREF2}$ ) are 4ch x 2 configuration, and the 4 quadrant operation is possible.

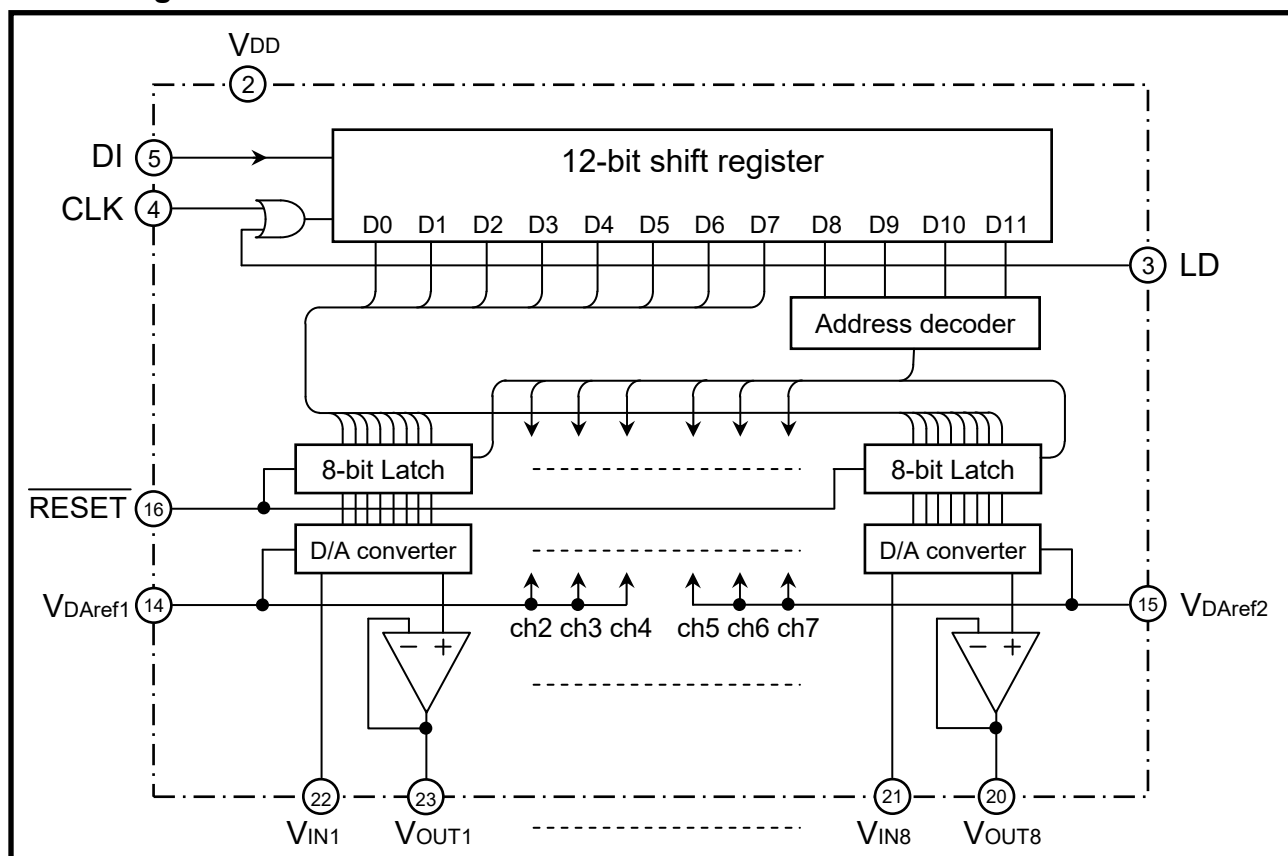
## Features

- Guarantee Nonlinearity error :  $\pm 1.0\text{LSB}$ , Differential nonlinearity error :  $\pm 0.7\text{LSB}$
- Three-wiring serial data transmission
- High performance 8ch D/A converter employing an R-2R with higher-order segment method
- 8 buffer amplifiers operating in a whole supply voltage range from  $V_{DD}$  to GND
- High anti-oscillation stability for capacitive loads
- 4 quadrant multiplication
- Very small package : QFN (pin pitch 0.5mm)

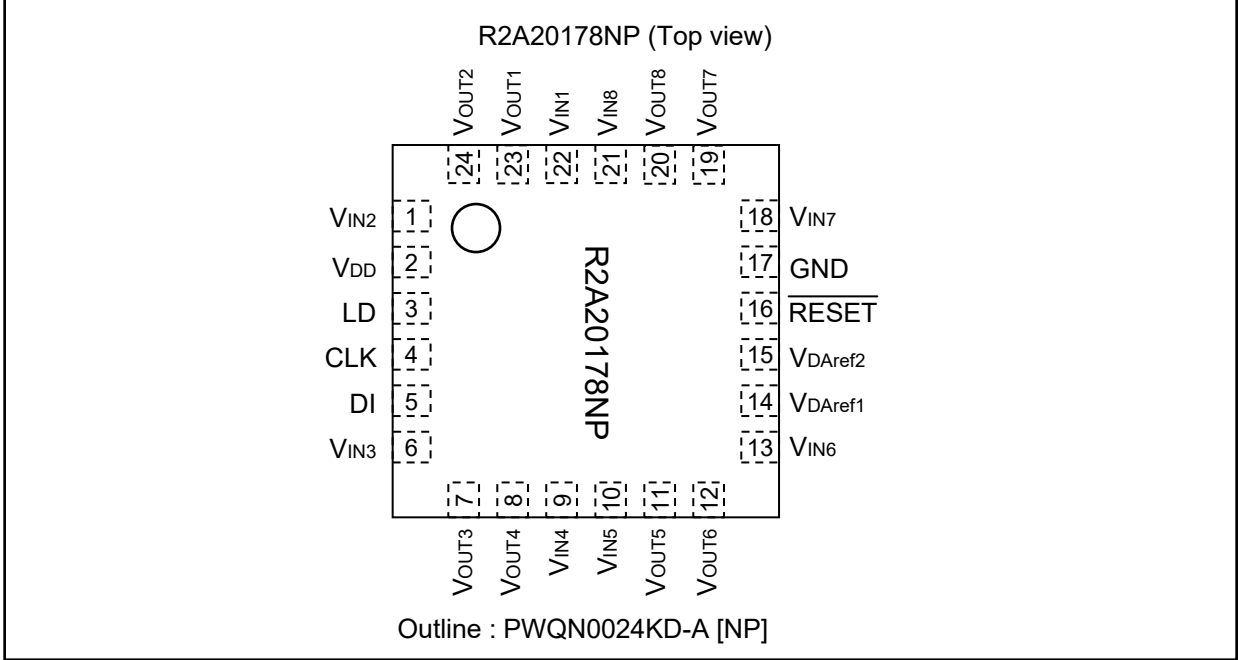
## Application

- Digital to analog conversion for consumer and industrial equipment.
- Self adjustment by combination with microcomputer and EEPROM (substitution of half fixed resistance)
- Signal gain control or automatic adjustment of LCD-TV, PDP-TV or LCD display-monitor.
- Voltage control of transmission power amplifier of transceiver

## Block Diagram



Pin Arrangement



Pin Description

Pin No.	Pin Name	Function
3	LD	A low state of LD enables data of DI loading to the 12-bit resister. During a rising edge of LD, the data in the 12-bit shift register on a rising edge of register.
4	CLK	Shift clock input. Input data of DI are taken into the 12-bit shift register on a rising edge Of the clock.
5	DI	Serial data input. The serial data length is 12-bit.
16	RESET	Reset 8-bit latches. A low state of RESET clear the all 8-bit latches.
23	VOUT1	D/A converter output with 8-bit resolution
24	VOUT2	
7	VOUT3	
8	VOUT4	
11	VOUT5	
12	VOUT6	
19	VOUT7	
20	VOUT8	
2	VDD	Power supply
17	GND	Ground
22	VIN1	D/A converter input
1	VIN2	
6	VIN3	
9	VIN4	
10	VIN5	
13	VIN6	
18	VIN7	
21	VIN8	
14	VDAref1	D/A converter reference voltage input (ch1 to ch4). $V_{OUT} = (V_{IN} - V_{DAref}) \times n/256 + V_{DAref1}$
15	VDAref2	D/A converter reference voltage input (ch5 to ch8). $V_{OUT} = (V_{IN} - V_{DAref}) \times n/256 + V_{DAref2}$

**Absolute Maximum Ratings**

(Ta = +25deg unless otherwise noted)

Item	Symbol	Conditions	Ratings	Unit
Supply voltage (for digital)	V <sub>DD</sub>		-0.3 to +6.5	V
Digital input voltage	V <sub>IND</sub>		-0.3 to +6.5	V
Analog input voltage	V <sub>IN</sub>		-0.3 to V <sub>DD</sub> +0.3 <+6.5	V
Analog output voltage	V <sub>OUT</sub>		-0.3 to V <sub>DD</sub> +0.3 <+6.5	V
D/A reference voltage	V <sub>DAref</sub>		-0.3 to V <sub>DD</sub> +0.3 <+6.5	V
Power dissipation	P <sub>d</sub>	Ta = +85deg	300	mW
Thermal derating	K theta	Ta > +25deg	7.5	mW/deg
Operating temperature	T <sub>opr</sub>		-30 to +85	deg
Storage temperature	T <sub>stg</sub>		-40 to +125	deg

**Electrical Characteristics**

&lt; Analog/Digital Common Part &gt;

(V<sub>DD</sub>, V<sub>IN</sub> = +5V +/-10%, V<sub>DD</sub>>V<sub>IN</sub>, GND=V<sub>DAref1</sub>=V<sub>DAref2</sub> = 0V, Ta = -30 to +85deg, unless otherwise noted.)

Item	Symbol	Conditions	Limits			Unit
			Min	Typ	Max	
Supply voltage	V <sub>DD</sub>		2.7	5.0	5.5	V
Supply current	I <sub>DD</sub>	CLK = 1MHz, V <sub>DD</sub> = 5V, I <sub>AO</sub> = 0μA	-	-	2.0	mA

&lt; Digital Part &gt;

(V<sub>DD</sub>, V<sub>IN</sub> = +5V +/-10%, V<sub>DD</sub>>V<sub>IN</sub>, GND=V<sub>DAref1</sub>=V<sub>DAref2</sub> = 0V, Ta = -30 to +85deg, unless otherwise noted.)

Item	Symbol	Conditions	Limits			Unit
			Min	Typ	Max	
Input leak current	I <sub>ILK</sub>	V <sub>IN</sub> = 0 to V <sub>DD</sub>	-10	-	10	μA
Digital input "Low" voltage	V <sub>IL</sub>		-	-	0.2 V <sub>DD</sub>	V
Digital input "High" voltage	V <sub>IH</sub>		0.8 V <sub>DD</sub>	-	-	V

&lt; Analog Part &gt;

(V<sub>DD</sub>, V<sub>IN</sub> = +5V +/-10%, V<sub>DD</sub>>V<sub>IN</sub>, GND=V<sub>DAref1</sub>=V<sub>DAref2</sub> = 0V, Ta = -30 to +85deg, unless otherwise noted.)

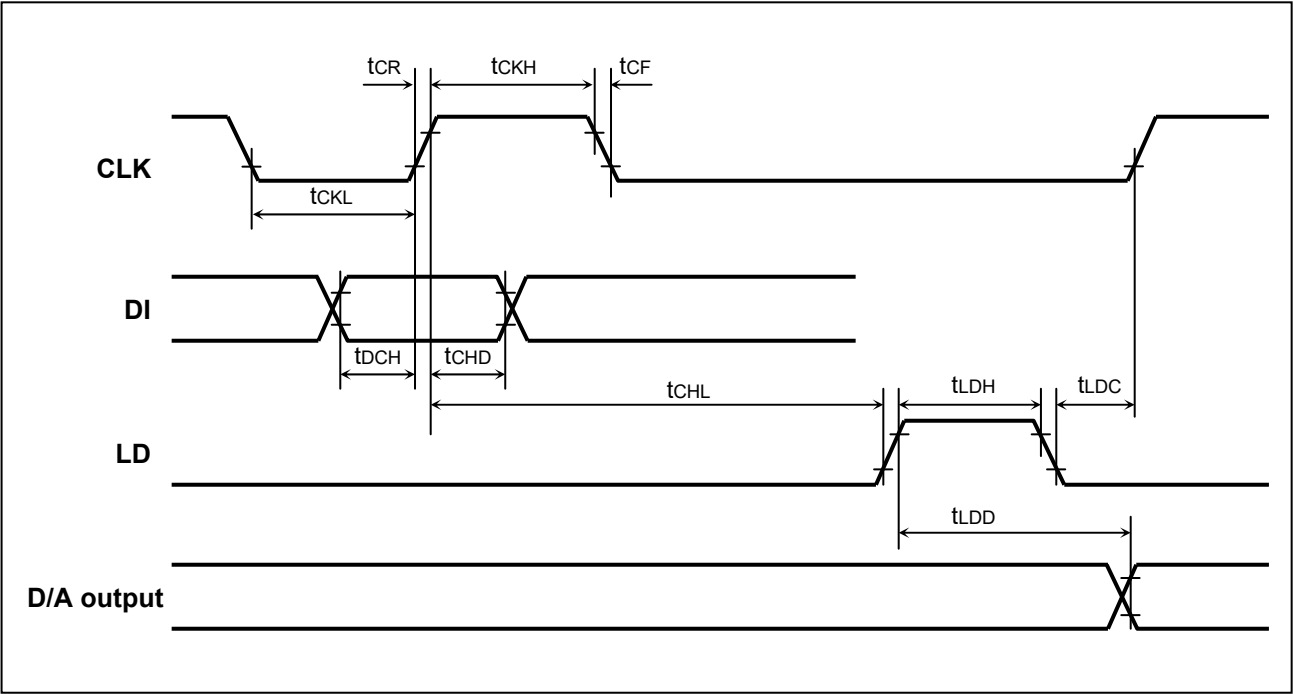
Item	Symbol	Conditions	Limits			Unit
			Min	Typ	Max	
Input current	I <sub>IN</sub>	V <sub>IN</sub> = 5V, V <sub>DAref</sub> = 0 V, Proportional to Max. input current condition (V <sub>IN</sub> - V <sub>DAref</sub> ) and digital data of each channels	-	-	0.3	mA
D/A reference input current	I <sub>DAref</sub>	V <sub>IN1</sub> to V <sub>IN8</sub> = 5V, V <sub>DAref</sub> = 0 V, Proportional to Max. input current condition (V <sub>IN</sub> - V <sub>DAref</sub> ) and digital data of each channels	-2.4	-	-	mA
Resolution	RES		-	8	-	bit
Differential nonlinearity	DNL	V <sub>DAref1</sub> = V <sub>DAref2</sub> = 0.05V,	-0.7	-	0.7	LSB
nonlinearity	NL	Without load ( I <sub>VOUT</sub> = 0μA )	-1	-	1	LSB
Buffer amplifier output voltage range	V <sub>AO</sub>	I <sub>AO</sub> = +/-100 μA	0.1	-	V <sub>CC</sub> - 0.1	V
		I <sub>AO</sub> = +/-500 μA	0.2	-	V <sub>CC</sub> - 0.2	
Buffer amplifier output current range	I <sub>AO</sub>	Upper saturation voltage = 0.4V, Lower saturation voltage = 0.4V	-1	-	1	mA
Output capacitive load	C <sub>O</sub>		-	-	0.1	μF
Buffer amplifier output impedance	R <sub>O</sub>		-	5	-	ohm

AC Characteristics

(V<sub>DD</sub>, V<sub>IN</sub> = +5V +/-10%, V<sub>DD</sub>>V<sub>IN</sub>, GND=V<sub>D</sub>Aref1=V<sub>D</sub>Aref2 = 0V, Ta = -30 to +85deg, unless otherwise noted.)

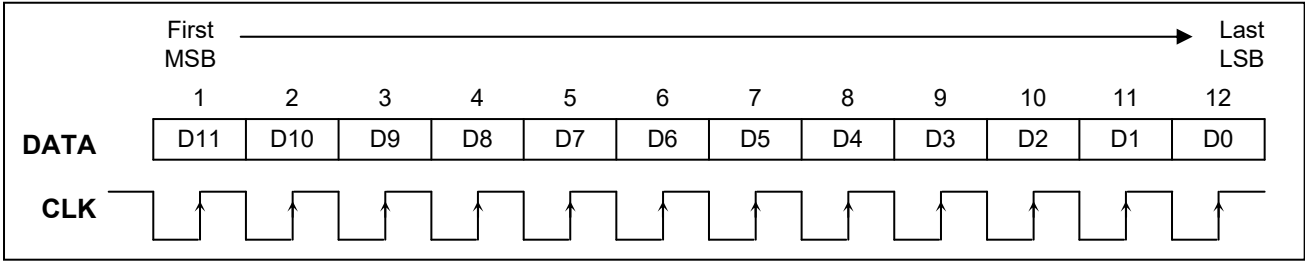
Item	Symbol	Conditions	Limits			Unit
			Min	Typ	Max	
Clock “L” pulse width	t <sub>CKL</sub>		200	-	-	ns
Clock “H” pulse width	t <sub>CKH</sub>		200	-	-	ns
Clock rise time	t <sub>CR</sub>		-	-	200	ns
Clock fall time	t <sub>CF</sub>		-	-	200	ns
Data setup time	t <sub>DCH</sub>		60	-	-	ns
Data hold time	t <sub>CHD</sub>		100	-	-	ns
LD setup time	t <sub>CHL</sub>		200	-	-	ns
LD hold time	t <sub>LDC</sub>		100	-	-	ns
LD “H” pulse duration time	t <sub>LDH</sub>		100	-	-	ns
D/A output settling time	t <sub>LDD</sub>	C <sub>L</sub> <100pF, V <sub>OUT</sub> : 0.5↔4.5V, Time until the output becomes the final value of 1/2 LSB	-	-	300	μs
RESET “Low” level minimum pulse width	t <sub>RL</sub>		200	-	-	ns

Timing Chart



Digital Data Format

12-bit serial data



Data Assignment

D8	D9	D10	D11	: DAC select data				
D0	D1	D2	D3	D4	D5	D6	D7	: DAC data

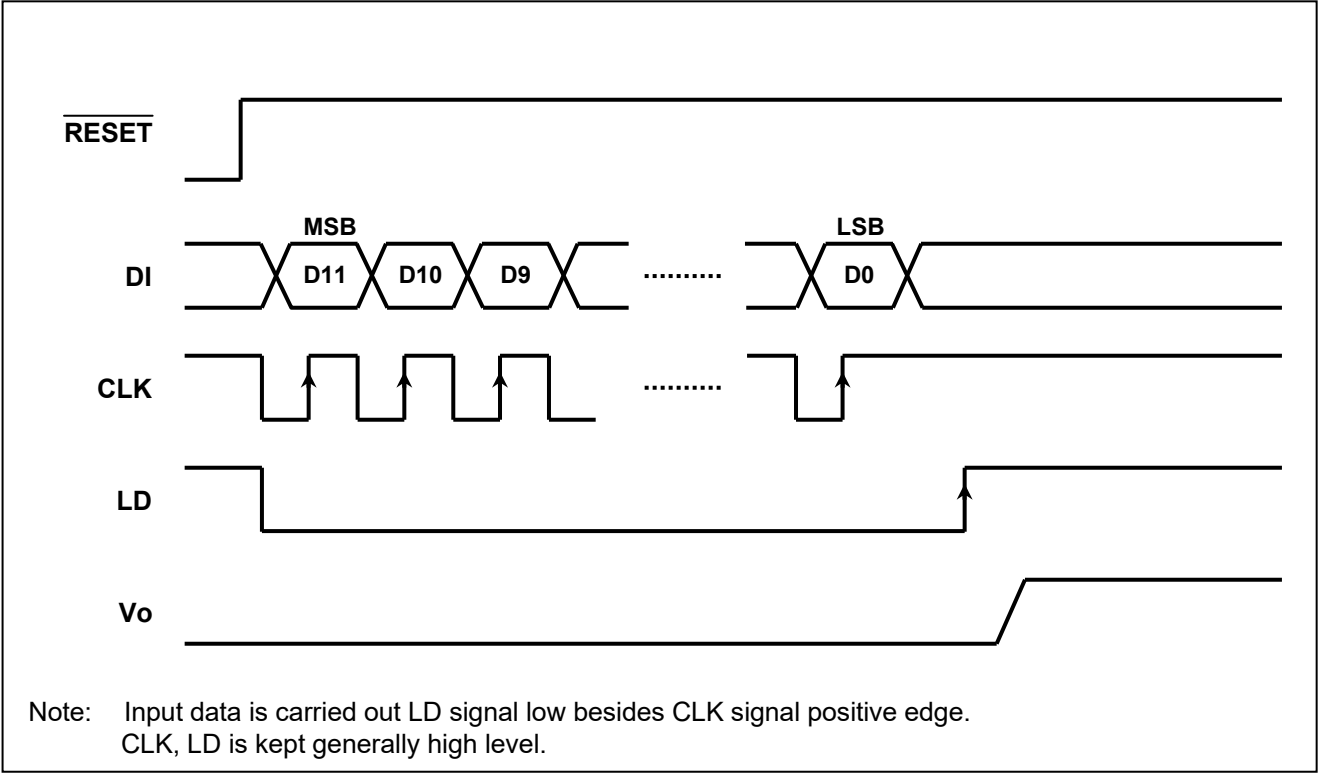
DAC select data

D8	D9	D10	D11	DAC Selection
0	0	0	0	Don't care
0	0	0	1	V <sub>OUT1</sub> selection
0	0	1	0	V <sub>OUT2</sub> selection
0	0	1	1	V <sub>OUT3</sub> selection
0	1	0	0	V <sub>OUT4</sub> selection
0	1	0	1	V <sub>OUT5</sub> selection
0	1	1	0	V <sub>OUT6</sub> selection
0	1	1	1	V <sub>OUT7</sub> selection
1	0	0	0	V <sub>OUT8</sub> selection
1	0	0	1	Don't care
1	0	1	0	Don't care
1	0	1	1	Don't care
1	1	0	0	Don't care
1	1	0	1	Don't care
1	1	1	0	Don't care
1	1	1	1	Don't care

DAC data

D0	D1	D2	D3	D4	D5	D6	D7	DAC Output
0	0	0	0	0	0	0	0	V <sub>DAref</sub>
1	0	0	0	0	0	0	0	( V <sub>IN</sub> – V <sub>DAref</sub> ) / 256 x 1+ V <sub>DAref</sub>
0	1	0	0	0	0	0	0	( V <sub>IN</sub> – V <sub>DAref</sub> ) / 256 x 2 + V <sub>DAref</sub>
1	1	0	0	0	0	0	0	( V <sub>IN</sub> – V <sub>DAref</sub> ) / 256 x 3 + V <sub>DAref</sub>
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	( V <sub>IN</sub> – V <sub>DAref</sub> ) / 256 x 255 + V <sub>DAref</sub>

Timing Chart ( Model )

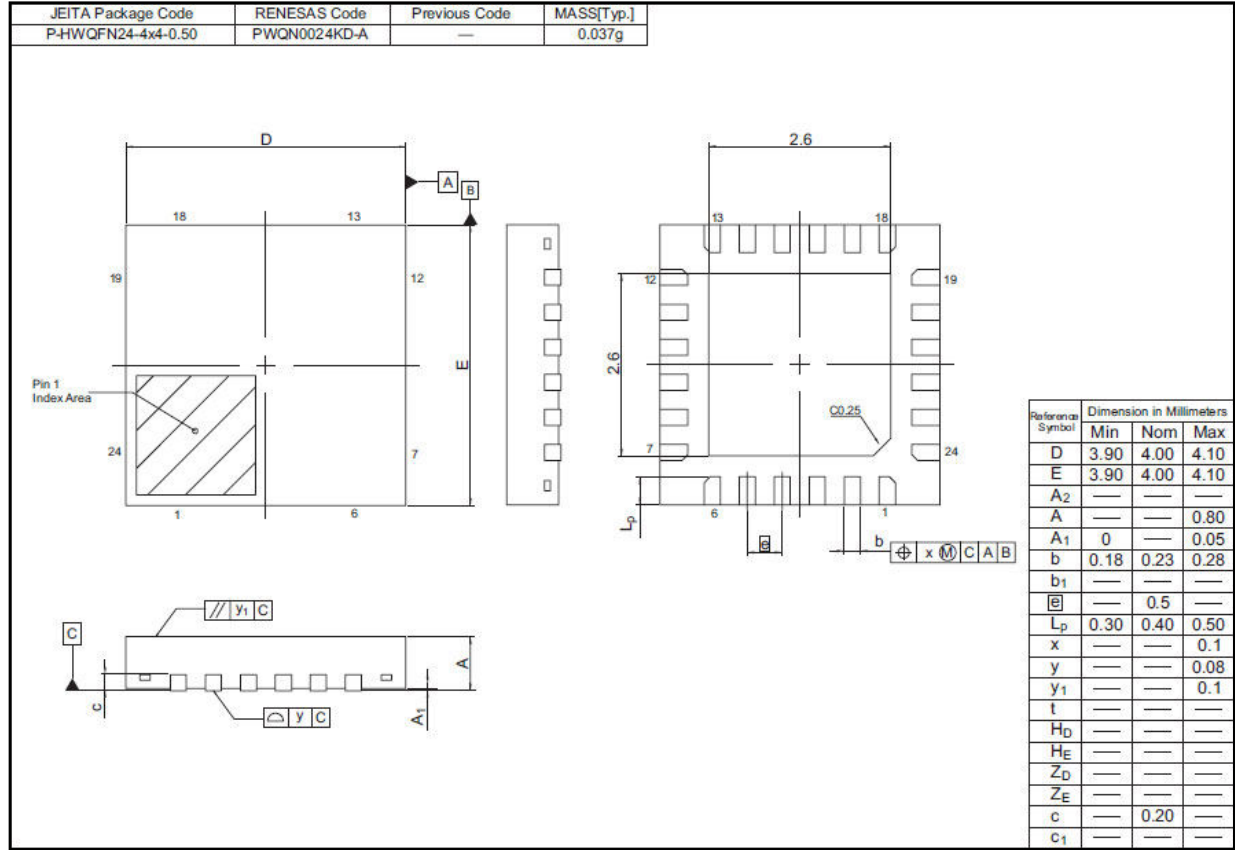


Ordering Information

Order part No.	Package Name	Package Code	Package type No.	Packing/Quantity
R2A20178NP	QFN-24	PWQN0024KD-A	NP	Embossed Taping/2,500 pcs.

Package Dimensions

PWQN0024KD-A



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