TECHNICAL MANUAL

OPERATION, MAINTENANCE, INSTALLATION INSTRUCTIONS AND ILLUSTRATED PARTS BREAKDOWN

HF DSP RECEIVER
MODEL RX-330A

TEN-TEC, INC.
1185 DOLLY PARTON PARKWAY
SEVIERVILLE, TN 37862

THIS MANUAL WAS PREPARED IN ACCORDANCE WITH MIL-M-7298C

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RECORD OF CHANGES

CHANGE NO.	DATE	TITLE OR BRIEF DESCRIPTION	ENTERED BY

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WARNING

HIGH VOLTAGE

is used in the operation of this equipment.

DEATH ON CONTACT

may result if personnel fail to observe safety precautions.
Learn the areas containing high voltage within the equipment.
Be careful not to contact high voltage connections when installing,
operating or maintaining this equipment.
Before working inside the equipment, turn power off
and ground points of high potential before touching them.

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INTRODUCTION

This technical manual provides operation and maintenance instructions for the RX-330A HF DSP Receiver. The manual was prepared in accordance with MIL-M-7298C, "Manuals, Technical: Commercial Equipment". This manual is organized into nine chapters along with a Table of Contents and lists of tables and illustrations.

Chapter 1 presents general information about the Receiver, which includes functional capabilities, performance specifications, and physical dimensions. Chapter 2 provides information concerning the unpacking and initial installation of the receiver. A general theory of operation is provided in Chapter 3 which describes the functioning of the Receiver's individual circuit boards. Chapter 4 contains information on operation of the multi-drop RS 232 Interface and the parallel data output.

Chapter 5 provides information on maintenance and troubleshooting measures to be employed at the user's level. Instructions pertaining to the reshipment or long term storage are provided in Chapter 6. A detailed list of unique single source parts is provided in Chapter 7. In addition, Chapter 7 contains a list of manufacturers for these parts and their addresses. Chapter 8 provides a listing of replaceable modules and parts. Chapter 9 contains detailed parts lists for each of the replaceable modules. Chapter 9 also contains schematic diagrams for the electronic circuits.

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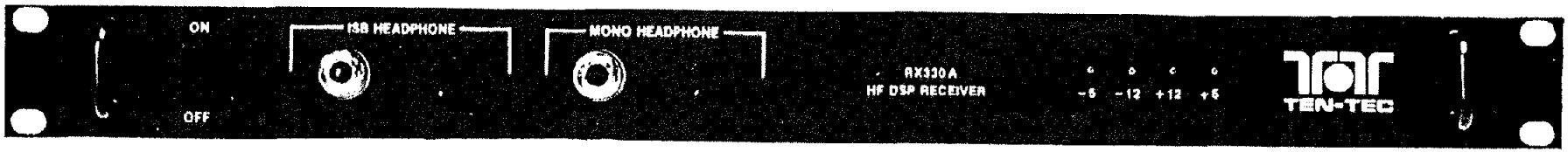

FIGURE I. RX-330A FRONT VIEW

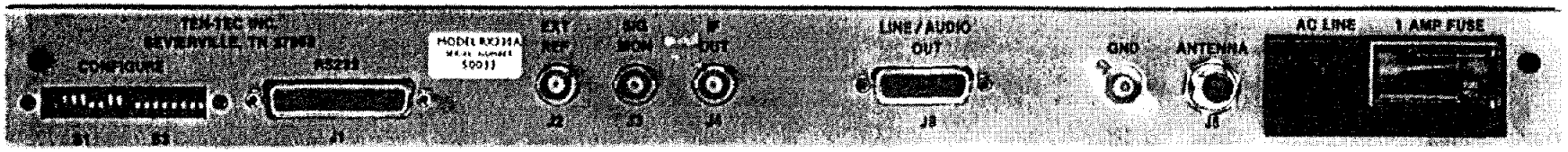

FIGURE II. RX-330A REAR VIEW

CHAPTER 1

GENERAL INFORMATION

1-1 PURPOSE AND FUNCTION: The TEN-TEC RX-330A is a remotely controlled Monitor Receiver capable of tuning the .5 to 30 MHz HF range in 1 Hz steps. The Control Interface is Multi-drop RS-232, allowing multiple receivers to be addressed on one RS-232 line. Available detection modes are: USB, LSB, ISB, CW, AM, Synchronous AM, and FM. IF Bandwidth is selectable in 57 steps from 100 Hz to 16 KHz. Manual (MAGC) and automatic (AGC) gain control modes are selectable. In CW mode, the adjustable BFO has a range of ± 8000 Hz. In CW, LSB and USB modes, a passband tuning function allows simultaneous adjustment of BFO and receiver tuning over a ± 2000 Hz range. Three Audio and two IF outputs are provided.

1-2 SPECIFICATIONS

Power Supply:

Internal, accepts 48-440 Hz line power, 120/240 VAC, rear panel selectable. 30 watts nominal.

Frequency tuning system:

Tuning Range: 500 KHz to 30 MHz. Tunable to 0 MHz with degraded performance.

Tuning Increment: 1 Hz minimum.

Synthesizer lock time: 10 mS nominal.

BFO: Tunable in CW mode only, ± 8 KHz, 10 Hz steps. Fixed frequency in SSB and ISB modes, disabled in AM and FM modes.

Accuracy: All internal oscillators can be locked to either internal or external frequency standards. The internal reference is adjustable by a continuously variable trimmer to allow calibration to any desired accuracy.

Stability (internal standard): ± 1 ppm per degree C within the operating range of 0 to 50 degrees C. An optional TCVCXO provides ± 1 ppm over entire range (0 to 50 degrees C).

External Frequency Standard: 1, 2, 5, or 10 MHz ± 1 ppm, 200 mV p-p, high impedance load. The receiver automatically detects and uses the external standard upon application, at power-up, or after any serial link activity. If the external standard input slews far outside the ± 1 ppm specified, the internal circuitry will lose lock until the input returns to within spec, or will re-lock at the next power-up or serial activity if the input is within specification at a valid reference frequency (1, 2, 5, or 10 MHz). A frequency-out-of-lock condition is always reported over the serial link. Removal of the external frequency standard input immediately returns the receiver to the internal standard.

Tuning Method: Remote control via multi-drop RS-232.

Frequency Indication: None visible. Frequency status reported by the RS-232 serial link.

Interface connections:

RF Input:

Impedance:	50 Ohms, nominal.
VSWR:	2.5 : 1 maximum in preselector passband.
Connector:	rear panel BNC.
Protection:	internal surge protector.

Audio Outputs:

Two 600 Ohm lines

Level:	0 dBm nominal, center-tapped, ungrounded.
Connector:	3 pins of rear panel DA-15 connector, each line.
Function:	Upper and lower sideband audio on separate lines in ISB mode. Same signal on both lines in other modes.

Stereo Headphone:

Level:	10 mW maximum into 600 Ohm load. Front panel volume control.
Connector:	Front panel 1/4" stereo phone jack.
Function:	Upper and lower sidebands in ISB mode. Monaural output in other modes.

Single-ended Audio:

Level:	10 mW maximum into 600 Ohm load.

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Connector: 2 pins of rear panel DA-15 connector, one grounded
Function: Upper, lower, or both sidebands in ISB mode, software configured.

Mono Headphone:
Level: 10 mW maximum into 600 Ohm load. Front panel volume control.
Connector: Front panel 1/4" mono phone jack.
Function: Upper, lower, or both sidebands in ISB mode, software configured.

Signal Monitor:
Frequency: 455 KHz center.
Bandwidth: 16 KHz (-6 dB).
Level: -10 dBm nominal. AGC delayed 40 dB.
Impedance: 50 ohms nominal.
Connector: Rear panel BNC.

IF Output:
Frequency: 455 kHz center.
Bandwidth: Determined by IF filter selection.
Level: -10 dBm nominal (AGC leveled).
Impedance: 50 ohms nominal.
Connector: Rear panel BNC.

Sensitivity:

Noise Figure: 10 dB typical, 14 dB maximum - preamp on.
18 dB typical, 20 dB maximum - preamp off.

Spurious Responses: All spurious less than -19 dBm equivalent input - preamp on.

Control Interface:
Standard: Multi-drop RS-232.
Config: Dipswitch programmable, 300 to 19200 baud, 7 or 8 data bits, even, odd, or no parity.
Connector: DB-25 female.

Gain Characteristics:

Gain control:
The receiver can operate in automatic (AGC) or manual (MAGC) gain control modes. Manual gain control reduces receiver gain and increases the AGC threshold by up to 120 dB.

AGC:
Range: 90 dB minimum
Threshold: 3 uV typical
Attack Time: 15 mS typical
Release Time:
Fast 25 mS
Medium .5 second
Slow 4 seconds

MAGC:
Range: 120 dB. Controlled through the RS-232 interface.
Attack/Release Times: Limited only by RS-232 serial transfer rate.

Sensitivities by mode:

	BW	SINAD	PREAMP OFF TYP	PREAMP OFF MAX	PREAMP ON TYP	PREAMP ON MIN/MAX
AM: (50% Mod @ 400 Hz)	6 kHz	10 dB	-100 dBm 2.25 uV	-98 dBm/ 2.8 uV	-112dBm/ 0.56 uV	-108dBm/ 0.9 uV
FM: (6 kHz dev @ 1 kHz)	16 kHz	16 dB	-99 dBm/ 2.5 uV	-97 dBm/ 3.2 uV	-108dBm/ 0.9 uV	-104dBm/ 1.4 uV
USB/LSB/ISB:	3.2 kHz	10 dB	-109 dBm/ 0.8 uV	-107 dBm/ 1.0 uV	-119dBm/ 0.25 uV	-115dBm/ 0.4 uV
CW:	300 Hz	16 dB	-113 dBm/ 0.5 uV	-111 dBm/ 0.63 uV	-124dBm/ 0.14 uV	-120dBm/ 0.22 uV

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Signal handling characteristics: - preamp off

Image Rejection: 90 dB typical, 70 dB minimum (all mixers).

IF Rejection: 90 dB typical, 80 dB minimum (all IFs).

Third order intercept point: 30 dBm typical, 25 dBm minimum.

Second order intercept point: +75 dBm, typ, 60 min.

Selectivity: 57 bandwidths selectable from 0.1 to 16 kHz. Shape factor better than 1.5:1 (6 to 60 dB): 100, 120, 150, 170, 200, 220, 250, 300, 350, 400, 450, 500, 600, 700, 800, 900 Hz, 1, 1.1, 1.2, 1.3,1.4, 1.5, 1.6, 1.7, 1.8, 1.9, 2.0, 2.2, 2.4, 2.6, 2.8, 3.0, 3.2, 3.4, 3.6, 3.8, 4.0, 4.4, 4.8, 5.2, 5.6, 6.0, 6.4, 6.8, 7.2, 7.6, 8.0, 8.8, 9.6, 10.4, 11.2, 12.0, 12.8, 13.6, 14.4, 15.2, 16.0 KHz. The receiver automatically selects the best match greater than or equal to the requested bandwidth.

Blocking on tune: <5% THD: 0dBm input 30% AM 1 KHz

Blocking off tune: 200 KHz offset. 15dBm typ. 10 dBm min for 3 dB desense

Ultimate Rejection: Greater than 70 dB regardless of filter selected.

Group Delay: No more than .1 ms variation over entire passband.

Lo Phase noise: -120 dBc/Hz @ 20 KHz offset, typ. -110 dBc/Hz max.

1-3 ENVIRONMENTAL CONDITIONS

Normal Operating:

Temperature: 0 to 50 deg C (32-122F)
Humidity: Up to 95% Rel, non-cond.
Altitude: Up to 10,000 feet MSL
Shock: Not applicable
Vibration: Not applicable

Storage/Transport:

Temperature: -46 to 71 deg C (-50-160F)
Humidity: Up to 95% Rel, non-cond.
Altitude: Up to 15,000 feet MSL
Shock: 10 G, 11 mS duration
Vibration: 1-1/2 G, 5 to 200 Hz

1-4 MECHANICAL

Size: 1.75H x 19W x 21.31D inches
44.45H x 482.6W x 541.4D mm

Weight: 12.2 lbs. (5.53 kg)

Cooling: Air convection cooled within fan ventilated rack cabinet. Units are directly stackable with no fillers required between chassis.

Mounting: Model RX-330A conforms to EIA standard 19 inch rack mount panel space and is 1 U (1.75) high. Slide mechanism attachment points (10-32 thread) are compatible with Jonathan slide type 375 QD.

Cable connectors Rear panel:

Receiver RF input: BNC female
IF output 455 kHz: BNC female
Signal Monitor: BNC female
External Reference: BNC female
Remote Control: (Multi-drop RS-232) DB 25, female
Main Power: Detachable 3 conductor ac cord
Line Audio: 15 pin D connector, female

Front Panel:

Mono headphone: 1/4" mono jack
Stereo headphone: 1/4" stereo jack

1-5 EQUIPMENT/PARTS SUPPLIED

1 HF DSP RECEIVER MODEL RX-330A
1 AC POWER CORD
1 FUSE - 1A SLO-BLOW MDL 1
1 TECHNICAL MANUAL

Specifications subject to change without notice.

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CHAPTER 2

PREPARATION FOR USE AND INSTALLATION

2-1 UNPACKING AND INSPECTION: Examine the shipping carton for damage before unpacking the unit. If the carton is damaged, open the carton in the presence of an agent of the shipping carrier if possible. If the carton is not damaged, retain the carton and packing materials for inspection if damage is found after the unit is unpacked.

Open the carton and remove the foam packing materials on top of the unit. Lift the unit free of the carton. No packing materials are required or provided inside the unit. Replace the foam packing material in the carton. The carton may be saved for possible reshipment if required.

Upon unpacking, inspect the unit for obvious external damage. Pay particular attention to dents or bent sheet metal. If damage is evident, remove the top cover of the unit and inspect for further damage such as damaged circuit boards. Do not attempt to operate the unit if such damage is noted until further checks are made.

2-2 MOUNTING: RX-330A is designed for EIA standard 19 inch panel space rack. Slide mechanism attachment points (10-32 thread) are compatible with Jonathan slide type 375QD.

2-3 POWER: The RX-330A is designed to operate from either 120 or 240 VAC. A small pc board located in the power entry module can be removed and reinserted to select proper ac voltage.

2-4 ANTENNA: Connect the antenna to the BNC connector on the RX-330A labeled antenna (shown in Figure II).

2-5 IF OUT: A 455 KHz signal with bandwidth dependent on filter selected (shown in Figure II).

2-6 SIG MON: A 455 KHz signal with a fixed bandwidth of 16 KHz (shown in Figure II).

2-7 EXT REF: Automatically turns off the internal 10 MHz reference if a 1 MHz, 2 MHz, 5 MHz or 10 MHz 200 mV p-p signal is applied (shown in Figure II).

2-8 RS-232: The RS-232 will accept a standard DB-25 connector (shown in Figure II).

2-9 LINE A: Provides a 600 Ω balanced center tapped output (shown in Figure II).

2-10 LINE B: Provides a 600 Ω balanced center tapped output (shown in Figure II).

2-11 AUDIO: Provides a 600 Ω unbalanced output (shown in Figure II).

2-12 MONO HEADPHONE: Provides a 600 Ω unbalanced output controlled by a front panel volume control (shown in Figure I).

2-13 ISB HEADPHONE: Provides both sidebands controlled by front panel volume control (shown in Figure I).

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CHAPTER 3

GENERAL THEORY OF OPERATION

3-1 INTRODUCTION: The TEN-TEC Model RX-330A receiver combines a high dynamic range front end with a versatile DSP back end to provide extraordinary performance and flexibility. Refer to the overall block diagram Figure 9-1 and interconnect diagram Figure 3-2.

The RF signals applied to the receiver Antenna Input (J5) are bandpass filtered in one of eight bands of approximately one-half octave bandwidth. Balanced amplifiers and high level first mixer stages preserve the second and third order intercept points during conversion to the first IF of approximately 45.105 MHz. Two 2-pole crystal filters provide first IF selectivity to reject 1st mixer spurious products and the 2nd mixer image (at -910 KHz).

After conversion to the second IF of approximately 455 KHz in the second mixer stage, the signal is bandpass filtered to 16 KHz bandwidth and applied to an AGC'd 2nd IF amplifier with up to 80 dB gain. After post-filtering (again 16 KHz bandwidth), the signal is made available at the Signal Monitor output (J3) and also applied to the third mixer stage.

The third mixer converts the signal to a center frequency of 16 2/3 KHz where it is low pass filtered and applied to an analog to digital converter. The A/D converter produces a serial data stream at a 66 2/3 KHz sample rate for input to the Digital Signal Processor.

Serial data from the DSP at a 133 1/3 KHz sample rate is applied to a digital to analog converter. The D/A output samples are time de-multiplexed into two or three output channels, depending on the mode selection. Half of the D/A output time is devoted to the DSP'd IF output which is first converted back to 455 KHz by mixing with the third LO, then bandpass filtered to 16 KHz bandwidth, and finally made available at the IF Output connector (J4).

The other half of the D/A bandwidth is separated into USB and LSB audio channels in Independent Sideband mode, or into a single audio channel in all other modes.

3-2 PRESELECTOR (81727): Eight bandpass filters covering the frequency range of 500 KHz to 30 MHz are controlled by the DSP/CPU Board (81721). A six FET push-pull amplifier makes up for loss in the bandpass filter.

3-3 PREAMP/ATTN: Refer to Preselector schematic diagram Fig. 9-6. The normal signal path is through pin diode D19 and D20. For weak signal reception, diodes D17 and D18 and preamplifier Q7 may be enabled. For very strong signals, a 15 dB attenuator may be inserted in the signal path by diodes D21 and D22.

3-4 FIRST MIXER (81728): The input signal passes through a 30 MHz low pass filter to a diode mixer and mixes with the amplified first LO to produce an IF frequency of 45.105 MHz. The signal is applied to a six FET push-pull amplifier, then a 2 pole 45.105 MHz crystal filter. A second amplifier and 2 pole 45.105 MHz crystal filter produce an overall 4 pole response at the 1st IF to reject the 2nd mixer image. The 45.105 MHz signal is amplified again for use in the second mixer.

3-5 SECOND MIXER / 3RD LO (81729): The 2nd mixer / 3rd LO board handles the conversion of the first IF of approximately 45.105 MHz to the second and third IFs of 455 KHz and 16 2/3 KHz respectively. It provides outputs to the Signal Monitor connector (J3 #56), the A/D converter (#51), AGC (#16), and LO3 (#52). Required inputs are: 1st IF (#54), LO2 (#55), 10 MHz reference (#57), PLL data (#12), MAGC (#17), and power of ±5 (#20) and +12V (#23).

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The 1st IF input (45.105 MHz) is applied to a high level diode ring mixer along with the amplified 2nd LO (44.6-44.7 MHz) from Q1. The mixer output at 455 KHz is buffered, bandpass filtered and then amplified by controlled-gain IF amplifier U1. The IF amplifier output is post-filtered and then splits three ways: (1) AGC detector Q2/Q3 pulls the IF amplifier gain control pins 9 & 16 low at a rate of 31.25 mV per dB when the output signal exceeds a threshold set by AGC ADJ pot R64. (2) Opamp U2a buffers the IF output and applies it to Signal Monitor connector J3. (3) The IF output is applied to third mixer U3 along with the 471 2/3 KHz 3rd Local Oscillator signal from U4b to produce the third IF of 16 2/3 KHz.

The 3rd IF signal from U3 passes through anti-aliasing lowpass filter U5 to the IF3 output connector #51. DC OSET pot R50 nulls any DC offset at the A/D input (connector #51).

The AGC voltage on IF amplifier pins 9 & 16 is buffered by opamp U2b and output to AGC connector #16. Opamp U6 provides a means for setting the IF gain externally via MAGC connector #17. A current-sink type D/A converter connected to MAGC pulls the IF amplifier gain control pins low, overriding the AGC detector, and reducing IF gain at a rate of 32 dB/Volt.

Phase locked loop U7, charge pump and VCO transistors Q4-Q8, and divider U8/U4 develop the third Local Oscillator frequency of 471 2/3 KHz. This signal drives the third mixer U3 and the 3rd LO output connector #52. The PLL is fixed programmed by the CPU at power-up for a reference frequency of 66 2/3 KHz and a VCO frequency of 37 11/15 MHz.

3-6 CONVERTER-I/O BOARD (81730): The Converter-I/O board contains the main A/D and D/A converters that provide the interface to the Digital Signal Processor, timing and multiplexing circuits that separate D/A data into the various audio and IF channels, and analog reconstruction filters and audio drivers that form the final audio outputs of the receiver. This board also contains the mixer and filter used to convert baseband IF signals back to 455 KHz for the DSP'd IF output.

Refer to the Converter Board schematic diagram Fig. 9-14. Connectors #4, #5 and #64 carry the serial data to and from the DSP. Word framing signals for the A/D and D/A converters (CVST and LDAC), and timing signals for the analog switch de-multiplexers (AF, IF, USB, and LSB) are formed by the dividers and combinational logic circuits U1-U5. Refer to the timing diagram part of Fig. 9-1 for the timing relationships between the converters and de-multiplexers.

The 3rd IF signal at 16 2/3 KHz is applied to the sampling input of A/D converter U7. On command of CVST from U4b, the analog input voltage is converted to a serial bit stream and transferred to the DSP via connector #4.

Serial data from the DSP is transferred to D/A converter U8 via connectors #5 and #64, and, under control of LDAC from U4a, output as discrete voltage samples at V out. Each voltage sample from the D/A converter is steered to the proper audio or IF channel by analog switch de-multiplexers U9 and U10, timed by AF/IF and USB/LSB signals from U4c, d and U5b, c.

Reconstruction filters U11-U14 attenuate the sample clock frequencies (66 2/3 or 33 1/3 KHz) and present a smoothed analog voltage to mode switches U9z and U10z or, in the case of the IF channel, to switching mixer U14b/U15x. The 471 2/3 KHz LO3 from connector #52 mixes with the 16 2/3 KHz baseband IF signal in section x of U15 to produce a 455 KHz component. This component is selected by 16 KHz wide bandpass filter FL1, buffered by opamp U18b, and output to connector #53 and the DSP'd IF Output connector J4.

Based on the mode selected by the CPU/DSP via connector #5, the z sections of U9 and U10 connect the appropriate reconstruction filter outputs to the audio and line drivers U16 and U17. Connector #8 carries both audio channels to the front panel

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ISB level control and stereo phone jack J6. Connector #9 supplies transformer coupled audio to the 600 Ohm line connections on rear panel J8.

Controlled by SB select lines from connector #18, U15 sections y and z connect either one or both audio channels to the monaural audio driver U18a and to audio connectors #7, 10 and 34, rear panel J8, CPU/DSP Board and front panel mono level control and phone jack J7.

3-7 FIRST LO (81731): The first conversion oscillator VCO is split into four ranges to cover the 45.6-75.1 MHz spectrum. The VCO output is buffered by a J310 amplifier before being passed through a bandpass filter and on to the First Mixer (81714). An additional J310 amplifier isolates the VCOs from the MC145170P PLL Frequency Synthesizer IC. The MC145170P develops the reference frequency, accepts frequency information from the microprocessor and outputs a voltage that drives the loop filter and VCOs. Pin 11 of the MC145170P provides a lock detect signal to the CPU/DSP Board (81726).

3-8 SECOND LOCAL OSCILLATOR (81732): The second LO board contains both 2nd LO and Reference frequency synthesizers. The 2nd LO synthesizer develops the second local oscillator injection frequency of 44.6 to 44.7 MHz in 1 KHz steps. The Reference synthesizer locks the 10 MHz internal reference oscillator to an optional external frequency standard.

Refer to 2nd LO schematic Fig. 9-25. The 2nd LO synthesizer is a two loop architecture. PLL chip U1 and charge pump U13 steer VCO Q1/D5/D6 over a range of 60 to 80 MHz in 200 KHz steps. The VCO output is buffered by Q2 and then divided by 200 in counters U2 and U3 to produce a tuning loop output of 300 to 400 KHz in 1 KHz steps for input to the mixing loop phase detector U6.

Phase detector U6, charge pump U7, VCO Q5, and mixer U4 form a mixing loop which translates the tuning loop output to the LO2 frequency range of 44.6 to 44.7 MHz, while preserving the 1 KHz tuning resolution.

The 45 MHz translation frequency required by the mixing loop is developed by first dividing the 10 MHz reference by 2 in U5 to produce a 5 MHz square wave, and then selecting the 9th harmonic with 45 MHz monolithic filter FL1. The resulting 45 MHz sine wave is applied to active mixer U7 along with a sample of the 2nd LO output to produce a 300 to 400 KHz intermediate frequency in the mixing loop.

Differential amplifier Q7/Q8 presents a high impedance to external reference input connector #63 and J2. A sample of Q8's output is detected by diode D13 and compared to a threshold voltage by U9b. When the external reference amplitude exceeds the threshold set by U9b, transistors Q9-Q11 change state, allowing the gate of FET switch Q12 to pull high. This condition connects the output of PLL U8, filtered by U9a, to VCO tuning diode D14, completing the loop and locking the VCXO Y1/Q13 to 10 MHz.

When no external reference is applied to J2, transistors Q9-Q11 conduct, holding the gate of FET switch Q12 low. In this condition the bias on tuning diode D5 is set by trimpot R1, and crystal Y1 is the frequency standard for the receiver.

3-9 DSP/CPU (81726): The DSP/CPU board consists of two separate processor systems; the MAIN CPU (U1) which controls the RX330A's interface and the DSP CPU (U22) which performs signal processing functions. The two system busses integrate together through parallel latches U5-U8. Communication between the MAIN CPU and DSP CPU is handled by a combination of hardware and software, providing bidirectional data capability.

The MAIN CPU system consists of CPU (U1), latch (U2),ROM (U3) and battery backed RAM (U4). Latches U23 and U24 buffer rear panel switch settings while IC's U9 and U10 are for address control. Three Serial/Parallel converters

(U11-U12) add additional output capability to the system. Converter U12 provides VCO selection signals to the FIRST LO BOARD, converter U11 provides audio controls to the CONVERTER BOARD. RS-232 interface controller chip (U15) handles buffering and level translation for the MULTI-DROP network. This is a special RS-232 IC that allows its output to be completely turned off when not active. It is this feature of IC15 that permits multiple connects to a common RS-232 bus. Audio output levels are also monitored by U1 via an internal A/D converter.

U25,U26 and U27 process the DSP digital output. A Programmable Logic device U25 converts the DSP serial output data to a dual byte parallel output and creates the HIBYTE/LOWBYTE, STROBE, IFAF and USB/LSB control signals. U26 and U27 provide output buffering for the data and control signals. In addition, U26 & U27 add tristate capability to the interface with output enabled by software via U11.

The DSP system core consists of the DSP PROCESSOR (U22), ROMs (U21 & U22), AGC A/D (U18), manual AGC DAC (U14), and latch (U19). The DSP system is connected to the CONVERTER BOARD via connectors 4,5,18 and 64. Serial data travels from the CONVERTER BOARD to the DSP/CPU at a 66 2/3 KHz sample rate. After signal processing serial data travels to the CONVERTER BOARD at twice the input rate or 133 1/3 KHz. The DSP output data is multiplexed to provide AUDIO and IF data to the CONVERTER BOARD which demultiplexes the data and directs it to the proper output. Front end AGC levels are monitored by AGC A/D (U18).

3-10 POWER SUPPLY (81733): 120VAC or 240VAC to the input of the power supply is selected by a small pc board in the power entry module. The secondaries of transformer T1 are wired in series to provide 16VAC to a full wave bridge rectifier. The secondaries of transformer T2 are wired the same as T1 and applied to a separate bridge rectifier. The output of both bridges are connected together and filtered by a 4700mf capacitor. This voltage is applied to a chassis mounted 7812 for regulation. The center taps of T1 and T2 are connected together and filtered by a 4700µf capacitor. Regulation is then achieved by a chassis mounted 7805. The secondaries of transformer T3 are wired in series to provide 16VAC to a full wave bridge rectifier. The negative output of the bridge is filtered by a 1000µf capacitor and applied to a chassis mounted 7912 for regulation. The center tap of transformer T3 is filtered by a 470µf capacitor and regulated by a chassis mounted 7905 regulator.

3-11 LED BOARD (81720): Voltage from the four chassis mounted regulators is applied to four individual LEDs. These LEDs offer a visual indication that the power supply is operating.

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