



HF SSB Transceiver

9313/9480 series

Technical service manual

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General Information

1.1 Introduction

The 9313 and 9480 transceivers feature synthesized frequency generation with sealed membrane controls. All differences are in the front panel and the controlling EPROM. All transceiver functions are controlled by a central microprocessor.

The 9313 transceiver has a blank front panel and is connected by up to 100 metres of cable to the control head.

The 9480 comprises of two versions:

- one for front panel control
- one for extended control.

The extended control transceiver has a blank front panel and is connected by up to 100 metres of cable to an 9482 control head. The control head may also be used with the front panel control version allowing for both local and extended control.

Channel capacity is 15 single or two frequency simplex channels in EEPROM. Transmit frequencies may be front-panel entered by a qualified technician or where permitted, by the operator.

The 9313/9480 transceiver has a twenty-digit liquid crystal display showing the transmit and receive frequencies and channel number, or selective call send and receive identification. Selective call addresses may be entered by keypads.

1.2 Specifications

Specification figures will normally be exceeded by production equipment. Where relevant, acceptance limits are given in parentheses. All measurements are made at 13.6V DC, 50Ω source and load, and 25°C ambient temperature (unless otherwise specified).

1.2.1 General

Specifications cover	9313 and 9480 transceiver
Frequency Range	Transmit: 2 to 24MHz Receive: 0.25 to 30MHz
Frequency Generation	All frequencies generated by synthesizer, with 10Hz resolution.
Channel Capacity	15 channels. Transmit frequencies can be entered from the front panel by qualified technical personnel or (where authorised) by the operator.
Operating Modes	9313 Single sideband (J3E) USB 9480 Single sideband (J3E) USB/LSB.
Frequency Stability	USB: $\pm 2(3)$ ppm -30°C to $+60^{\circ}\text{C}$ LSB: $\pm 2(3)$ ppm $\pm 20\text{Hz}$ -30°C to $+60^{\circ}\text{C}$
Long term ageing	1 ppm per year.
Oven warm-up time	1 minute.
Controls	Sealed membrane switches.
Indicators	Refer to illustrations for details. All indicators except Tx may be manually dimmed by front panel controls if required.
Connectors	RF-UHF connector Remote control Antenna control Extension loudspeaker
RF Input/Output Impedance	50 ohms nominal.
Supply Voltage	12V DC nominal, negative earth. Normal operating range 10.5 to 15V DC. Maximum operating range 9 to 16V DC.
Overvoltage Protection	Shutdown at 16V DC (nominal) for duration of overvoltage.

Supply Current

9313/9480: Receive, no signal, 800mA.
Transmit: see section 1.2.3

Environmental

Ambient Temperature	Relative Humidity
-30°C to +30°C	95%
+30°C to +60°C	from 95% at +30°C to 30% at +60°C

Derate upper ambient temperature by 1°C per 330m above sea level.

Cooling

Convection or fan (Option F).

Size and weight

Transceiver only:
250mm W x 78mm H x 350mm D;
3.41kg

With mounting cradle:
270mm W x 90mm H x 350mm D;
3.92kg

9313/9480 Control Head:
180mm W x 65mm H x 70mm D;

With mounting bracket:
190mm W x 78mm H x 70mm D; 700g

With mounting bracket: 252mm W x
92mm H x 70mm D; 900g

Note: Depth measurements (D) include rear connectors/cables.

Finish

Case: Silver-grey
Panel surround and heat sink: Matt black
Panel overlay: Lexan—Matt black

Painted surfaces are scratch-resistant textured polyester powdercoat.

1.2.2 Receiver

Type	Dual conversion superheterodyne.
IF Frequencies	45MHz, 1650kHz.
Sensitivity	0.25 to 0.5MHz: Not specified 0.5 to 2MHz: Approximately 8 μ V PD 2 to 28MHz: 0.25(0.35) μ V PD [-119(-116)dBm] for 10dB SINAD with greater than 50mW audio output. 28 to 30MHz: 0.5 μ V PD
Input Protection	Will withstand 50V rms RF from a 50 Ω source.
Selectivity	Greater than 70(65)dB at -1kHz and +4.2kHz ref SCF USB. Pass band -6(-8)dB 300 - 2800Hz. Ripple 1.5(3)dB pp 500 - 2500Hz.
Desensitisation	10dB SINAD reduced to 7dB SINAD. -1 and +4.4kHz ref SCF (USB) 62(55)dB. \pm 10kHz 85(80)dB. \pm 50kHz 100(95)dB.
Image Rejection	Better than 90(80)dB
Spurious Responses	Better than 90(70)dB. Self generated signals >0.25 μ V PD; 6.6MHz, 9.998MHz, 13.2MHz, 19.8MHz, 26.4MHz.
Cross Modulation	A signal 90(85)dB above a signal producing 10dB SINAD, modulated 30% and removed at least 20kHz from the wanted signal will produce an increase in receiver noise of less than 3dB.
Blocking	As for desensitisation.
Intermodulation	To produce a third order intermodulation product equivalent to a wanted signal producing 10dB SINAD, two unwanted signals greater than 30kHz removed from the wanted signal must have a level greater than 85(80)dB above the wanted signal. Third order intercept +10(7)dBm, not affected by AGC.
AGC	Less than 6dB variation in output level for input variations between 1.5(2.5) μ V and 100mV PD. Fast attack, slow release.
AF Response	-1 typical (-3)dB 300 to 2800Hz.

AF Power and Distortion	2.5W into 8 ohms: 5% THD 5W into 4 ohms: 5% THD 8W into 2 ohms: 5% THD
Clarifier	±0.001% Clarifier is automatically reset to mid-range with channel change.
Inband IMD	Better than 25dB IMD with two 50mV PD RF inputs.
Signal to noise vs Input Level	5μV PD: 34dB S/N 50μV PD: 53dB S/N 500μV PD: 60dB S/N

1.2.3 Transmitter

Power Output 9313	100W PEP at 2MHz falling linearly with frequency to 90W PEP at 24MHz ±0.5dB.
Power Output 9480	125W PEP at 2MHz falling linearly with frequency to 90W PEP at 24MHz ±1dB. CW or single tone: approximately 60% of PEP with average PEP control.
Duty Cycle	100% normal speech over full temperature range.
Supply Current	Output power 100/125W 2-tone or CW: 9 to 12A Average speech: 6A for battery life calculations.
Protection	Safe under all load conditions by limiting reflected power to 6W and limiting PA transistor collector voltage swing. Thermal protection against excessive heatsink temperature.
AF Response	Overall response of microphone and transmitter rises approximately 6dB/octave 300 – 2800Hz. Electrical input –6(–8)dB, 300 – 2800Hz. Ripple 1.5(3)dB pp, 500 – 2500Hz.
Spurious & Harmonic Emissions	Better than 60(48)dB below PEP.
Carrier Suppression	60(50)dB below PEP.

Unwanted Sideband	50(45)dB below PEP (400Hz) 70(65)dB below PEP (1kHz)
Intermodulation Distortion 2-tone Test	100W: 32(26)dB below each tone 38(32)dB below PEP 125W: 30(26)dB below each tone 36(32)dB below PEP
ALC	A 10dB increase in input level above compression threshold produces less than 0.5dB increase in power output. Maximum ALC range greater than 30dB. ALC attack time approximately 1mS.
Residual Noise	65(55)dB below PEP in 3kHz channel.
Transmitter Noise Floor	Transmitter noise output below cut-off frequency of harmonic filter in 3kHz bandwidth typically -67dBm.
Microphone	Dynamic type with push-to-talk switch fitted in case.

1.2.4 Rear Panel Connectors

The following tables show the pin connections, functions, and signal levels for the rear connectors.

Antenna Select Facility (15-way, D-type Socket)

Pin Number	Function	Signal Level
1	Channel Number Bit 3	Logic (Open Collector)
2	Channel Number Bit 4	Logic (Open Collector)
3	N/C	
4	TUNE IN/OUT	5V Logic (Active Low)
5	SCAN (Active Antenna)	Logic (Open Collector)
6 & 7	N/C	
8	PTT out	+10V (1k Ω source)
9	Channel Number Bit 1	Logic (Open Collector)
10	Channel Number Bit 2	Logic (Open Collector)
11	TUNED IN	5V Logic (Active Low)
12 & 13	A rail	+ Battery supply out

14 & 15	0V	Ground
---------	----	--------

N/C = Not Connected

All channel number bits active high. (Pull-up resistors required.)

Option R (15-way, D-type Plug)

Pin Number	Function	Signal Level
1	Loudspeaker	Ref Spec
2	Remote PTT	0 Volts = PTT
3	Receiver Audio Output	Special *
4	Power On	Momentary 0V for Power ON
5	Data	5 Volt Logic
6	Data Line Enable	5 Volt Logic
7	Clock	5 Volt Logic
8	Transmit Lamp	Modulated by Tx output
9 & 10	0V	Ground
11	Transmit Audio I/P	Nom. 1.5Vpp (8k Ω input impedance)
12	Receiver Demodulator O/P	Nom. 1.5Vpp (1k Ω output impedance) (Min. load 5k Ω)
13	Receiver Audio I/P	Special*
14	Interrupt	5 Volt Logic
15	A rail	+ Battery supply out

* Special: adjusted to suit attached equipment

1.2.5 Front Panel Connector

Microphone Connector

Pin Number	Function
1	PTT ground
2	PTT active low
3	Microphone input
4	Microphone ground
5	N/C
6	Audio output
7	Audio output

1.3 Options and Accessories

1.3.1 Options

The following is a list of the options available with brief descriptions.

AD Fit antenna driver interface for 8558 automatic tuning whip antenna.

Programmable Options (per channel)

E RFDS Emergency call (9313 only).

INHIBIT Receive only.

1.3.2 Accessories

The following is a list of the accessories available.

Code

112 Vehicle installation hardware kit.

117 Vehicle mounting cradle—front entry.

649 Extension loudspeaker.

704 Vehicle interference suppression kit.

1.4 Abbreviations

A/D	Analog to digital
A/F	Across flats (hexagon)
AC	Alternating Current
ACIA	Asynchronous Communication Interface Adapter
ADJ	Adjust
AF	Audio Frequency
AFC	Automatic Frequency Control
AGC	Automatic Gain Control
ALC	Automatic Level Control
ALF	Absorbtion Limited Frequency
AM	Amplitude Modulation
ASCII	American Standard Code for Information Interchange
ASSY	Assembly
ATU	Antenna Tuning Unit
AUX	Auxiliary
AV	Average
BAL	Balance
BALUN	Balanced to Unbalanced Transformer
BCD	Binary Coded Decimal
BPF	Band Pass Filter
BW	Bandwidth
C/O	Change-over
CAL	Calibrate
CCT	Circuit
CCW	Counterclockwise
CH	Channel
CMOS	Complementary Metal Oxide Semiconductor
COAX	Coaxial
COM	Common
CPU	Central Processing Unit
CRO	Cathode Ray Oscilloscope
CRT	Cathode Ray Tube
CSK	Countersink

CW	Continuous Wave, Carrier Wave or Clockwise
D/A	Digital to Analog
DC	Direct Current
DEMUX	Demultiplexer
DMA	Direct Memory Access
DPDT	Double Pole, Double Throw
DPST	Double Pole, Single Throw
DRG	Drawing
DSB	Double Sideband
DTL	Diode Transistor Logic
DVM	Digital Voltmeter
dB	Decibel
dBm	Decibel relative to 1mW
EAPROM	Electrically Alterable Programmable Read Only Memory
ECL	Emitter Coupled Logic
EDP	Electronic Data Processing
EEPROM	Electrically Erasable Programmable Read Only Memory
EMF	Electromotive Force
EMI	Electromagnetic Interference
EPROM	Erasable Programmable Read Only Memory
EXT	External
F/V	Frequency to Voltage
FET	Field Effect Transistor
FM	Frequency Modulation
FREQ	Frequency
FSK	Frequency Shift Keying
FTTL	Fast Transistor Transistor Logic
GND	Ground
GPIO	General Purpose Interface Bus
HCMOS	High Speed Complementary Metal Oxide Semiconductor
HEX	Hexadecimal or Hexagon
HF	High Frequency
HMOS	High Speed Metal Oxide Semiconductor
HORIZ	Horizontal

HPF	High Pass Filter
I/COM	Intercom
I/F	Interface
I/O	Input Output
I/P	Input
IF	Intermediate Frequency
IMD	Intermodulation Distortion
INT	Internal
ISB	Independent Sideband
JFET	Junction Field Effect Transistor
J3E	Single Sideband Suppressed Carrier Telephony Emission
LC	Inductance-Capacitance
LCD	Liquid Crystal Display
LDR	Light Dependent Resistor
LED	Light Emitting Diode
LF	Low Frequency
LIN	Linear Law
LNA	Low Noise Amplifier
LO	Local Oscillator
LOG	Logarithmic Law
LPF	Low Pass Filter
LS	Loudspeaker or Low Power Schottky
LSB	Lower Sideband or Least Significant Bit
LSI	Large Scale Integration
LSTTL	Low Power Schottky Transistor Transistor Logic
LTU	Line Terminating Unit
MAX	Maximum
MF	Medium Frequency
MIN	Minimum
MODEM	Modulator-Demodulator
MOL	Maximum Operating Level
MOS	Metal Oxide Semiconductor
MPU	Microprocessor
MSB	Most Significant Bit
MSI	Medium Scale Integration

MUF	Maximum Useable Frequency
MUX	Multiplex, Multiplexer
N/C	Normally Close
N/O	Normally Open
NC	Not Connected
NMOS	N Type Metal Oxide Semiconductor
NOL	Normal Operating Level
NOM	Nominal
NORM	Normal
NPO	Zero Temperature Coefficient
NTC	Negative Temperature Coefficient
O/C	Open Circuit
ODU	Outdoor Unit
OMT	Orthomode Transducer
O/P	Output
OPR	Operator
OPT	Option
OSC	Oscillator
OWF	Optimum Working Frequency
PA	Power Amplifier
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PD	Potential Difference
PEP	Peak Envelope Power
PH	Phase
PIA	Peripheral Interface Adapter
PIV	Peak Inverse Voltage
PKG	Package
PLL	Phase Locked Loop
PMOS	P Type Metal Oxide Semiconductor
POL	Peak Operating Level
POT	Potentiometer
PP	Peak to Peak
PPM	Parts per Million
PROM	Programmable Read Only Memory
PSU	Power Supply Unit

PTC	Positive Temperature Coefficient (Resistor)
PTT	Push To Talk
PUT	Programmable Unijunction Transistor
PWM	Pulse Width Modulation
RAM	Random Access Memory
R/C	Remote Control
RC	Resistance-Capacitance
RCU	Remote Control Unit
REF	Reference
REG	Regulated, Register
RF	Radio Frequency
RFI	Radio Frequency Interference
RMS	Root Mean Square
ROL	Reference Operating Level
ROM	Read Only Memory
RTL	Resistor Transistor Logic
RTTY	Radio Teletype
Rx	Receive, Receiver
S/C	Short Circuit
S/N	Signal To Noise
(S+N)/N	Signal Plus Noise to Noise Ratio
SCF	Suppressed Carrier Frequency
SCR	Silicon Controlled Rectifier
SINAD	Signal + Noise + Distortion to Noise + Distortion Ratio
SMPS	Switching Mode Power Supply
SOT	Select On Test
SPDT	Single Pole Double Throw
SPST	Single Pole Single Throw
SSB	Single Sideband
STTL	Schottky Transistor Transistor Logic
SWR	Standing Wave Ratio
SYNC	Synchronisation
SYNTH	Synthesizer
T/R	Transmit Receive
TC	Temperature Coefficient
TCVR	Transceiver

TCW	Tinned Copper Wire
TCXO	Temperature Compensated Crystal Oscillator
TVRO	Television Receive Only
TDM	Time Division Multiplex
THD	Total Harmonic Distortion
TRIG	Trigger
TS	Tag Strip
TSM	Technical Service Manual
TTL	Transistor Transistor Logic
TYP	Typical
Tx	Transmit, Transmitter
UART	Universal Asynchronous Receiver Transmitter
UJT	Unijunction Transistor
USART	Universal Synchronous/Asynchronous Receiver Transmitter
USB	Upper Sideband
UT	Universal Time
UTC	Universal Co-ordinated Time
V/F	Voltage to Frequency
VA	Volt ampere
VCO	Voltage Controlled Oscillator
VCXO	Voltage Controlled Crystal Oscillator
VDR	Voltage Dependent Resistor
VERT	Vertical
VFO	Variable Frequency Oscillator
VHF	Very High Frequency
VOX	Voice Operated Switch
VSWR	Voltage Standing Wave Ratio
VU	Volume Unit
WRT	With Respect To
WT	Weight
XTN	Extension
XTND	Extend
λ	Wavelength
+ve	Positive
-ve	Negative

∅ Phase, Diameter in mm

Note: EMF is the source voltage behind the output resistance (R_s) and is independent of the signal generator loading. Many signal generators are calibrated in PD (across the load) assuming a total load resistance equal to the generator source resistance; for these, the EMF is twice the attenuator scale reading.

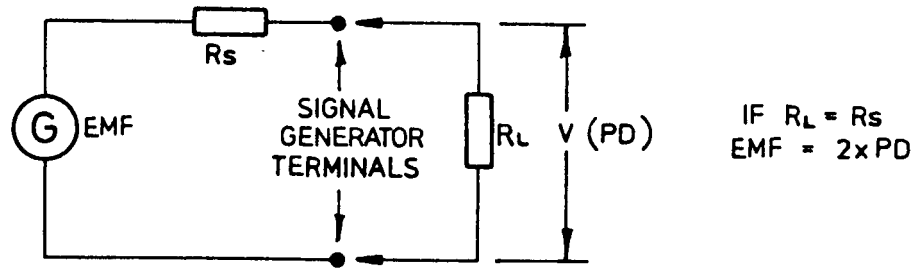


Figure 1.1 EMF Verses PD

1.5 Circuit Reference Designations

A	Assembly
B	Transducer—Microphone, Loudspeaker, etc
C	Capacitor
D	Diode—small signal and power
E	Heating device
F	Protection device—Fuse, etc
G	Generator—battery, etc
H	Signalling/indicating device—Lamp, LED, Buzzer, etc
IC	Integrated Circuit, thick film hybrid
J	Jack socket
K	Relay, key switch
L	Inductor
M	Indicating device—meter, etc
P	Plug
R	Resistor
S	Switch
T	Transformer, common mode choke
TP	Test Point
U	Modem, Modulator
V	Semiconductor (not including small signal and power diodes)
X	Terminals
Z	Quartz Crystal, Crystal Filter, Frequency Network

1.6 Units

A	Ampere	m	metre
C	Celsius (degrees)	min	minute
C	Coulomb	N	Newton
F	Farad	Pa	Pascal
g	gram	S	Siemen
h	hour	s	second
H	Henry	T	Tesla
Hz	Hertz	V	Volt
J	Joule	W	Watt
K	Kelvin (degrees)	Wb	Weber
l	litre	Ω	Ohms

1.7 Unit Multipliers

T	tera	one million million	10^{12}
G	giga	one thousand million	10^9
M	mega	one million	10^6
k	kilo	one thousand	10^3
h	hecto	one hundred	10^2
da	deca	ten	10
d	deci	one tenth	10^{-1}
c	centi	one hundredth	10^{-2}
m	milli	one thousandth	10^{-3}
μ	micro	one millionth	10^{-6}
n	nano	one thousand millionth	10^{-9}
p	pico	one million millionth	10^{-12}



3

Brief Description

3.1 General

This description should be read in conjunction with Block Diagram 03-00905.

The same frequency conversions are used in both transmit and receive modes, therefore many circuits are common to both modes of operation. Signal routing is determined by switching and control voltages according to the mode selected.

3.2 Receive

The RF signal from the antenna passes through the PA low-pass filters, then via the transmit/receive relay and broadcast filter on the PA PCB, to the switched high-pass filters on the RF, Mixer, and Dual Synthesizer PCB. Filters are automatically selected according to the frequency band in use.

The band-pass filtered signal is applied to the first mixer. This double-balanced, diode-ring mixer, driven from VCO1, converts the signal up to a 45MHz IF signal.

The 45MHz signal is amplified and filtered with a 20kHz wide 'roofing' filter. The output of this filter is mixed with the output of VCO2 in another double-balanced, diode-ring mixer. This produces a second IF of 1650kHz.

The second IF signal is passed to the IF amplifier and noise limiter. The noise limiter is designed to suppress impulse noises such as motor vehicle ignition noise. The limiter operates by 'gating' the IF signal path for the duration of the noise pulses.

The crystal filter on the Audio and 1650kHz IF PCB reduces the bandwidth to 2.5kHz before passing the signal to the 1650kHz tuned AGC controlled IF amplifier.

The signal is then demodulated to provide an audio signal which is fed via the mute gate to the digital volume control and audio PA where it is amplified before being passed to the speaker.

3.3 Transmit

The audio signal is amplified and levelled in the microphone amplifier and compressor, then fed to the balanced modulator where it is mixed with the 1650kHz (USB) or 1647kHz (LSB) local oscillator to produce a DSB signal. The resulting signal is filtered by the 2.5kHz crystal filter to produce the SSB signal (USB or LSB) required for transmission.

In the transmit mode, the IF amplifier is switched to produce a buffer to feed the mixer where the SSB signal is mixed with the output of VCO2 to produce the 45MHz IF signal.

After the 'roofing' filter, the signal is mixed with VCO1 output to produce the required channel frequency (2MHz to 24MHz). This is taken, via the transmit/receive switch, to the PA and Filter PCB where it is amplified and filtered (band-switched filters) before being passed to the antenna.

Forward and reflected power circuits are used to control the power amplifier. If a high VSWR is detected, the PA's output power is reduced to prevent damage.

3.4 Synthesizers

Two single-loop synthesizers are used, the main synthesizer (VCO1) generating a 45.25MHz to 75MHz signal i.e. 0.25 to 30MHz, plus 45MHz, in 2kHz steps, and a 'vernier' synthesizer (VCO2) generating 43.352 to 43.350MHz in 10Hz steps.

The synthesizers are controlled by the microprocessor which controls the transceiver. Serial data is loaded into both synthesizers; the data varying according to the required channel frequency preprogrammed into memory.

The system uses a single oven crystal reference oscillator of 6.6MHz. This reference is also used to provide the 1650kHz (6.6MHz divided by 4) signal for the audio modulator/demodulator.

3.5 Display, Control and Switching

All the transceiver functions are microprocessor controlled with the required channel frequencies, facilities, etc being preprogrammed into an Erasable Programmable Read Only Memory (EPROM).

The 9313/9480 control head displays, and switch-pads are controlled via a two-wire serial bus.

Other functions such as filter switching, PTT and tone generation are controlled either by buffered microprocessor signals or the relay-switched 'C' and 'D' supply voltages. The microprocessor switches the associated relay (K1 on the Motherboard), depending on the transceiver mode. The relay is energised during transmit and de-energised in receive.



4

Technical Description

All circuit paths of the following PCB assemblies are made through the Motherboard and Chassis (04-02453), where the connector and pin numbers of the interconnections are shown:

RF Mixer & Dual Synthesizer	(04-02450)
Audio & IF 1650kHz	(04-02093)
Microprocessor Controller	(04-03031)
Front Panel Display PCB	(04-03045)
Control Head	(04-03038)
PA & Filter	(04-02452)

4.1 Control and Supply Voltages

All switching, except 'power-on', is controlled either directly or indirectly by the microprocessor on the Microprocessor Controller PCB.

4.1.1 Supply Voltages

The supply voltages used are as follows:

- **'A' rail**—unregulated battery supply.
- **'B' rail**— +10 Volt regulated supply derived from the 'A' rail.
- **Volt supplies**—individual three-terminal regulators supplied from 'A' rail.
- **Volt supply**—'pump up' switching supply on the RF Mixer and Dual Synthesizer PCB (IC1).

4.1.2 Power and Control Lines

By controlling relay K1 on the Motherboard, the microprocessor on the Microprocessor Controller PCB generates two switched +10V power and control lines designated as the 'C' and 'D' rails. These rails are defined as follows:

- 'C' rail—10 volts on receive; 0 volts on transmit.
- 'D' rail—0 Volts on receive; +10 Volts on transmit

All other control lines come directly from the Microprocessor Controller PCB and are described in section 4.5.

4.1.3 Overvoltage and Reverse Voltage Protection (refer Dwg 04-02452)

Overvoltage protection is provided by V3, V2, R4, R5 and V1 on the PA and Filter PCB. If the battery voltage rises above the 15V reference of V1, plus V2 V_{be} drop and the 0.6V diode drop of D6, transistor V2 turns on and hence turns off V3 to de-energise the power-on relay K7. This occurs at nominally 16V. Diode D6 provides reverse voltage protection.

4.1.4 Transceiver Power On/Off

When primary power is first applied to the transceiver, V3 on the PA and Filter PCB (04-02452) is turned on (by R5 to ground) charging C56 through D6 and K7 which momentarily pulses on. With primary power applied and in the power off condition, K7 is de-energised and the dual-coil latching relay K2 on the Motherboard (04-02453) is in the 'off' position.

Switching power on is a hardware operation; switching off is basically a software operation.

When the power on-off pad on the front panel is pressed, a ground is applied to the cathode of D4 on the Display PCB. This will forward bias V2 via R12 on the Motherboard. The emitter of V2 is connected to the positive supply via K7, V3 and D6 on the PA PCB. When V2 on the Motherboard conducts, latching relay K2 contacts close, operating the power-on relay K7. C56 ensures that there is sufficient current to toggle K2.

Operation of the on/off pad on a control head (when connected), switches on V2 via the rear panel connector P502 pin 4. This has the same effect as operation of the front panel on/off pad.

Once power 'on' has been established, the diodes connected to the power on/off switch-pad are reverse biased, and no longer affect the operation of those lines.

Pressing the power on/off pad with relay K2 set to 'on' has no effect on V2 on the Motherboard. However, via the front panel I²C bus control, the microprocessor grounds the Power Off line, J3 pin 5. This energises the 'off' coil of K2, toggling the relay back to its 'off' state. Contacts of K2 open to break the energising path for relay K7 on the PA and filter PCB.

4.2 Receiver

4.2.1 Input Filters (Refer 04-02452)

The receiver input signal is passed through the PA low-pass filter selected by the PA band line, the transmit/receive relay K6 and the 2MHz high-pass broadcast filter to the RF, Mixer & Dual Synthesizer PCB.

Option LF adds a 1nF capacitor C111 in parallel with C47, reducing the broadcast filters passband to 1.6MHz. D3 and D4 provide protection against excessive input signals.

4.2.2 Mixers, First IF Amplifiers and Filters (Refer 04-02450)

The receive input signal enters the PCB at pin 1 of J1. Five high-pass filters are used to complete the bandpass filter characteristics and are switched according to the frequency band in use by grounding the appropriate select line (The band 2.0 to 3.1MHz is not filtered on this board). From the selected filter, the received RF is passed via a 28MHz low-pass filter (C32 to C37 and L15 to L18) to the first mixer.

The first mixer is a double-balanced, diode-ring mixer consisting of transformers T1 and T2, and diode ring D13 to D16. The 0.25MHz to 30MHz signal is mixed with the output of VCO1 (45.25MHz to 75MHz) to produce the first IF signal, at 45MHz.

FETs V7 and V8 are switched as a grounded-gate amplifier through diodes D22 to D24 by the C rail being high and D rail being 0V. The amplified output is passed, via a crystal roofing filter Z1 (approx. 20kHz bandwidth) to FET V9.

FET V9 is switched as a source follower by the C and D rails through diodes D26 to D29. The output is applied to the second mixer, formed by transformers T5 and T6, and diode ring D31 to D34. The 45MHz signal is mixed with the output of VCO2 (43.350MHz to 43.352MHz) to produce the second IF signal at 1650kHz. This signal is passed to both the second IF amplifier and the noise blanker.

FETs V16 and V17 are switched to form the second IF amplifier as a grounded gate amplifier by the C and D rails through diodes D35 to D38.

4.2.3 Noise Blanker

The 1650kHz IF signal is amplified by the RC coupled stages V15 and V18 and fed to the tuned collector amplifier V20. V21 is an active rectifier. Noise bursts produce negative going pulses at the emitter of V21 which drives the monostable flip-flop V25 and V26. The output of V25 and V26 are complementary gating pulses which are fed to FET gates V23 and V24 respectively. With V23 on and V24 off, the IF signal is passed to the crystal filter. With V23 off and V24 on, the IF signal is blocked.

The average DC component of the collector current of V21 passing through R65 is amplified by V22 and applied as reverse AGC to V15 and V18. Thus only impulse type signals produce sufficient rectified output at V21 emitter to trigger the monostable. C119 sets the monostable pulse width such that the noise burst has finished before the IF is again enabled.

C rail biases off V15 and V18 in transmit and the noise blanker may be disabled for test purposes by grounding TP6.

4.2.4 IF Crystal Filter and Amplifier (04-02093)

The 1650kHz IF signal from the noise gate on the RF Mixer and Dual Synthesis PCB (V23, V24 04-02450) enters the board at P1 and is filtered by Z1 to pass 1647.2kHz to 1649.7kHz (2.5kHz bandwidth) to the two-stage AGC amplifier V2 and V3. IF output amplifier V4 drives the demodulator IC8 and the AGC active rectifier V6. AGC attack time is set by R21/C17 and release time by R24/C17, giving a fast attack/slow release response. Divider R23/R24 sets the AGC threshold level while the voltage set by the divider, combined with the gain of IC1a, IC1b and the bias on IC1b positive input, determines the static AGC voltage. D2 and D3 hold the sources of V2 and V3 positive to enable the AGC voltage applied to gate 2 of these FETs to go negative with respect to sources for full AGC control.

4.2.5 Demodulator

The IF from V4 is converted to the required audio output by double balanced mixer IC8. When receiving an RF USB signal, the IF signal is LSB with an SCF of 1650kHz due to the sideband inversion in the first mixer. With an RF LSB signal, the IF signal is USB with an SCF of 1647kHz. Thus the demodulator requires a 1650kHz local oscillator for USB reception and a 1647kHz local oscillator for LSB reception at P2. The oscillators are described in Section 4.4.5.

The audio output (pin 6) of IC8 passes through a third-order low-pass filter IC4a and associated components to remove noise above the wanted audio bandpass.

4.2.6 Audio Mute

The audio from the output of IC4a is looped back through the Motherboard to the Audio and IF 1650kHz PCB and applied to the audio mute input (R63/C37) and the mute gate (V12).

IC4b and IC3a are arranged as a squaring amplifier. The squared signal charges C38 via D8 during negative excursions and the charge is transferred to C39 by V13 during positive excursions. The resultant DC voltage on C39 is proportional to the frequency of the audio. IC3b and its associated components form a low-pass filter with a cut-off frequency of approximately 10Hz. The output from IC3b is a DC voltage varying at the syllabic rate of the received speech.

IC5a and IC5b form a window comparator whose window width is adjusted by R73, setting the mute sensitivity. The divider formed by R75 and R76, together with C42, averages the output of IC3b and provides the reference voltage for the window comparator. If the output from IC3b rises above or below this reference by the amount set by R73, then the output of either IC5a or IC5b will go high.

The comparator outputs are diode ORed into C43 to provide a fast attack, slow release (3 seconds) mute control signal.

The microcontroller on the Microprocessor Controller PCB can override the mute control circuit in two ways:

- It can force the unmuted condition by grounding the inverting input of IC6b (via J3 pin 9). This applies a high to the gate of V12 to switch it on.
- It can force the muted condition by grounding the gate of V12 via J3 pin 8.

The control circuit is also over-ridden at D7 by the C rail being taken to 0V in transmit. This forces the mute condition, thus preventing acoustic feedback during transmission.

4.2.7 Volume Control and Audio Amplifier

The post-mute audio from V12 is passed to the volume control section. The switches in IC9 control a resistive ladder network used as an attenuator. Sixteen steps are available with each step, giving approximately 4dB attenuation for a total of 64dB. The switches in IC9 are controlled by the microprocessor on the Microprocessor Controller PCB.

IC6a buffers the attenuated audio and passes it to the audio amplifier, IC10. The audio amplifier is capable of 8 Watts output into a 2 ohm load and gives approximately 2 Watts into the internal 8 ohm speaker.

4.3 Transmitter Exciter

4.3.1 Microphone Amplifier (Refer Dwg 04-02093)

The input to the microphone amplifier is J1, pin 6. Transistor V7 is an audio clamp which is released only when the microphone PTT button is pressed. This prevents the microphone picking up background noise and sidetone from the loudspeaker when transmitting emergency calls etc.

IC2a amplifies the microphone input to approximately 1V pp (gain=100). The signal is then connected to the AGC detector (IC2b, V10) and the modulator (IC8).

The output of IC2a to the AGC detector is fed directly to V10, and via inverter IC2b, to V11. Transistors V10 and V11 form a full wave rectifier to drive V9, which in turn drives V8 to complete the AGC loop by shunting the input signal to ground.

The release time-constant of the amplifier is set by R37 and C25. Diode D4 allows the gain to rise exponentially to maximum. The three-terminal regulator IC7 prevents power supply variations affecting the AGC circuit.

4.3.2 Modulator

The microphone amplifier output is capacitively coupled via C28 to the temperature compensating resistor network R55 and R56. R55 is an NTC resistor; as the temperature increases its resistance decreases and so the audio signal level passed to IC8 increases. This is to compensate for reduced gain at higher temperatures mainly in the 45MHz IF amplifier.

The selection of the AM (H3E) mode forward biases V3 on the Motherboard (04-02453). This switches R17, R27 and C23 (also on the Motherboard) into circuit between the microphone amplifier output J1 pin 3 and ground. This attenuates the audio signal to the lower level required by the modulator in this mode. Link Y is inserted in H versions which reduces the audio drive by approximately 3dB to improve the exciter IMD products.

IC8 is the modulator during transmit and mixes the audio signal with the 1650kHz (1647kHz, LSB) local oscillator to produce a DSB signal output, centred on the LO frequency, from pin 12.

This signal is then passed via the transmit/receive switch V1 and D1 to the 1650kHz crystal filter.

4.3.3 Crystal Filter

One sideband of the DSB signal from the modulator is selected by the crystal filter to give an SSB signal. During transmit, the C rail is at 0 Volts, and forces a low output from IC1b for maximum AGC to V2 and V3. Thus, none of the transmit signal passes through the IF Amplifier.

4.3.4 Mixers, IF Filters and IF Amplifier (Refer Dwg 04-02450)

The SSB signal from the crystal filter is applied to J4 on the RF Mixer and Dual Synthesizer PCB. As the C rail is at 0 Volts in transmit, the noise blanker is disabled, switching V23 on and V24 off.

V16 and V17 are switched as a source follower selected by the C and D rails, via diodes D35 to D37. The output is applied to the double-balanced, diode-ring mixer formed by T5, T6, and D31 to D34. Here the signal is mixed with the output of VCO2 (43.352 to 43.350MHz) to produce the 45MHz IF.

The 45MHz IF signal is amplified by V9 switched as a grounded-gate amplifier by C and D rails, via diodes D26 to D29. The amplified output is passed to the crystal roofing filter (Z1) to remove the unwanted mixer products.

V7 and V8 are switched as a source follower by the C and D rails, via diodes D22 to D25. The output is passed to the double-balanced, diode-ring mixer formed by T1, T2 and D13 to D16. Here the 45MHz IF signal is mixed with the output from VCO1 to produce the required channel frequency. This signal is filtered by the 28MHz low-pass filter then passed by D12 to the Power Amplifier input.

The receive band-switched filters are switched off while transmitting.

4.4 Local Oscillators (04-02450)

Two synthesized oscillators are used to drive the first and second mixers. The first oscillator operates between 45.250MHz and 75MHz in 2kHz steps to convert the 250kHz to 30MHz received signal to 45MHz for the first IF. The second oscillator operates between 43.352 and 43.350MHz in 10Hz steps to convert the 45MHz first IF to the 1650kHz second IF.

Each oscillator consists of a voltage controlled oscillator (VCO), a divider, a phase/frequency detector and loop amplifier/filter together with a reference crystal oscillator and divider.

The division ratios required are provided in serial data form from the microprocessor from data stored in the memory. The reference frequency crystal (6.6MHz) is held at a constant temperature by a power PTC thermistor and is divided by 4 to provide the 1650kHz drive to the modulator/demodulator in USB operation. For LSB operation, a separate 1647kHz crystal oscillator is required.

4.4.1 Voltage Controlled Oscillators (VCO)

As VCO1 and VCO2 are virtually identical, only VCO1 will be described in detail:

- FET V2 operates as a Hartley oscillator tuned by varicaps D17 to D20. The output is levelled by schottky diode D21 which generates a negative bias voltage for V2 gate.
- Unity gain feedback amplifier V3/V4 provides a buffer between the oscillator and the cascade connected amplifier V5/V6. The amplifier provides the +7dBm drive to the ring diode mixer and also drives the divide by 64/65 prescaler IC6.
- VCO2 differs from VCO1 only in having a single varicap because of the reduced frequency range required.

4.4.2 Phase/Frequency Detectors and Dividers

IC5 generates a DC voltage which controls the varicaps in VCO1 in order to lock the oscillator to its nominated frequency. A 6.6MHz oscillator in IC5 controlled by the crystal Z2, is divided within the IC to give a 2kHz reference for a phase/frequency detector also in the IC. VCO1 output is divided in a prescaler, IC6, and applied to further dividers in IC5, allowing for the VCO frequency to be changed in 2kHz steps. The divided output is compared with the 2kHz reference frequency.

When the phase/frequency difference is considerable, e.g. immediately after a change of channel, the output from PDB (IC5 pin 2) consists of pulses with their mark:space ratio proportional to the difference. These are integrated by R82 and C123 to provide an input to IC2b. The signal is further filtered by R85 and C127, while the output from IC2b is filtered by R90, R91, C131, C132, C133 and C134. At the same time PBA pin 1 gives an analogue output proportional to the phase/frequency difference. This is also applied to the input of IC2b, via R80. The resulting output drives VCO1 in the direction required to obtain the correct frequency, thus providing a coarse control of the frequency.

When the phase/frequency difference becomes small the PDB output goes high impedance and the analogue output from PDA becomes the only input to IC2b. This provides the fine control of the VCO1 output.

IC7 generates the DC voltage required to control the varicaps in VCO2. A similar arrangement of prescaler and internal dividers divides the VCO2 output in the same way as VCO1 was divided in IC5. The result is compared with a reference frequency within IC7. The 6.6MHz crystal oscillator output from IC5 is applied in IC7 to a divider which can be programmed to provide reference frequencies between 1.1 and 2kHz. This allows VCO2 frequency to be changed in 10Hz steps.

Coarse control of VCO2 is provided by the Freq output (pin 6) from IC7. This consists of low pulses if the VCO frequency is too high, and high pulses if it is too low. These are integrated in C147 to provide the correcting voltage to VCO2. Fine control is provided by the Phase output (pin 17).

4.4.3 Lock Signals

Both phase/frequency detectors give an output which is low while the VCO and reference frequencies are locked, and high when they are unlocked. The LD output from IC5 pin 3 is applied to the base of V28 and the Charge output from IC7 pin 4 is applied to V29. Thus the corresponding transistor is switched on to light the LED indicator (H1 or H2) in its collector circuit if either loop loses lock. The collector circuits are ORed by D45 and D46 so that if either collector is low, i.e. one loop has lost lock, an Unlock output is passed to the Microprocessor Controller PCB.

4.4.4 Loading Frequency Data to Synthesizers

Data containing the required division factors for both synthesizers is applied from the Microprocessor Controller PCB over the Data line. The serial data is clocked into IC7 under the control of the signal on the clock line. The first twenty-eight bits are clocked through IC7 and into IC5, via SR Out (pin 14) of IC7. When the twenty-eight bits have been clocked they are loaded in IC5 by the Enable 1 pulse from the Microprocessor Controller PCB. Similarly the next thirty-two bits are loaded into IC7 by the Enable 2 pulse.

4.4.5 1650/1647kHz Local Oscillators

When receiving (or transmitting) a USB signal, a 1650kHz local oscillator is required. This is obtained by dividing the buffered oscillator output of IC7 (6.6MHz) by 4 in IC9.

When receiving (or transmitting) an LSB signal, a 1647kHz local oscillator is required. This is obtained from IC10c and crystal Z3. A high on J3 pin 11 enables IC9 and disables IC10c giving 1650kHz (USB). A low on J3 pin 11 gives 1647kHz.

A tune output is provided from IC10a to the gate of source follower V16 and V17 when the tune line J3 pin 12 is low. The DC component of the tune output holds V26 conducting which switches V23 to open circuit, disconnecting the crystal filter from V16 and V17.

4.4.6 Clarifier

Operation of the clarifier control varies the frequency of VCO2 in 10Hz steps. This is achieved by varying both the VCO and reference frequency dividers according to a 'look-up' table in the transceiver's operating system. Thus the phase comparison frequency is not constant but varies from 1.1 to 2.0kHz.

The limits of the clarifier are 0.001% (± 10 ppm) of carrier frequency. Consequently the number of steps are also a function of the carrier frequency. At low frequencies dummy steps are inserted to increase the time the clarifier takes to go from end to end of its range.

An audible indication is given when the clarifier reaches its upper or lower limit. The clarifier automatically resets to mid frequency when the channel is changed.

4.5 Microprocessor Controller PCB (04-03031)

Circuits on the Microprocessor Controller PCB govern the functions of the transceiver including the operator controls and displays. The microcontroller on the board accepts inputs from within the transceiver and from the operator's controls. Under control of the program in the EPROM, it outputs the data necessary to achieve the appropriate response to input signals.

The microcontroller is connected with other devices on the board by three buses: a conventional microcontroller bus (8-bit data, 16 bit address) and two 'Inter-Integrated Circuit' (I²C) buses.

4.5.1 Microcontroller Bus

The microcontroller (IC11) is an 80C32 which is a member of the Intel 8051 8-bit microcontroller family. It has 128 bytes of internal RAM, no internal program memory, two counter/timers, two external interrupt sources and an internal clock oscillator.

The microcontroller operates in a conventional 8-bit data, 16-bit address configuration. To minimise the pin count, the low-order address bits are multiplexed with the data on pins 32 to 39 onto a common 8-bit bus. IC13 is used to latch the low order address bits to facilitate access to the external non-multiplexed devices. The address latch enable (ALE) signal (IC11 pin 30) indicates to the latch when the address is present on the bus. The high order address bits are provided directly on pins 21 to 28 of IC11.

The following external devices are connected to the bus:

- IC14—an EPROM containing radio control software. The microcontroller selects the EPROM via the program store enable (SE) signal (pin 29).
- IC10—a RAM device supplementing the microcontroller's internal RAM. It is selected via the Read or Write signals (IC11 pins 16 and 17) in conjunction with address line 15 (IC11 pin 28).
- IC12—a triple tone generator used to generate all audio tones required in the transceiver, e.g. emergency call tones, error beeps, etc. It is selected via the Read and Write signals in the same way as IC10 but in conjunction with address line 14 (IC11 pin 27).

Three audio tone outputs are generated within IC12 by dividing the clock inputs on pins 18, 15 and 9 by factors programmed into its data input. The clock input signal is derived from the microcontroller's ALE output. During those cycles when the microcontroller does not generate the ALE, the Read or Write signals are inserted via D3 and D4 to maintain a steady square wave signal.

4.5.2 Internal I²C Bus

The internal I²C bus consists of three lines: data, clock, interrupt and enable. The data and clock lines operate as an I²C bus; the data line carries data and address bits serially, with their transfer being synchronised by transitions on the clock line.

Data, clock and interrupt lines connect the microcontroller with 8-bit I/O IC's, IC3 and IC4. Each 8 bit I/O IC converts parallel data on its eight ports to serial data for application to the bus and conversely, converts serial data from the bus to parallel data on its ports. Each IC has a separate address set by the connections to its address pins (1, 2 and 3). When a data transfer is required, the microcontroller first outputs on the data line the address bits of the required IC and follows this with a Read/Write command. Data is then read from, or written to, the selected 8-bit IC.

When an input to any of the ports changes, the IC sends an interrupt to the microcontroller. As all the interrupts are connected to a single input, the microcontroller must interrogate each IC in turn until the changed data is read. When this is done, the IC removes the interrupt and the microcontroller can resume its other operations.

Part of IC3 is used for connection to selective call options. The remainder of IC3 and all of IC4 carry data to and from various functions within the transceiver.

The clock and data lines of the internal bus also connect the microcontroller with IC5 and IC15 which operate as I²C bus receivers. Under control of the data, each IC accepts serial bits from the bus. A set of bits consists of two address bits and sixteen data bits. On completion of the transfer of a set, the IC to which the set is addressed latches the data bits as 16-bit parallel data on its outputs. These two IC's provide 32 open drain outputs to various circuits throughout the transceiver.

The microcontroller is connected via the data and clock lines to the non-volatile memory, IC6. This stores the channel selection, volume control, clarifier and scan channel settings. When power is switched off, the data is retained in the memory by battery G1. Drain on the battery is very low, therefore the battery life is limited mainly by its shelf life i.e. approximately 10 years. A discharged battery will cause the channel, volume, clarifier and scan channel settings to require resetting each time the transceiver is switched on, but will allow normal operation of all other facilities.

Also connected to the microcontroller via the bus, is an EEPROM, IC16. This provides the non-volatile memory to store customer channel information and data entered on the front panel pads.

The clock and data lines are also connected to the synthesizer circuits on the RF, Mixer and Dual Synthesizer PCB via J4. Data for setting the two synthesizer frequencies is sent over the data lines and on completion of the transfer, the synthesizer latch line is pulsed.

The clock and data lines are also taken to connector P1 for application to I/O ports in the Selective Calling PCB when this is fitted. Provision is made for all four lines of the bus to be connected via P3 to further I/O IC's if required.

4.5.3 External Bus

A second three-line bus is provided for connection to 8-bit I/O IC's and 16-bit open-drain output IC's on the Display PCB in the Extended Control Head. All three lines are buffered in IC1 to allow for the longer lines to the Extended Control Head and to protect the microcontroller. Since the buffers can carry data in only one direction, data read from the control panels is buffered in IC1 and returned to a separate input of the microcontroller.

The interrupt line from the Display PCB is ORed with the internal bus interrupt by diode D5 and is also taken via two buffers in IC1 to a separate input of the microcontroller. By this means, the microcontroller can detect whether an interrupt has come from the internal or external bus.

4.5.4 RS232 Port

The microcontroller IC11, pin 10 receives serial data from the RS232 port P4, pin 1. Transmitted data from IC11, pin 11 is buffered by transistor, V5 and voltage limited by resistor, R37 before being sent out via the RS232 port P4, pin 2.

4.5.5 Reset and Watchdog Circuit

The microcontroller is reset by a +5V level on pin 9. This may be applied in three ways: by applying power to the unit, by the low voltage detection circuit or by the watchdog circuit.

When power is switched on, the reset input is held high, thus resetting the microcontroller ready for initial operation.

If the supply voltage (A rail) falls below 8 volts, IC7 output goes low. This switches on V3 which holds the microcontroller in the reset condition until the supply voltage is restored.

Schmitt Trigger IC8a, together with R9 and C4, form an oscillator with a period of approximately 600ms. However during normal operation, the microcontroller outputs a positive pulse from pin 14 at regular intervals of less than 600ms. Each pulse switches on V1 which discharges C4 thus preventing the oscillator from starting. Should the microcontroller operation fail, or be affected by abnormal inputs, the pulses cease thus allowing the oscillator to start. Each negative excursion of the oscillator output will switch on V3, resetting the microcontroller. The reset will therefore be applied at regular intervals until normal operation is resumed.

4.6 Motherboard and Chassis (04-02453)

The Motherboard interconnects circuit boards which are mounted directly on it and provides connections to other assemblies mounted on the chassis. It also provides connections which link these assemblies to external connectors. In addition the board carries components associated with these interconnections and with the power supplies and their switching.

4.6.1 Power Supplies

The Motherboard contains relays with their switching transistors associated with the power supplies as described in Section 4.1.

The board also contains two voltage regulators, IC1 and IC2. These provide stabilised DC supplies of 10V and 5V respectively from the A battery supply. The 10V and 5V supplies are used throughout the transceiver.

4.6.2 Antenna Control Facility

The Antenna control socket J201 on the rear panel of the transceiver provides an interface for various antenna tuning systems. The socket is connected to P201 on the Motherboard. Interconnections within the Motherboard provide access to the 12V supply, 4-bit binary-coded data indicating the channel selected, and various other outputs for use by automatic tuning systems. On entering the board the lines are filtered to prevent RF picked up on the external cable, from interfering with the operation of the transceiver. The table in Section 1.2.4 shows the pin connections and the signal level of each function.

4.6.3 Extended or Remote Control

The Remote Control plug (P502) on the rear panel of the transceiver provides an interface for extended or remote control equipment. When fitted the plug is connected to the Remote Control and Filter PCB mounted on the Motherboard. Transceivers manufactured for extended or remote control include these components.

The extended or remote control lines carry the services shown on the circuit diagram. Components on the Remote Control and Filter PCB prevent RF picked up on the external cable, from interfering with the operation of the transceiver.

The table in Section 1.2.4 shows the pin connections and levels of each function.

4.6.4 External Microphone Audio Clamp

The audio input from the Remote Control connector at pin 11 P502 is connected, via C102, R103, R101 and C101 to the Aux Compressor input of the Audio and IF 1650kHz PCB. FET V101 is normally biased on via R104 and R105, thus clamping the microphone input to ground. Operation of the remote PTT switch grounds the junction of R104 and R105 removing the bias from V101. This allows the microphone input to be applied to the compressor input.

4.6.5 AGC Dump Circuit

The synthesizer latch from the Microcontroller Controller PCB pin 1 P10 is used to turn on V4 thus grounding the AGC line on the Audio and IF 1650kHz PCB via R23. This discharges the reservoir capacitor in the AGC circuit so that the receiver has maximum gain immediately after a frequency change. This is particularly important when in the scan mode.

4.7 9480 Front Panel Display PCB, LCD (04-03045)

The LCD on the board has twenty digits and two enunciators which allow it display the channel number and transmit and receive frequencies of the currently selected channel. In addition it can display the identification number of a called or calling selective call station. The LCD is driven by IC4. The display data is applied to the driver via the I²C bus. The drive mode is 1:4 multiplexed with 1/3 bias.

The viewing angle is preset by adjustment of R12. This sets the voltage applied to the non-inverting input of IC1a while the voltage at the junction of R10 and D1 is applied to the inverting input. The output of IC1a is proportional to the difference between the two voltages. The temperature coefficient of D1 applies temperature compensation tending to keep the set viewing angle constant over a wide range of temperatures.

R12 is normally set during manufacture for viewing at right angles to the face of the panel. It can be adjusted for viewing angles above or below if required.

Six incandescent lamps, H1 to H6, are mounted behind the LCD to provide back-lighting so that the display can be read in low ambient light. Back-lighting for the 24 matrix switches is supplied by a LED mounted behind each matrix switch.

Common connections of the LED indicators H8 and H9 are taken to a positive supply regulated by IC2. The indicators are lit by grounding the appropriate connection via the 16-output driver IC3.

The Tx indicator LED is lit by grounding its cathode via a transistor on the PA and Filter PCB.

The current sinking provided in IC3 for the indicator LEDs H8 and H9, can be varied by operation of the DIM pad on the front panel. Any indicators lit will be at full brightness when the transceiver is first switched on.

The dimming operation is also applied to the LCD back lighting via IC2 pin 4. Normally high impedance (tristate), this impedance goes low in the dimmed condition. This is applied to the base of V2 to override the hold-on voltage applied via R6. With the transistor switched off the current for H1 to H6 is drawn through R30 and R31 thus reducing the brightness of the LCD back-lighting. The panel back-lighting is not controlled and remains at full brightness at all times.

A moveable jumper link closes either Link E for extended control, or Link F for front panel control. Closing the appropriate link modifies the address of the I/O port IC5 so that the microprocessor can recognise the type of control in use.

Link 1 is used in programming the transceiver options (refer to the Operator's Handbook) and link 2 is for possible further use.

Switches on the panel overlay (substrate) form a 4 x 6 matrix. The row and column connections are taken to the Display PCB. (a table listing the switch functions and the corresponding connections is given in Section 6.2.3). In the Display PCB the row connections are polled by the microprocessor via IC3, by taking them to 0V one at a time. Three of the four lines are taken to 0V via open collector drivers V4, V5, and V6. A switch operation is detected by the corresponding column connection to the 8-bit I/O port IC5 going to 0V. Data indicating the switch closure is encoded and returned via the bus, to the microprocessor.

4.8 Control Head (04-03038)

Overlays on the front panel of the control head contain sealed tactile membrane switches. A liquid crystal display (LCD) and light emitting diode (LED) indicators on a board behind the panel show through the appropriate part of the overlay when activated. Circuits on the board interface with the microprocessor in the transceiver to drive the displays and indicators, and to decode the operations of the front panel switches.

Surface mounted components are used in the display PCB. For removal and replacement of these components it is essential to use tools specifically designed for the purpose. Repairs to the board should not be attempted unless the appropriate tools are available.

The LCD, H14, has twenty digits and two enunciator's which allow it to display the channel number and the transmit and receive frequencies of the currently selected channel. In addition it can display the identification number of a called or calling selective call station. The LCD is driven by IC5. The display data is applied to the driver via an I²C bus. The drive mode is 1:4 multiplexed with 1/3 bias. The driver is powered by a separate supply derived from the A rail by diode D7 and zener diode V7.

The viewing angle is preset by the adjustment of R34. This sets the voltage applied to the non-inverting input of IC4a, while the voltage at the junction of R32 and D6 is applied to the inverting input. The output of IC4a is proportional to the difference between the two voltages. The temperature coefficient of D6 applies temperature compensation tending to keep the set viewing angle constant over a wide range of temperatures.

R34 is normally set during manufacture for viewing at right angles to the face of the panel. It can be adjusted for viewing angles above or below if required through the hole in the bottom of the case.

Six incandescent lamps, H1 to H6 are behind the LCD. These provide back lighting so that the LCD can be read in low ambient light. Backlighting for the 24 matrix switches is supplied by a LED mounted behind each matrix switch.

Common connections of the LED indicators H12 and H13 are taken to a positive supply derived from the A rail and regulated by IC1. The indicators are lit by grounding the appropriate connection via the 16-output driver IC2.

The Tx indicator LED, H7, is lit by grounding its cathode via a transistor on the PA and Filter PCB.

The current sinking provided by IC2 for the indicator LEDs H12 and H13 on the front panel can be varied by the operation of the **DIM** pad on the front panel. Any indicators lit will be at full brightness when the transceiver is first switched on.

The dimming operation is also applied to the LCD back lighting via IC2 pin 4. Normally high impedance (tristate), this output goes low in the dimmed condition. This is applied to the base of V1 to override the hold-on voltage applied via R1. With the transistor switched off the current for H1 to H6 is drawn through R3 and R4 thus reducing the brightness of the LCD back lighting. The panel back lighting is not controlled and remains at full brightness at all times.

Link 1 is used in programming the transceiver options (Refer to the Operator's Handbook). Link 2 is for possible future use.

Switches on the panel overlay (substrate) form a 4 x 6 matrix. The row and column connections are taken to the Display PCB. (A table listing the switch functions and the corresponding connections is given in Section 6.2.3.) In the Display PCB the row connections are polled by the microprocessor, via IC2, taking them to 0V one at a time. (Three of the four lines are taken to 0V via open collector drivers V2, V3 and V4.) A switch operation is detected by the corresponding column connection to the 8-bit I/O port, IC3, going to 0V. Data indicating the switch closure is encoded and returned, via the bus, to the microprocessor.

To compensate for the long lines connecting the Control Head to the transceiver, on entering the board each line is filtered to prevent interference picked up on the lines from affecting the operation of the head. The Clock line is also buffered by a small amplifier formed by V8 and V9.

The A rail from the transceiver is used by various circuits on the board and is also applied to a regulator, IC6, to provide the +5V supply for other circuits within the board.

An amplifier formed by IC4b and its associated components amplifies the microphone input to a suitable level for application to the lines. V5 on the input to the amplifier operates as a clamp in the same way as V7 on the Audio and IF 1650kHz PCB. This circuit is powered by a separate supply derived from the A rail by zener diode V6.

4.9 PA and Filters (04-02452)

4.9.1 PTT Control

The driver and output stages are permanently connected to the supply voltage when the Power On relay K7 is energised. Power to the rest of the PA and the bias for the driver and output stages is switched by V14 when the PTT input (D rail, P1 pin 2) goes high causing pin 10 of IC1 to sink base current from V14 through the antenna change-over relay K6 coil. In transmit, the input stage V7 and V9 becomes active when its emitter circuit is connected to ground on the C rail through D12 on the RF Mixer and Dual Synthesizer PCB (04-02450).

4.9.2 Gain Control Stage

The RF input to the PA is terminated in R21 and drives the common base long tailed pair V7 and V9 through R29 and R30 in parallel for signal currents.

The input voltage is also buffered by V8 and additional input current fed to V7 and V9 through L17, C66 and R32 to compensate for PA high frequency gain roll-off.

The gain of V9 is controlled by the ratio of emitter DC currents in V7 and V9. The RF input current is split between the emitters of V7 and V9 in inverse proportion to their input impedance. The gain of V9 is therefore reduced when the ALC increases the current in V7.

4.9.3 Pre-Driver Stages

The output current of V9 drives the collector-base feedback stage V10 which is direct coupled to the transformer feedback stage V12. High frequency peaking is provided by C72, D11 and D12 provide temperature compensation for V10 and V12.

4.9.4 Driver Stage

The driver stage V16 and V17 is voltage driven from the secondary of T2 and with emitter resistors R52 to R55 provides a current drive to the output stage. L20, C78 and R56 provide damping for a harmonic resonance in T3.

The bias for V16 and V17 is provided by the current of the pre-driver stages passing through the diode-connected transistor V13. The bias may be increased by R46, the current through R46 causing a voltage drop across R47 in addition to the base-emitter voltage of V13. The current in V16 and V17 may be measured at the link in the DC feed to T3.

4.9.5 Output Stage and Bias Regulator

The output stage V18 and V19 is current fed from the secondary of T3 with low frequency current feedback through R58 and R59 from a winding on the output transformer T4. C93, C94 with C116 and C81 with C82 provide frequency compensation for T3 and T4 respectively.

The balanced output auto transformer also contains a balun winding so that one output can be AC coupled to ground and the other output capacitively coupled to the load.

The bias regulator (V11 and V15) provides a constant voltage to the bases of V18 and V19. V11 and V15 form a feedback voltage regulator, the output voltage being the base-emitter voltage of V11. R76 and V23 cause the bias to increase at low supply voltage (10V approx) to reduce intermodulation distortion.

V11 is mounted on the PA heatsink and provides temperature compensation based on heatsink temperature.

When low power is selected, V21 is turned on by V20 collector going high. This increases the bias voltage via R71 and therefore the bias current in V16 and V17. This is required to improve the intermodulation distortion at low power.

4.9.6 Output Filters and Control

The output of the PA is passed through one of six low-pass filters to remove harmonics generated in the PA. These filters are relay selected (K1 to K5 and K8) by the band lines generated by the microprocessor controller and buffered by IC1.

4.9.7 ALC Control

ALC control is provided from the following sources:

- Forward power
- Reflected power
- Battery voltage
- Low Power control
- Heatsink over-temperature
- Output stage collector swing.

The ALC control inputs are applied to IC2a which provides a fast attack, slow decay control voltage to the base of V7. In the absence of any ALC input, the negative input of IC2a is held at 3.9V by voltage divider R16, R17 and R19 and the voltage on C59 and V7 base is held at a similar level. V7 is cut off and V9 then operates at maximum gain.

The R16, R17 and R19 voltage divider chain is used to control ALC action for heatsink temperature. When the heatsink temperature exceeds 80°C, PTC resistor R16 rapidly increases in value, reducing the ALC threshold level and reducing the power output such that the heatsink does not rise above 90°C.

The output voltage from the RF bridge T1, L1, R2, R3, C1 and C2 is rectified by D1 as forward power and by D2 as reflected power. The forward power output is divided by R9, R10 and R11 and ORed by D8 with the output of the reflected power detector into the positive input of the ALC level comparator IC2a. The power output is set by R10.

The output voltage of the forward power detector is averaged by R68, C92 and ORed into the ALC comparator. The value of R68 is chosen so that a average forward power of 60W will provide ALC control.

When the DC supply drops below 12.5V, V5 starts to conduct, increasing the voltage across R11. This effectively raises the forward power detector level, resulting in increased ALC, reducing the output power.

A low on the LO PWR input (P3 pins 1 and 2) will cause V20 to conduct also raising the current in R11 and reducing the power output.

The peak positive swings of the PA output transistors V18 and V19 are rectified by D13 and D14, divided by R61 and R62 and buffered by V22 before being ORed into the ALC comparator. Thus excessive swings of the PA collector voltage reduces the output power to prevent damage to the PA transistors. The output from V22 is also applied to one input of IC2b where it is compared with the forward power to the antenna. If the forward power is very low (or absent) indicating a fault in the antenna circuit, the output power is reduced to prevent damage to the PA transistors.

4.9.8 Transmit Indicator

The forward power voltage developed by D1 is divided and applied to V4 base producing a current in V4 proportional to power output to illuminate the Tx LED indicator.

4.10 Selective Calling (04-02250)

Selective Calls are sent as FSK signals using 1700Hz and 1870Hz at 100 Baud.

4.10.1 Selective Calling

The call is initiated by pressing the Call pad on the front panel. On recognising the request for a call, the microcontroller first checks that the channel selected is one on which selective calls are programmed. If it is, the microcontroller generates the required codes including the Called Address and Self Ident codes set in the transceiver. The settings of each pair of switches are encoded by the corresponding 8-bit I/O port IC4, IC5, IC6 and IC7 and sent to the microcontroller as serial data when the appropriate port is addressed.

The microcontroller (04-03031) applies the generated code to the tone generator IC12. The resulting FSK tones from IC12 pin 10 are filtered by C20 and R21 and applied via J3 pin 9 to the auxiliary compressor input of the Audio and IF 1650kHz PCB. The FSK tones are also attenuated by R23 and applied as a side tone via J3 pin 10 to the auxiliary LS input of the Audio and IF 1650kHz PCB. At the same time, the microcontroller generates a PTT signal so that the FSK tones are transmitted. On completion of the coded transmission, the PTT signal is removed and the transceiver returns to the receive mode.

4.10.2 Selective Call Detection

The received audio is applied via J1 pin 2 to a band-pass filter formed by IC1a, IC1b and their associated components. The filter has a 3dB bandwidth of 400Hz centred on 1775Hz. The filter output passes to the phase locked loop IC2.

The voltage controlled oscillator frequency in IC2 is set by C10, R15 and R16. In the absence of FSK signals, the lock detect output from pin 6 will fluctuate and the resulting charge on C8 will be less than half the supply voltage. This is applied via R11 to the comparator input pin 8, resulting in a low output from pin 7. Some of the output is fed back to the input via R13 to provide hysteresis. The comparator output is taken via D3 to the non-inverting input of IC3b. This results in a low output from IC3b which effectively cuts off V1. When FSK signals are detected the lock detect output goes high. The resulting high comparator output reverse biases D3, enabling IC3b.

When FSK signals are applied, the data appears on the loop phase detector output pin 11. This is applied to the data filter IC3a and associated components. This is a low-pass filter at approximately 80Hz which passes the resulting data to the input of IC3b. The data filter output is also peak rectified by D1, D2, C17 and C18. The voltages on the two capacitors are summed at the inverting input of IC3b to give a reference voltage equal to the mean frequency of the FSK signal. Consequently, IC3b regenerates the data, ignoring any frequency shift in the RF path.

Demodulated FSK signals are applied via P2 pin 6 to the Microprocessor Controller PCB (04-02451) on P1 pin 1. From there they are applied to the microcontroller which decodes the addresses contained in the data. If the selective call is found to be addressed to the transceiver, the microcontroller sends a revertive message to the caller. At the same time the controller gives outputs which activate the necessary audio and visual indications that a selective call has been received.

If the transceiver PTT is not pressed, on completion of the audio alarm period, the microprocessor applies a low on J1 pin 6 (04-02451). This is fed to J1 pin 4 (on 04-02250) which, through V2 and V3, energises relay K1 for 2 minutes, operating an external alarm (if fitted). K1.1 contacts are rated at 50V 1A. Operation of the PTT cancels the alarm.

Refer to section 7.3.15 for setting up instructions.

4.11 Options

Options may be fitted to the transceivers as described in the sections which follow.

4.11.1 LU—Switched LSB Operation

Individual channels can be programmed to operate on upper and lower sidebands; the choice being made and indicated at the USB/LSB pad on the front panel. For LSB operation, a 1647kHz crystal is fitted in the Z3 location on the RF Mixer and Dual Synthesizer PCB 0803740. Adjustment is carried out as described in section 7.3.11 of this manual. Selection and operation of the oscillator circuit is described in Section 4.4.5. The required facilities are programmed into the EPROM.

4.11.2 AD—Antenna Driver

Option AD enables Type 9313/9480 Series Transceivers to be used with Codan Automatic Tuning Whip Antennas Type 8558 while still retaining the capability of using antennas with preset tuning.

The option consists of a single PCB (Antenna Driver PCB Assembly (08-04285)). The PCB plugs into J202 on the Mother Board of the transceiver after disconnecting the ribbon cable previously connected to this plug. The ribbon cable, which carries the antenna control facility to J201 on the rear panel of the transceiver, is then connected to a plug (P1) on the Antenna Driver PCB. Two further connections are made: J2 of the Antenna Driver PCB is connected to J1 of the Microprocessor Board and J3 of the Antenna Driver PCB is connected to P4 on the PA and Filter Board.

(Refer to Circuit Diagram 04-02724)

The inclusion of the option is indicated to the microprocessor in the transceiver when the IO device, IC3, on the board responds to being polled, on the I²C bus to its Clock and Data lines, when the transceiver is switched on.

When the Tune pad on the transceiver control panel is pressed the microprocessor causes some RF, at the required transmission frequency, to be applied to the antenna. At the same time the microprocessor prepares the IO device, IC3, to respond to the VSWR measurement. Voltages proportional to the forward and reflected power at the antenna are applied from the PA and Filter Board to J3 of the Antenna Driver PCB.

The forward power is compared in IC4a with a preset voltage to establish whether the RF is adequate for the VSWR measurement to be made. If the voltage proportional to the forward power exceeds the preset voltage the output of IC4a goes to the low logic level to indicate ADEQUATE. The result of the comparison is passed, via IC3, to the microprocessor.

The microprocessor has recorded the last used frequency and is given the new frequency and it uses this information to drive the antenna tuning motor in the appropriate direction to improve the VSWR. It does this by sending data to IC3 to switch on one of the transistors, V4, V6, V8 or V10. These switch on the corresponding Darlington transistors V5, V7, V9 or V11. The antenna motor is a 4-phase, uni-polar stepper motor and is driven in the wave mode (i.e. one phase at a time). +12V is applied to one end of all four windings of the motor and, when switched on, each Darlington transistor grounds the other end of one winding.

The forward and reflected power are compared in IC4b, IC5a and IC5b. One input to each of these comparators is from a potential divider on the forward power voltage, while the other input to each is the reflected power voltage. The potential divider values are such that the output of IC4b will go low when the VSWR is less than 3:1, IC5a will go low when it is less than 2:1 and IC5b will go low when it is less than 1.5:1.

The outputs of the comparators are sent to the microprocessor via IC3 and, as the antenna tuning changes, the microprocessor detects any improvement in the VSWR. As soon an improvement is detected, provided the RF has been found to be adequate, the microprocessor stops the tuning and a positive voltage is applied to the Load input to the board (J1 pin 7). This switches on V2 so that the Load output (P1 pin 4) goes low.

The Load output is applied to a circuit in the antenna which controls a 2-coil latching type relay (K2 on the Auto Antenna PCB). The low level on the Load input to the antenna causes the load presented by the antenna to be 22 ohms, while a high level on the input causes the load to be 35 ohms. The microprocessor assesses whether the change of load has improved the VSWR.

The microprocessor continues the process of changing the antenna tuning and the load until either the VSWR is found to be less than 1.5:1 or no further improvement can be made. Provided the final VSWR is less than 3:1 a Pass indication is given. If it is greater than 3:1, or the RF is inadequate, a Fail indication is given.

On completion of the tune operation a positive voltage is applied to the Brake input (J1 pin 6). This switches on V1 which bypasses R1 to lower the output of IC1 to approximately 1.3V. This is applied to the antenna motor windings. At the same time V5 is switched on so that a small current (approximately 120mA) is passed through one motor winding. This has a braking effect so that the antenna tuning does not change with vibration.

Power for the comparator circuit is derived from the A rail by IC2. This remains operative on completion of the tune operation so that any change in the VSWR will still be detected. If a transceiver fitted with the option is used with a non-tunable antenna an excessive VSWR will cause an "Untuned" indication which cannot be corrected. The reflected power voltage, via R10, is, therefore, taken to the disable line (P1 pin 5). When the transceiver is used with a non-tunable antenna, pin 3 of the rear panel D connector (J201) can be linked to pin 14 to disable the comparator so that no "Untuned" indication is given.

When the transceiver Scan mode is selected, the \overline{SCAN} input (J1 pin 9) is taken low to switch on transistor V3. The collector current of the transistor energises relay K1 in the antenna. This switches into circuit a wide-band amplifier in the antenna which provides good reception over the entire range of the antenna.

To retain the ability to use a transceiver fitted with the option with a pretuned antenna, the lines from the Microprocessor Controller Board carrying the BCD data for presetting the antenna are carried through the option board to the rear panel D connector (J201).



5

Operating Instructions

Refer to the relevant Operator's Instructions.



6

Maintenance

6.1 General

6.1.1 CMOS Devices

A number of Complementary Metal Oxide Semiconductor (CMOS) devices are used in the transceiver. Although protection is built into most of these, their extremely high open-circuit impedance makes them susceptible to damage from static charges. Care must therefore be used when shipping and handling the devices and in servicing equipment in which they are installed. The following precautions should be observed:

- **Packaging**—Replacement CMOS devices are supplied in special conductive packaging. They should be left in this packaging until required for use.
- **Switch off**—Ensure that supplies are switched off before disconnecting or reconnecting any connections between circuit boards and the remainder of the transceiver.
- **Handling**—Handling of circuit boards and particularly touching any conductive parts should be kept to a minimum.
- **Grounding**—Anything connected to or touching the circuit board tracks should be grounded. Observe the following:
 - Test equipment connected to a board should be grounded via its mains lead.
 - Static charges which may build up on the person can be discharged by touching a grounded metal surface with both hands. This should be done before, and at frequent intervals while, working on circuit boards.
 - Wearing a suitably grounded conductive wrist strap will minimise the static build up on the person.

6.1.2 Circuit Boards

When servicing printed circuit boards the following should be observed:

- **Excessive heat**—Excessive heat may lift the track from circuit boards, causing serious damage. Avoid the use of high powered soldering irons: a 60W maximum iron, preferably temperature controlled at approximately 370°C, is sufficient for most tasks. A slightly higher temperature (425°C) iron may be required for heavier components such as PA transistors. Apply the iron only long enough to unsolder an existing joint or to solder a new one.
- **Unsoldering**—When unsoldering use a solder-sucker or Solderwick to remove solder. **DO NOT USE SHARP METAL TOOLS SUCH AS SCREWDRIVERS OR TWIST DRILLS AS THESE WILL DAMAGE THE PRINTED CIRCUIT TRACK.**

- Component substitution—Avoid unnecessary component substitution as this may damage the component, the circuit track or adjacent components.
- Component replacement—When a component is diagnosed as defective, or the fault cannot be diagnosed in any other way than by substitution, observe the following when installing the replacement:
 - Axial leads—Components with axial leads, e.g. resistors and tubular capacitors, can often be replaced without unsoldering the joints on the boards. The defective component can be removed by clipping its leads close to the component leaving the leads soldered to the board. These leads should be straightened so that the leads of the replacement can be wrapped around them and soldered. After soldering the excess lead should be clipped off.
 - Remove solder—When a component has been unsoldered from the board ensure the holes are clear of solder before inserting the leads of the replacement. **ON NO ACCOUNT FORCE THE LEADS THROUGH THE HOLES AS THIS WILL DAMAGE THE CIRCUIT TRACK PARTICULARLY WHERE PLATED THROUGH HOLES ARE USED.**
 - Observe orientation—When replacing diodes, transistors, electrolytic capacitors or integrated circuits, before removing the defective component, observe any marking indicating polarity or orientation. It is essential that these types of components are installed with the correct connections. If necessary consult the manufacturer's data for indications of the polarity of diodes or capacitors and connectors of transistors.
 - Heat sinking—Whenever possible use long-nosed pliers or some other form of heat sinking on the leads of heat sensitive components while soldering them to the board.
 - Thermal conduction—When replacing transistors which are mounted on heat sinks ensure good thermal conduction between the heat sink and the replacement by cleaning the mounting surfaces and recoating them with a thermal conduction compound such as Jermyn Thermaflow A30.
- Track repair—Broken or burned sections of printed circuit track can be repaired by bridging the damaged section with tinned copper wire. The section where the repair is to be made must be cleaned observing the precautions outlined above before soldering.

- Integrated circuit replacement—In some cases it is possible to desolder and remove components from the board without damage to the component or the board. However, integrated circuits with a large number of connections, mounted on double-sided circuit boards with plated-through holes are almost impossible to remove intact, and the operation is likely to damage the circuit boards. To replace these components their leads must be cut individually until the body of the component can be removed from the board. Individual leads must then be unsoldered and removed. Excess solder must be removed before inserting the replacement component.

6.1.3 Transmitter Precautions

When making measurements of the low level stages of the exciter it is advisable to remove the drive to the PA stages by disconnecting P2 on the PA and filter PCB. The supply voltage is applied to the PA at all times when the transceiver is switched on. Due care should be exercised when connecting probes.

6.1.4 Probe Precautions

The following should be observed when connecting CRO probes to the transceiver:

- When connecting probes to the PA assembly, the earth clip lead should be wound around the body of the probe so that the earth clip just reaches the probe tip. This reduces stray pick-up.
- The earth clip should be connected to the ground plane immediately adjacent to the point of measurement to which the probe tip is connected.
- It is not advisable to connect two probes at the same time, particularly when one is earthed to the PA ground plane and the other is earthed to the chassis, as this may cause earth loop problems.
- Probes should be connected after power has been applied to the transceiver and the test equipment. The earth connection should be made first and disconnected last.

6.1.5 Surface Mounted Components

Surface mounted components are used on some printed circuit boards. For removal and replacement of these components it is essential to use tools specifically designed for the purpose. Repairs to these boards should not be attempted unless the appropriate tools are available.

6.2 Fault Diagnosis

6.2.1 General

The removal and substitution of components may damage the components and/or the printed circuit boards. In some cases it is impossible to remove components without destroying them. It is important therefore to carry out as much fault diagnosis as possible with components in situ. Specific tests are described later in this section. The general points which follow should also be of assistance:

- Spare boards—If spare boards are held in stock, they may be substituted in order to positively localise the fault to one board.
- Transistor tests (static)—Transistor failures are most often due to open-circuit base-emitter or base-collector junctions, or a short circuit between emitter and collector.

These types of faults can often be detected without removing the transistor, using the ohms range of a multimeter. The two junctions should both give the appearance of a diode, i.e. high resistance with the multimeter leads one way round and low resistance when the leads are reversed. (Polarity depends on whether a PNP or NPN transistor is being tested.) Resistance between collector and emitter should be high with the multimeter leads either way round. The circuit diagram should be examined for parallel paths before a transistor failing these tests is removed.

- Transistor tests (dynamic)—Some transistor faults can be diagnosed by measuring voltages within the circuit. One of the most significant voltage measurements is the base-emitter voltage. The polarity of this will depend on the type of the transistor (PNP or NPN). A base emitter voltage between 0.5 and 0.9V should be measured on a forward-biased base-emitter junction.

With its base emitter junction forward biased the transistor should conduct. Some indication of satisfactory operation of the transistor can be obtained by measuring the voltage drop across its collector or emitter resistor and short circuiting its base to the emitter. The short circuit will remove the forward bias cutting off the transistor so that the voltage across the resistor will be considerably reduced.

- Integrated circuits—If there appears to be no output from an integrated circuit, before replacing the device, it should be ascertained whether the fault is due to the IC or its load. As a general rule, if changes in input cause absolutely no changes in the corresponding output the IC should be suspected. If, however, even a very small change in output can be detected the load is more likely to be the cause. Depending upon the circuit, further tests should be made by disconnecting resistors, capacitors, etc to verify this diagnosis before removing the IC.

6.2.2 Voltage Measurement

The circuit diagrams and the relevant circuit notes give voltages at various points under the various conditions to enable the faulty section of the transceiver to be located.

The parameters listed below should always be checked first:

1. Supply voltages on the Motherboard and Chassis:
 - Main B rail regulator (IC1) $10V \pm 0.2V$
 - C rail, B rail voltage in Receive, 0V in Transmit,
 - D rail, 0V in Receive, B rail voltage in Transmit,
 - Main 5V regulator (IC2) $5V \pm 0.4V$.
2. Supply voltages on the RF Mixer and Dual Synthesizer PCB:
 - +5V supply (IC4) $5V \pm 0.4V$
 - +26V supply (TP7) $26V \pm 1V$
 - +9V supply (V1 emitter) $9V \pm 0.25V$

6.2.3 Front Panel Controls

Lack of response to controls may be due to malfunction of one or more of the sealed membrane switches. These can be tested by disconnecting the connector from the control head switches at P1 on the Control Head PCB and testing between pins of the connector as shown in the table below. A meter connected between each pair of pins in turn should indicate open circuit with the corresponding switch not operated and continuity (less than 100Ω) when the switch is pressed.

Front Panel Switch Test

Connector Pin	9313	9480
1 - 2	Mute	Mute
1 - 4	1	1
1 - 5	3	3
1 - 7	2	2
1 - 8	Power On/Off	Power On/Off.
1 - 10	—	USB/LSB
3 - 2	Scan	Scan
3 - 4	4	4
3 - 5	6	6
3 - 7	5	5
3 - 8	RFDS Call	Emgcy
3 - 10	Tune	Tune
6 - 2	Channel (up)	Channel (up)
6 - 4	7	7
6 - 5	9	9
6 - 7	8	8
6 - 8	Clarifier (up)	Clarifier (up)
6 - 10	Volume (up)	Volume (up)
9 - 2	Channel (down)	Channel (down)
9 - 4	B'con (Enter)	Enter
9 - 5	Call	Call
9 - 7	0	0 (B'con)
9 - 8	Clarifier (down)	Clarifier (down)
9 - 10	Volume (down)	Volume (down)

6.2.4 Logic Levels

If the switches are found to be satisfactory, the lack of response may be caused by faults in the main microprocessor or the associated data buses. If this type of fault is encountered, the I²C bus lines should be monitored with an oscilloscope. This can be done at J1 pins 1 to 4 and P3 pins 1 to 3 on the Microprocessor Controller PCB. Operation of any of the front panel controls should cause the exchange of data via the bus lines. This should be seen on the oscilloscope as rapidly changing levels between +5 and 0V. No data on a line, or failure of the levels to change cleanly should be investigated further. Failure may be due to an IC or its load. Refer to 6.2.1. Ensure that the terminations of all interconnecting ribbon cables are correctly mated and aligned.

6.2.5 No Reception

If no signal is received, after confirming the supply voltages described in 6.2.2, the signal path should be traced back from the output stages by applying the appropriate signals at convenient points. Voltages to be expected at various points are shown in the circuit diagrams.

6.2.6 No Transmission

If no signal is transmitted, after confirming the supply voltages described in 6.2.2, a single tone approximately 1kHz at 20mV rms should be applied to the microphone input. The voltages to be expected in the transmit mode at various points with this input applied are shown in the circuit diagram.

6.2.7 Unlocked Synthesizer

Should the synthesizer lose lock (indicated by UL being shown on the channel display and Unlock indicators H1 or H2 on the RF Mixer and Dual Synthesizer PCB, being lit) the following procedure should locate the cause of the failure:

- Verify the correct voltage on Z2 as shown on the circuit diagram 04-02450.
- Verify that the Enable, Data and Clock pulses on J3 pins 3, 4 and 5 respectively are the correct levels (0 or +5V).
- Verify the correct output level from IC6 and IC8 as shown on the circuit diagram.
- Verify the VCO control voltages at TP8 and TP9 are within the range shown on the circuit diagram.
- Verify that the VCO frequencies and levels (V6 and V14 emitters) are as shown on the circuit diagram.

6.2.8 Typical PA Voltages

In order to optimise the amplifier performance the PA amplifier transistors are matched in pairs identified by a coloured dot. Measurements taken in this area will depend upon the matched pair of transistors fitted and the frequency of transmission.

The tables below are a guide to the peak-to-peak voltages to be expected at specified points in the PA circuit. They are given for full power output when driven with a two-tone input. For the tests the supply voltage is 13.6V and the output is terminated into a 50Ω load.

Frequency (MHz)	Battery Current (Amps)	V18/V19		V16/V17		V12	
		C Vpp	B Vpp	C Vpp	E Vpp	C Vpp	B Vpp
2	9.7	27	2.4	13.2	0.4	3.2	0.9
4	9.8	27	2.4	13.2	0.5	3.2	0.9
6	9.2	27	1.9	12.0	0.4	2.7	0.9
8	9.0	32	2.5	13.5	0.5	2.7	0.9
16	10.4	24	2.8	14.0	0.7	5.0	1.5
18	8.9	26	2.3	11.5	0.7	6.3	1.3
24	8.9	22	2.4	12.5	0.8	7.5	1.8

6.3 Dismantling and Re-assembly

6.3.1 General

It may be necessary to remove printed circuit boards from the transceiver in order to carry out certain repairs. The paragraphs which follow give instructions for the removal and re-installation of boards. While carrying out these the following general points should be observed:

- **Screwdriver**—Screws with Pozidrive heads are used in almost all locations. Ensure that the appropriate screwdriver of the correct size is used.
- **Connectors**—The ribbon cable header and multiway connectors used in some locations can be incorrectly mated with their corresponding connectors. Care must therefore be taken when re-installing to ensure that these connectors are correctly mated.

6.3.2 Top and Bottom Covers

To gain access to the boards, the top or bottom cover must be removed from the transceiver. To remove either cover, the two screws (one on each side) must be removed and the rear edge of the cover lifted and drawn back so that the front edge is released from the panel surround.

When re-installing the cover, it should first be placed on the transceiver with its front edge resting on the two spring clips of the panel surround. The front edge must then be pressed firmly down while it is slid forward under the panel surround. When the cover is correctly positioned the rear edge can be pressed down so that the retaining screws can be re-inserted and tightened.

6.3.3 Circuit Board Removal

Printed circuit boards connected directly to the Motherboard are easily removed. After disconnecting any flexible leads connected to the board, its retaining screws can be removed and the multiway sockets on the board can be withdrawn from the corresponding pins of the Motherboard. This should be done by progressively raising each socket a small amount so that the board rises evenly. The procedure is reversed to re-install the boards.

Note: When removing the Audio and IF 1650kHz PCB, the heat sink secured to the side of the cabinet should be released before the screws retaining the board. On re-installation it should be secured last.

To remove the boards mounted behind the front panel, the flexible leads should be disconnected and the two countersunk screws released from each side so that the panel can be withdrawn from the cabinet. The two boards can then be released and separated.

6.3.4 PA and Filter Assembly

Note: The PA output transistors can be replaced without removing the board from the heat sink. Refer to para 6.3.5.

The PA and Filter PCB (08-03021) can be removed as follows:

1. Disconnect:
 - Ribbon cable(s) connecting rear panel connector(s) to the Motherboard.
 - Cable loom connecting the Option PS connector (if fitted) to the Motherboard. (This connection is made by two 4-way connectors. Note their positions to avoid cross-overs when reconnecting.
 - The ribbon cable connecting the PA and Filter PCB to the Motherboard. (This can be disconnected at both ends and removed.)
 - The 4-way Molex connector connecting two coaxial cables to the PA and Filter PCB.
2. Release the two screws at each side of the PA and Filter PCB which secure the board and the heat sink to the chassis side rails.
3. Release the two screws at the rear edge of the Motherboard which secure it to the heat sink assembly. Note that these two screws are shorter than the other screws securing the board.
4. Slide the heat sink assembly complete with rear panel and PA and Filter PCB away from the chassis.
5. Release the four screws securing the PA transistors to the heat sink. Note that at least one of these screws may be concealed by a capacitor, one end of which may have to be unsoldered to gain access to the screw.
6. Release the screw securing the clamp on the two driver transistors. Note that this screw is longer than the other screws used to secure the board.
7. Release a further two screws which secure the board to the heat sink.
8. Release the earth screw and the three screws that secure the rear panel to the heatsink.
9. Lift the board clear of the heat sink.
10. If work on the PA and Filter PCB is extensive, the dc power input lead may be unsoldered so that the rear panel can be taken away from the board.

11. Before re-installing the board, clean all the components in contact with the heatsink and the corresponding surfaces of the heat sink. Re-coat the cleaned areas with Jermyn Thermaflow A30. To re-install the board reverse the removal procedure taking particular care with the following:
 - When remounting the board on the heatsink, ensure that R16 and V11 are correctly located in their holes in the heat sink and that a mica insulator is under V15.
 - Ensure that the screws removed in disassembly are re-installed in their correct locations.
 - Screws should not be tightened until the reassembly is complete. To avoid straining connections to the PA transistors the screws securing these should be tightened last.

6.3.5 Replacement of PA Transistors

Since the PA output transistors are fitted in matched pairs they should be replaced only in matched pairs. The gain groupings of the SRFH1008 (selected MRF455s) transistors are identified by a coloured dot. Transistors of the same dot colour only should be fitted.

The PA transistors can be replaced without removing the PA and Filter PCB from the heatsink. It is necessary to release only the screws securing the transistors and to unsolder connections as follows:

1. Remove the transistor flange fixing screws.
2. Use a de-soldering tool or 'Solder-wick' to remove the bulk of the solder from each connection. Gently pull the leads away from the PCB while heating the joint.
3. Clear away any excess solder from the emitter, base and collector pads.
4. Thoroughly clean the transistor mating surface on the heatsink with a cloth or tissue.
5. Form the leads of the replacement transistor using the discarded transistor as a guide.
6. Coat the transistor flange with a thin film of thermal compound, e.g. Jermyn Thermaflow A30.
7. Check the orientation and fit the new transistor. Tighten the flange fixing screws evenly.
8. Carefully resolder the transistor connections. This should be carried out quickly using a very hot tipped soldering iron.
9. Re-adjust the bias current. Refer to 7.3.13.



7

Adjustments

7.1 Introduction

Two types of adjustment are covered under separate headings.

- Channel Addition: (no internal adjustments necessary)
- Preset Adjustments: normally factory-set adjustments will require attention only if components which affect their settings are replaced.

7.2 Channel Addition

For channel additions refer to the XP Programming Manual.

7.2.1 Channel Addition, Front Panel Programming Channels

In 9313/9480 series transceivers, fifteen channels can be programmed from the front panel to suit the user's requirements. However, to prevent transmission on frequencies for which the operator is not authorised, option TxD inhibits the entry of new transmit frequencies by the operator. This can be overridden by an internal link in order to program new transmit frequencies.

Enabling

Transmitter programming is enabled by shorting link 1 on the Microprocessor Interface PCB (refer to Fig. 7.1). The status of the link is noted by the microprocessor during the initialisation program; therefore it is only necessary to short the link (e.g. with a pair of tweezers) at switch on. Once the display panel is lit, the link may be removed but will remain effective until power is switched off. It should be noted that normal operation of the transceiver is inhibited in the programming mode. If it is intended to change or delete existing channels, refer also to Program Inhibit Indication below.

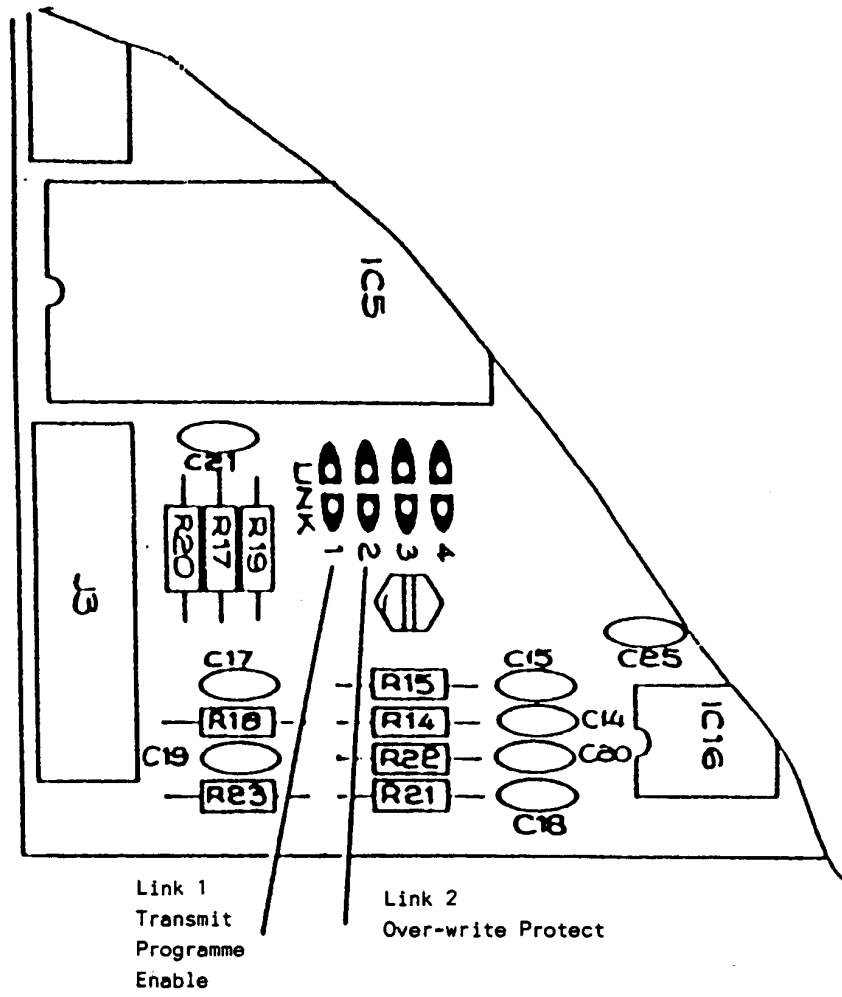


Figure 7.1 Microprocessor Interface PCB

Transmit Frequency Programming

Once the link is effective, transmit frequencies can be entered from the front panel as follows:

Action	Display will show	Remarks
Select any channel	Tx and Rx frequencies Channel No.	
Press Enter	Tx _____	Next action must be started within 60 seconds
Press number pads for transmit frequency	Tx 12.345.6	2000.0 to 24000.0
Press number pads for receive frequency (if same as Tx, press Enter only)	Rx _____	(23.000 in suffix H)
Press Enter	Rx 12.345.6	250.0 to 30.000.0
Press Enter	OPTION ___U___	Refer to Operators Handbook, section 5
Press Enter	P _____	
Press number pads for channel number	Pxx	
Press Enter	Tx and Rx frequencies P channel number	If the display shows prog inhib, USED or Full , refer to the corresponding heading below

Program Inhibit Indication

Established P channels can be protected from being accidentally deleted or over-written by the insertion of Link 2 on the Microprocessor PCB inside the transceiver (refer to figure 7.1). If an attempt is made to over-write or delete a channel when the link is installed, the display will show prog inhib for a few seconds when Enter is pressed. The Tx and Rx parameters can still be accepted by entering a new channel number and pressing Enter again. To over-write or delete existing channels, the transceiver must be switched off and the link unsoldered. The link should be resoldered with the transceiver switched off when the programming has been completed.

Used Indication

Channel numbers will normally be accepted on pressing the **Enter** pad. However, if a channel with the entered number has previously been programmed and the over-write link is not installed, the display will show USEd. The channel number can be either:

1. changed by entry of a new number on the number pads, or
2. accepted and the previously programmed frequencies over-written by a second operation of the Enter pad.

Full Indication

When all ninety-nine P channels have been programmed, on pressing the Enter pad to accept another channel, the display will show Full. A further press of the Enter pad will over-write the nominated channel. Alternatively some redundant channels can be deleted and then re-used. If the over-write protection link is installed, this must first be removed before channels can be deleted.

Too Hi, Too Lo Indications

If an attempt is made to program a channel with either a Tx or Rx frequency outside the range of the transceiver, an error message will be displayed. The error can be corrected by simply entering a new number on the number pads.

7.3 Preset Adjustments

7.3.1 Test Equipment Required

- A calibrated CRO with 10X probe with $10\text{M}\Omega$ and less than 12pF input impedance. Y amplifier frequency response of at least 25MHz .
- RF dummy load, 50Ω 100W RMS minimum and Power Meter to suit.
- RF signal generator covering the range 250kHz to 30MHz and capable of providing calibrated signals down to $0.25\mu\text{V}$ EMF from a 50Ω source.
- Frequency counter capable of resolving to 1Hz frequencies up to 24MHz .
- Regulated Power Supply which can be set to $13.6\text{V} \pm 0.2\text{V}$ and capable of supplying 20A peak current.
- Two-tone (i.e. 700Hz and 2300Hz) audio generator capable of providing $0\text{—}100\text{mV}$ RMS.
- Spectrum analyser suitable for SSB
- Multimeter or meters for measuring voltages ($20\text{k}\Omega/\text{V}$ or better) and current (100mA and 1A ranges) and an audio voltmeter.
- Transceiver Test Unit to Codan drawing 04-01868. (The isolating transformer should be screened to prevent pick-up from nearby mains transformers.)
- Square-wave generator capable of 5.5V pp at 100Hz .
- Decade resistance box for ease of determining select-on-test (SOT) resistors. (A resistance box constructed using the E12 series values of resistors is very useful.)

Before making any adjustments, the supply voltage must be set to $13.6\text{V} \pm 0.2\text{V}$.

When working on the low level stages, e.g. the receiver and exciter, the PA may be isolated by removing the dual coax socket to the PA and Filter PCB. This will prevent unnecessary heating of the heatsink and removes the possibility of high level RF fields being picked up by test leads which may cause erroneous measurements or transmitter instability. Note that this also disconnects the receive path (between the PA and Filter PCB and RF Mixer and Synthesizer PCB).

7.3.2 Voltage Regulators

None of the voltage regulators used are adjustable, so only their output voltage can be checked. The location and correct output voltages are as follows:

1. B rail regulator, $10V \pm 0.2V$; IC1 on Motherboard.
2. +5V regulators, $5V \pm 0.4V$.
 - IC2 on Motherboard.
 - IC7 on Audio and 1650kHz PCB
 - IC4 on RF, Mixer, and Dual Synthesizer PCB.
 - IC9 on Microprocessor Controller PCB
3. 26V regulator, $26V \pm 1V$; TP7 on RF Mixer and Dual Synthesizer PCB.
4. 9V regulator, $9V \pm 0.25$ Volts; emitter of V1 on RF Mixer and Dual Synthesizer PCB.

These voltages should be checked with the transceiver in receive mode.

7.3.3 Crystal Oven

The oven temperature cannot be adjusted but should be checked after allowing a five minute warm-up period. The temperature should be approximately 60°C .

7.3.4 VCO Adjustments (RF Mixer and Dual Synthesizer PCB)

These adjustments must be made with the metal shields in place.

VCO1

1. Select 30MHz frequency.
2. Using a DC Voltmeter or CRO, monitor TP8.
3. Adjust C42 via access hole in shield cover for $22.5V \pm 0.5V$ DC on TP8.
4. Select 250kHz; check TP8 is at $2V \pm 1V$ DC, and the 'unlock' LED for VCO 1 is not lit.

VCO2

1. Select any frequency.
2. Using a DC Voltmeter or CRO, monitor TP9.
3. Adjust C79 via access hole in shield cover for $2.7V \pm 0.2V$ DC

7.3.5 45MHz IF Alignment—Receive

1. Ensure the dual coax socket is connected to the PA and Filter PCB.
2. Connect the signal generator to the antenna socket.
3. Select a channel (USB) and adjust the signal generator output to the selected channel frequency plus 1kHz.
4. Increase the signal generator output until the signal is heard from the loudspeaker.
5. Connect the audio voltmeter to the Demodulator output on the Audio and IF 1650kHz PCB (TP2).
6. Adjust the 45MHz IF trimmer capacitors (outermost holes in shield lid) to half mesh i.e. screwdriver slots parallel to the long edge of the shield.
7. Adjust L29 and L32 (centre holes) for a maximum signal on the audio voltmeter.
8. Reduce the signal generator output and repeat step (7) until no further increase can be obtained on the audio voltmeter (below AGC threshold).

7.3.6 1650kHz IF Alignment

1. Align the 45MHz IF as above.
2. While still in Rx, peak the audio voltmeter reading by adjusting L1, L2, and L3 (on the Audio and 1650 IF PCB) and reducing the signal generator output to remain below AGC threshold.
3. When no further increase in the audio voltmeter reading can be achieved, check that the signal generator output is below 0.35 μ V PD for 10dB SINAD.

7.3.7 45MHz IF Alignment—Transmit

CAUTION

THE PROCEDURE WHICH FOLLOWS INVOLVES ALTERNATELY APPLYING A SIGNAL GENERATOR TO THE ANTENNA SOCKET TO SET RECEIVER ADJUSTMENTS AND SWITCHING TO TRANSMIT TO SET TRANSMIT ADJUSTMENTS. THE SIGNAL GENERATOR WILL BE DAMAGED IF IT REMAINS CONNECTED WITH THE TRANSCEIVER IN TRANSMIT.

1. Align the 45MHz IF in receive as above.
2. Align the 1650kHz IF as above.
3. DISCONNECT SIGNAL GENERATOR FROM ANTENNA SOCKET.
4. Disconnect dual coax socket from PA and Filter PCB.
5. Connect audio two-tone source to microphone input and switch transceiver to transmit.
6. Connect CRO across TP1 on the RF Mixer and Dual Synthesizer PCB.

7. Adjust L29 and C64 (second and fourth holes from left transceiver facing toward operator) for maximum amplitude of the displayed waveform.
8. Set the transceiver to receive and repeat steps (1) to (5) of 7.3.5.
9. Adjust C58 and L32 (extreme left and third hole from left) for maximum signal on the audio voltmeter.
10. DISCONNECT THE SIGNAL GENERATOR FROM ANTENNA SOCKET.
11. Switch the transceiver to transmit.
12. Ensure the two-tone signal is applied to the input and observe the amplitude of the waveform displayed on the CRO:
 - If the amplitude is below 200mV pp return to step (7) and repeat the procedure.
 - If the amplitude is greater than 200mV pp, disconnect the dual coax socket from the PA and Filter PCB and confirm that the amplitude increases to at least 400mV pp.
13. Reconnect the dual coaxial socket.

7.3.8 Highpass Filters

Five adjustments are required for the highpass filters, one for the Broadcast filter on the PA and Filter PCB and one each for the band selected filters on the RF, Mixer, and Dual Synthesizer PCB.

To adjust these filters:

1. Connect a CRO, set for maximum sensitivity, across TP1 on the RF Mixer and Dual Synthesizer PCB.
2. Connect a signal generator to the antenna socket.
3. Select a channel within each of the Frequency ranges shown in table below, in turn.
4. With each channel selected set the signal generator to the corresponding Sig Gen Freq and adjust its output level until adequate indication is seen on the CRO. (A starting level of 100mV is suggested.) Adjust the corresponding inductor for minimum indication on the CRO.

Channel Frequency (MHz)	Sig Gen Freq (MHz \pm 20kHz)	Inductor	Location of inductor
2 - 3.1	1.45	L14	PA & Filter PCB
3.1 - 4.8	2.2	L11	RF Mixer & Dual
4.8 - 7.5	3.4	L8	Synth PCB
7.7 - 11.6	5.3	L5	"
11.6 - 18	8.2	L2	"
18 - 24	10-12	No Adjustment	"

Note: When Option LF is fitted, the first adjustment (2 – 3.1) must be made with the signal generator frequency set to 1.18MHz.

7.3.9 Noise Limiter

1. Connect a DC Voltmeter to TP6 on the RF, Mixer, and Dual Synthesizer PCB. With no signal applied TP6 should be at approximately 2.5V DC.
2. Connect a signal generator to the antenna socket, select a channel (USB) and set the signal generator output to the selected channel frequency plus 1kHz.
3. Increase the signal generator output until the voltage at TP6 reduces to 2 Volts DC.
4. Adjust L47 for a minimum voltage on TP6.

Note: The null is not well defined.

7.3.10 Frequency Adjustment (USB)

1. Select the highest channel frequency (above 10MHz if possible) that is not transmit inhibited. Remove the dual coax socket to the PA and Filter PCB.
2. Connect the frequency counter across TP1 on the RF Mixer and Dual Synthesizer PCB.
Allow at least 5 minutes warm up before adjustment.
3. Press and hold the **Tune** pad.
4. Adjust C143 on the RF Mixer and Dual Synthesizer PCB for the correct frequency for the channel selected.
Note: If the adjustment range of C143 is not enough, the value of capacitor C142 may be changed. The temperature coefficient of the replacement capacitor must match that of the factory-fitted capacitor.
5. Reconnect the dual coax socket.

7.3.11 Frequency Adjustment (LSB)

9480 Only

1. Perform USB frequency adjustment as above.
2. Select a channel with LSB mode enabled.
3. Press the TUNE pad and adjust C162 until the output frequency (at TP1) is correct for the selected channel.
4. If the range of C162 is insufficient C161 may be altered to compensate.

7.3.12 Mute Adjustment

1. Connect the transceiver to an antenna (a short length of wire will suffice) and select an unoccupied channel.
2. To light the Voice Mute indicator, press the mute pad.
3. Begin with R73 on the Audio and IF 1650kHz PCB fully anti-clockwise and slowly rotate the control clockwise until the mute audio gate opens.
4. This is the threshold of mute operation. In order to reduce the sensitivity, rotate the control anti-clockwise 1/4 turn.
5. The mute circuit should now be sensitive enough to detect weak signals without false triggering on noise pulses. However, if desired, the sensitivity may be varied from this setting to suit individual requirements.

7.3.13 PA Adjustments

Disconnect the dual coax socket from the PA and Filter PCB.

Driver Bias

1. On the PA and Filter PCB (08-03743) remove the link feeding the centre tap of T3 primary and replace with an ammeter set to read 10 to 20mA.
2. Select on test a value for R46 for a current reading between 10 and 15mA with the microphone PTT switch pressed.
3. Remove the ammeter and re-install the link.

PA Bias

1. Remove link marked 'PA' on the PA and Filter PCB (F2 on circuit diagram 04-02452).
2. Replace link with an ammeter set to read 100 to 200mA.
3. Adjust R48 for a current reading between 100 and 150mA with the microphone PTT switch pressed.
4. Remove the ammeter and re-install the link.
5. Reconnect the dual coax socket.

7.3.14 Output Power

1. Ensure the dual coax socket is connected to the PA and filter PCB.
2. Connect an RMS or PEP power meter with dummy load to the antenna socket.
3. Connect a CRO via a 47k Ω resistor to the antenna socket.
4. Connect the audio output of the two-tone source to the test unit (AF in). Ensure the microphone amplifier is into compression.
5. Select the lowest frequency channel on the transceiver and operate the microphone PTT switch.

6. Select a value for the SET PWR resistor (R10) to set the two-tone output to:
 - for type 9313—100W PEP (i.e. 200V_{pp} into 50Ω)
 - for type 9480—125W PEP (i.e. 224V_{pp} into 50Ω)
7. Check the IMD (Intermodulation Distortion) over the band 2MHz to 24MHz. The power output may be reduced if necessary to give -26dB IMD on the worst channel.

7.3.15 Selective Call

The oscillator frequency of the phase locked loop on the Selective Call PCB must be set up as follows:

1. Apply a 1775Hz sine wave at 1.0V_{pp} to pin 2 of J1 on the Selective Call PCB. (Pin 3 ground.)
2. Connect a dc voltmeter between TP2 and TP3 of the PCB. (Polarity may be either way, connect so that meter deflection is forward.)
3. Adjust R15 for 0V ±50mV deflection of the voltmeter.

7.4 Receiver Performance Checks

7.4.1 Sensitivity and Signal + Noise to Noise Ratio

Connect an AC voltmeter across the audio output. Set the signal generator to 0.35μV PD output, connect it to the antenna socket and adjust the frequency to produce a 1kHz audio output.

Adjust the signal generator to a frequency outside the receiver passband and check that the audio output drops by at least 10dB.

7.4.2 AGC Check

Reset the signal generator output to 50mV PD and adjust the frequency to produce a 1kHz audio output. Reduce the volume to a convenient level. Reduce the signal generator output until the receiver output drops by 6dB. The signal generator level should be less than 2.5μV PD.

7.4.3 Audio Output

Increase the signal generator output to 50μV PD, adjust the frequency for 1kHz audio output. The audio output should exceed 4V RMS at the onset of clipping, as displayed on a CRO.

7.4.4 Selectivity (USB Operation)

Set the signal generator output to $0.5\mu\text{V}$ PD and note the audio output reference level. Increase the signal generator output 60dB and, using the Frequency Counter on the signal generator, adjust the frequency to -1kHz and then to $+4.2\text{kHz}$ from SCF. At these points the audio output should be less than reference level.

7.4.5 Clarifier Operation

With an input signal of SCF $+1\text{kHz}$ (SCF preferably greater than 10MHz) adjust clarifier and ensure frequency shifts of 0.001% (10ppm) can be made.

7.4.6 Noise Limiter Operation

Connect a BNC T-piece into the 50Ω coax from the signal generator to the transceiver. To the unoccupied socket add a BNC to two-terminal adaptor. Connect the output from a square-wave generator at a level of 5Vpp at 100Hz via a 100pF capacitor to the adaptor.

With the signal generator output set to produce a 1kHz audio output at a $0.5\mu\text{V}$ PD level switch the noise limiter on and off by shorting TP6 on the RF Mixer and Dual Synthesizer PCB. When ON, the audio tone should be clearly heard if the noise limiter is effective.

7.5 Transmitter Performance Checks

7.5.1 Frequency

Check as in section 7.3.10.

7.5.2 ALC

Use the Transceiver Test Unit and Audio Two-tone Source to modulate the transmitter. Slowly increase the audio input until the output power just ceases to increase (ALC threshold). Note the PEP output and increase the audio input by 30dB . The increase in output should be less than 0.5dB .

7.5.3 Power Output and Intermodulation Distortion

9313

The power output at 2MHz is 100W PEP falling to 90W PEP at 24MHz ($\pm 0.5\text{dB}$) and the IMD should be better than -26dB as measured on the spectrum analyser (use 700Hz and 2300Hz Audio Tones).

9480

Power output at 2MHz is 125W PEP falling to 90W PEP at 24MHz (+1dB); the IMD should be better than -26dB as measured on the spectrum analyser. (Use 700Hz and 2300Hz Audio Tones.)

Note: The indication of 100W PEP with two-tone modulation will depend upon the type of meter used to make the measurement, as follows:

- Peak reading meter: 100W
- RMS reading (thermal): 50W
- Average reading (Bird Model 43): 40.5W

7.6 RFDS Emergency Call Frequencies

9313 RFDS

Select an RFDS channel and disconnect dual coax socket to PA and Filter PCB. Press the **RFDS Call** pad and measure the frequencies on pins 10 and 13 of IC12 on the Microprocessor Controller PCB. Frequencies should be 880Hz +2Hz and 1320Hz +2Hz respectively. Reconnect dual coax socket.



8

Parts List

8.1 General Information

The parts list for each assembly contains the following information:

- circuit reference number.
- description giving the value and type of component.
- manufacturer and manufacturer's part number.
- Codan part number.

Note: Items having numerical references identifying specific components or subassemblies may be encountered in the parts lists included in this handbook. These items, selected from master manufacturing information, identifying parts which either are useful for maintenance purposes or relate to other items as cross referenced in the remarks column.

The following abbreviations are used for resistor and capacitor types:

Resistors	Capacitors
CC—carbon Composition	AS—solid aluminium electrolytic
CF—carbon film	CC—ceramic multilayer chip
MF—metal film	CE—ceramic
MG—metal glaze	EL—wet aluminium electrolytic
MO—metal oxide	M—stacked mica
WW—wire wound	PC—polycarbonate
PE—polyester	
PP—polypropylene	
PS—polystyrene	
PT—PTFE	
TA—solid tantalum	

8.1.1 Ordering Information

When ordering replacement components, all the following information should be quoted to minimise the risk of obtaining the wrong part and to expedite dispatch:

- equipment type (i.e. Type 9313 Transceiver)
- component location (e.g. Audio & IF 1650kHz PCB 08-03025)
- component circuit reference number (e.g. R3)
- full component description (e.g. Resistor 330k Ω 5% 0,33W CF)
- manufacturer and manufacturer's Part Number
- Codan Part Number.

8.1.2 Component Substitution

Due to continuous process of updating equipment and changes in component availability, minor variations in components may be noted from those listed. Equipment performance is in no way adversely affected by their substitution.

When replacing general purpose components (resistors, capacitors etc.), equivalent parts of other manufacture may be used provided that they have similar tolerances, voltage/power rating and temperature coefficients as those of the specified part.

8.2 Parts Lists

8.2.1 RF Mixer and Dual Synthesizer 03740-001	08-
Includes: 45MHz IF PCB	08-03097
VCO1 PCB	08-03098
VCO2 PCB	08-03099
8.2.2 Audio and IF 1650kHz PCB	08-03025
8.2.3 Microprocessor Controller	08-05090-001
Includes: Microprocessor Interface	08-05088-001
Microprocessor Assembly	08-05089-001
8.2.4 Motherboard	08-03744-001
Includes: Filter, Remote Control PCB	08-03127
Option R	15-10272
8.2.5 Display PCB, Transceiver	08-05129-001
8.2.6 Display PCB, Head	08-05113-001
8.2.7 PA and Filter	08-03743-001
8.2.8 Selective Call SD	08-03300-000
8.2.9 Antenna Driver PCB	08-04285
8.2.10 Cable Interface (Transceiver/Head)	08-03051



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Drawings

RF Mix and Dual Synthesizer	Circuit Diagram	04-02450
	PCB Assembly	08-03740
45MHz IF	PCB Assembly	08-03097
VCO1 and Mixer	PCB Assembly	08-03098
VCO2 and Mixer	PCB Assembly	08-03099
Audio and IF 1650kHz	Circuit Diagram	04-02093
	PCB Assembly	08-03025
Microprocessor Controller	Circuit Diagram	04-03031
Microprocessor Interface	PCB Assembly	08-05088
Microprocessor Assembly	PCB Assembly	08-05089
Motherboard and Chassis	Circuit Diagram	04-02453
Motherboard	PCB Assembly	08-03744
Filter Remote Control	PCB Assembly	08-03127
Display PCB, Transceiver	Circuit diagram	04-03045
	PCB Assembly	08-05129
Display PCB, Head	Circuit Diagram	04-03038
	PCB Assembly	08-05113
PA & Filter	Circuit Diagram	04-02452
	PCB Assembly	08-03743
Selective Call	Circuit Diagram	04-02250
	PCB Assembly	08-03300
Antenna Driver	Circuit Diagram	04-02724
	PCB Assembly	08-04285

