ELECTRICAL AND MECHANICAL
ENGINEERING INSTRUCTIONS (AUST)

TELECOMMUNICATIONS H 172

RADIO SET AN/GRC 106

TECHNICAL DESCRIPTION
RADIO SET AN/GRC-106

TECHNICAL DESCRIPTION

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For Figs 1001 to 1029 Circuit Diagrams For Radio Set AN/GRO 106 refer page 1000
INTRODUCTION

1. The Radio Set AN/GRC 106 is a HF (SSB) receiver-transmitter which operates on any one of 28,000 selectively tuned channels, spaced at 1 kc/s increments in the 2 to 29,999 Mc/s frequency range. Vermin tuning (±500 kc/s about any 1 kc/s increment) allows the receiver to be tuned to any frequency in the operating frequency range, ensuring compatibility with existing AM and radio-teletype terminal equipment that do not have the same accuracy and stability.

2. The radio set is used for reception and transmission of upper sideband (USB) voice, USB compatible AM and CW signals in simplex operation over a 50 mile range. Conventional double sideband, AM signals can be received but not transmitted. Frequency shift-keyed (FSK) and narrow frequency shift-keyed (NSK) signals can be received and transmitted using the appropriate radio teletype terminal equipment and primary power source.

3. The AN/GRC 106 is primarily intended for use as a mobile radio link (using a whip antenna), however, it may be used as a fixed mobile station using a doubler antenna to extend the effective range of operation.

4. The equipment consists of three major assemblies:
   a. Receiver-Transmitter, Radio, RT-662/GRC
   b. Amplifier, Radio Frequency, AM-334/GRG-106
   c. Mounting, MT-3140/GRC-106.

BRIEF ELECTRICAL DESCRIPTION

Transmission

5. SSB: Voice signals developed in the microphone are applied to the transmitter section of the RT-662/GRC where they are amplified and modulate the 1.75 Mc/s carrier in a balanced modulator to produce a double sideband signal with a suppressed carrier. The signal is filtered to allow only the USB portion (between 300 and 3,500 c/s above the original carrier) to pass. The USB signal is amplified further and translated, by a triple conversion process, to the desired RF operating frequency.

6. This RF signal is applied to the power amplifier portion of the AM-334/GRG 106 where the level is raised to 400 W PEP. The signal is then applied to the antenna coupler which matches either the 15 foot whip, or the doubler antenna, to the power amplifier to ensure efficient transfer or power with linear operation.

7. Compatible AM: The voice signals are developed and transmitted in the same manner as for SSB with one exception. Before the triple conversion process, the local carrier is reinserted into the signal, resulting in an USB RF output signal with a reduced carrier.

8. CW: In CW operation each time the key is pressed, a 2 kc/s generator is turned on in the transmitter. This 2 kc/s signal is used to modulate the local carrier and the resulting 1.75 Mc/s RF signal is filtered and translated in the same manner as for SSB operation. The transmitted RF is always 2 kc/s above the selected front panel frequency.

9. FSK: In FSK operation, a coded signal is applied to the RT-662/GRC (transmitter section) by the teletypewriter terminal equipment. The frequency of the coded signals will depend on the type of TTY terminal equipment used (MARK and SPACE frequencies must fall within the audio passband of 300 c/s to 3,500 c/s). Two audio tones produced are processed and transmitted in the same manner as SSB signals. The resultant RF output provides two CW signals (USB) at the following frequencies:
   a. Frequency as selected on the front panel plus MARK frequency.
   b. Frequency as selected on the front panel plus SPACE frequency.

10. NSK: The NSK operation is identical to FSK working except that the difference between the MARK and SPACE frequencies is much less i.e. narrow band, normally 85 c/s. By using suitable VF Telegraph equipment a greater number of channels are available for simultaneous operation in the audio pass band (300 c/s to 3,500 c/s) than is possible in the FSK operation. NSK signals are transmitted on the upper sideband only.
RECEPTION

11. SSB: The SSB signals appearing at the antennas are applied, via the AM-3349/GRC-106 to the receiver section of the RT-662/GRC where they are amplified and converted to a 1.75 Mc/s IF by a triple heterodyne process. The signal is then demodulated by inserting both it and the 1.75 Mc/s output, into a product detector. The resultant audio signals are then amplified. Two outputs are available, 10 nW and 2 W, for monitoring.

12. Compatible AM: Compatible AM (USB and carrier) signals are processed in the same manner as for SSB signals.

13. Conventional Double sideband AM: Conventional double sideband AM signals are converted to 1.75 Mc/s IF in the same manner as SSB signals. With the RT-662/GRC tuned to the exact carrier frequency of the received signal, the lower sideband (LSB) portion of the signal is suppressed by a crystal filter. The remaining USB portion is applied to a product detector along with the 1.75 Mc/s local carrier to accomplish the necessary demodulation. The resulting audio signals are then amplified to a 10 nW and 2 W level for monitoring.

14. CW: The CW signals are processed in the same manner as SSB signals except that a frequency of 1.752 Mc/s (+ 5 Kc/s depending on setting of RGC control) is inserted into the product detection instead of the 1.75 Mc/s local carrier. This allows the operator to adjust the audio CW tone or to reduce co-channel CW interference by nulling out the unwanted signal.

15. PSK and NBF: The PSK and NBF signals are processed in the same manner as SSB signals. The receiver output signals are applied to the radio teletype terminal equipment where they are converted for the teletypewriter printout.

BRIEF MECHANICAL DESCRIPTION

General

16. There are two methods of mounting the AN/GRC-106.

a. When used in a 1/2 ton vehicle the RT-662/GRC and the AM-3349/GRC-106 are stacked mounted on a MT-3140/GRC-106.

b. When used in a tracked vehicle the RT-662/GRC and the AM-3349/GRC-106 are secured to separate MT-3140/GRC-106 and mounted side by side.

17. The transmit-receiver relay, in the AM-3349/GRC-106, permits the same antenna to be used for both transmission and reception.

Receiver-Transmitter RT-662/GRC

18. The RT-662/GRC is a self-contained modular constructed receiver, low level transmitter, consisting of eleven plug-in modules, six sub-assemblies, a chassis and a front panel housed in a water-proof case.

19. The equipment has a self-contained power supply consisting of a dc to dc converter, and a 20 V voltage regulator, to produce the required dc operating voltages from the primary power source (vehicular generating system).

20. All 28,000 incremental operating frequencies are automatically selectively tuned by using a digital tuning system. Selection of an operating frequency is accomplished by rotating the MO and KO Front panel controls until the digits of the selected frequency are displayed in the small windows above the controls. Rotating the MO and KO controls also initiates the generation of a tuning code that is applied to the AM-3349/GRC-106 to automatically broaden tune to the selected operating band.

Amplifier, Radio Frequency, AN 3349/GRC-106

21. The AM-3349/GRC-106 is a self contained, linear, RF, power amplifier consisting of six sub-assemblies, a front panel, chassis and case. The case contains a dc-to-ac inverter for supplying the required ac operating voltages for the electron tube filaments and two blower motors. The front panel includes a dc-to-ac converter for supplying the required dc operating voltages for the tube screens and plates in the transmit mode. The equipment uses the vehicle supply as a primary power source.
22. The amplifier uses an air-to-air heat exchanger assembly that requires an internal blower (with front-to-rear airflow) to transfer the component heat to the heat exchanger and an external blower to transfer exchanger heat to the outside (right to left airflow). The heat exchanger, in the top of the case, is connected to the internal assemblies, through the air duct mounted on the inside rear wall of the case and the air ducts located on the inside top front of the case.

Front Panels

23. All operating controls, indicators and connectors, for the AN/GRC 105 are located on the front panels of the AM-3349/GRC-105 and the RT-662/GRC.

RT-662/GRC

24. Table 1 lists the front panel controls, indicators, connectors and their function.

---

**Figure 1 - Receiver-Transmitter, Radio RT-662/GRC, Controls, Indicators, and Connectors**

**Table 1 - RT-662/GRC Controls, Indicators, Connectors and Function**

<table>
<thead>
<tr>
<th>Control/Indicator</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>NOISE BLANKER switch</td>
<td>In the ON position, a noise blanking circuit is energized to reduce receiver desensitization caused by ignition (pulse) noise impressed on the RF input circuits.</td>
</tr>
<tr>
<td>MANUAL RF GAIN control</td>
<td>Varies the sensitivity of the RT-662/GRC receiver circuits.</td>
</tr>
<tr>
<td>SIGNAL LEVEL Meter</td>
<td>When transmitting, a relative indication of RF output is provided. When receiving, a relative indication of the RF input signal level is provided in dB above the AGC threshold.</td>
</tr>
<tr>
<td>SERVICE SELECTOR switch</td>
<td>Selects the mode of operation for the RT-662/GRC.</td>
</tr>
<tr>
<td>CONTROL, INDICATOR CONNECTOR</td>
<td>FUNCTION</td>
</tr>
<tr>
<td>------------------------------</td>
<td>----------</td>
</tr>
</tbody>
</table>

**Switch position**

<table>
<thead>
<tr>
<th>OFF:</th>
<th>Equipment Response</th>
</tr>
</thead>
<tbody>
<tr>
<td>a. Primary power applied.</td>
<td></td>
</tr>
<tr>
<td>b. Frequency standard oven assembly is energised.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>STAND BY:</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>a. Primary power applied.</td>
<td></td>
</tr>
<tr>
<td>b. AN/GRC 106 is initially inoperative, but ready to operate after a 60 second delay.</td>
<td></td>
</tr>
<tr>
<td>c. Frequency standard oven is energised.</td>
<td></td>
</tr>
<tr>
<td>d. Initiates 60 second delay in AM/3349/GRC-106 when the PRIM FWR switch is ON.</td>
<td></td>
</tr>
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<table>
<thead>
<tr>
<th>SSB NSK:</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>a. All standby functions repeated.</td>
<td></td>
</tr>
<tr>
<td>b. Receive and transmit switching controlled by the microphone or handset press-to-talk switch in conjunction with VOX switch, or auxiliary radio-teletypewriter terminal equipment.</td>
<td></td>
</tr>
<tr>
<td>c. Provides squelch and VOX capability.</td>
<td></td>
</tr>
<tr>
<td>d. Permits USB voice transmission and reception.</td>
<td></td>
</tr>
<tr>
<td>e. Permits NSK transmission and receptions to be made when using the appropriate ancillary radio teletypewriter terminal equipment.</td>
<td></td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>PSDK:</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>a. All standby functions repeated.</td>
<td></td>
</tr>
<tr>
<td>b. Receive and transmit switching controlled by ancillary radio-teletypewriter terminal equipment.</td>
<td></td>
</tr>
<tr>
<td>c. Squelch and VOX capability disabled.</td>
<td></td>
</tr>
<tr>
<td>d. Permits PSDK transmissions and receptions to be made using the appropriate ancillary radio-teletypewriter terminal equipment.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>AM:</th>
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<tbody>
<tr>
<td>a. All standby functions repeated.</td>
<td></td>
</tr>
<tr>
<td>b. Receive and transmit switching controlled by the microphone or handset press-to-talk switch in conjunction with VOX switch.</td>
<td></td>
</tr>
<tr>
<td>c. Permits USB voice signals with a re-inserted carrier (compatible AM) to be transmitted and received. Conventional DSB signals also may be received.</td>
<td></td>
</tr>
<tr>
<td>d. Provides squelch and VOX capability.</td>
<td></td>
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<table>
<thead>
<tr>
<th>GW:</th>
<th></th>
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<tbody>
<tr>
<td>a. All standby facilities repeated.</td>
<td></td>
</tr>
<tr>
<td>b. BPO circuit energised.</td>
<td></td>
</tr>
<tr>
<td>c. External modulation capability disabled.</td>
<td></td>
</tr>
<tr>
<td>d. Squelch and VOX disabled.</td>
<td></td>
</tr>
<tr>
<td>e. Energises 2 kHz/second generator.</td>
<td></td>
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</tbody>
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**NOTE:** The transmitted RF signal is 2 kHz higher than the indicated frequency on the front panel.

**AUDIO GAIN control**

Adjusts the audio output levels from the RT-662/GRC.

**BFO control**

Varies BFO circuit output frequency.
<table>
<thead>
<tr>
<th>CONTROL, INDICATOR CONNECTOR</th>
<th>FUNCTION</th>
</tr>
</thead>
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<tr>
<td>SQUELCH switch</td>
<td>In the ON position, the squelch circuits are energised, eliminating receiver background noise in the absence of received signals.</td>
</tr>
<tr>
<td>VOX switch</td>
<td>Selects the method by which the AM/GRC 106 is keyed when transmitting in SSB or compatible AM mode of operation.</td>
</tr>
<tr>
<td></td>
<td>Switch position</td>
</tr>
<tr>
<td></td>
<td>VOX</td>
</tr>
<tr>
<td></td>
<td>PUSH TO VOX</td>
</tr>
<tr>
<td></td>
<td>PUSH TO TALK</td>
</tr>
<tr>
<td>FREQ VERNIER control</td>
<td>Provides for continuous frequency tuning in the receive mode of operation.</td>
</tr>
<tr>
<td>NC controls (2 off)</td>
<td>Provides selection of the 10 Mc/s and 1 Mc/s digits of the operating frequency. The display above each control indicates the digit selected.</td>
</tr>
<tr>
<td>KC controls (3 off)</td>
<td>Provides selection of the 100 kc/s, 10 kc/s and kc/s digits of the operating frequency. The display above each control indicates the digit selected.</td>
</tr>
<tr>
<td>AUDIO CONNECTORS (2 off)</td>
<td>Two 10 pin connectors, connected in parallel, used for connecting the audio accessories (e.g. Handset) to the RT-662/GRC.</td>
</tr>
<tr>
<td>FUSE 2 AMP</td>
<td>Provides protection for the primary power input line.</td>
</tr>
<tr>
<td>SPARE</td>
<td>Contains a spare 2A fast blow fuse.</td>
</tr>
<tr>
<td>RECEIVER IN CONNECTOR</td>
<td>Coaxial connector used for connecting the received signals, routed through the AM-3349/GRC-106.</td>
</tr>
<tr>
<td>BENDING POST</td>
<td>Spring loaded binding post used for connecting a long wire antenna when the RT-662/GRC is used only as a receiver.</td>
</tr>
<tr>
<td>IP IN connector</td>
<td>Coaxial connector used for connecting an external 1.75 Mc/s IF during Transmit mode of operation (requires internal jumpering).</td>
</tr>
<tr>
<td>IP OUT connector</td>
<td>Coaxial connector used for connecting the internal third IF signal to external equipment (receiver operation only).</td>
</tr>
<tr>
<td>RF DRIVE connector</td>
<td>Coaxial connector used for connecting the RF output of the RT-662/GRC to the RF input of the AM-3349/GRC-106.</td>
</tr>
<tr>
<td>PA CONTROL connector</td>
<td>Used for connecting all control function to and from the AM-3349/GRC-106.</td>
</tr>
<tr>
<td>FREQ STD connector</td>
<td>Coaxial connector used for connecting an external 5 Mc/s frequency standard or for connecting the internal 5 Mc/s standard to external equipment.</td>
</tr>
<tr>
<td></td>
<td><strong>NOTE:</strong> INT-EXT switch in the frequency standard module must be set at EXT if external standard is used.</td>
</tr>
<tr>
<td>POWER connector</td>
<td>Used for connecting the +27 Vdc primary power from the vehicle generating system.</td>
</tr>
</tbody>
</table>
**Table 2 - AM-3349/GRC-106 Controls, Indicators, Connectors and Functions**

<table>
<thead>
<tr>
<th>Control, Indicator, Connector</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>ANT TUNE control</td>
<td>Used in conjunction with ANT LOAD control to match antenna to 50Ω output of the final amplifier stage of the AM-3349/GRC-106 according to the operating frequency.</td>
</tr>
<tr>
<td>ANT TUNE counter</td>
<td>Provides an indication of ANT TUNE control position. Initially set by ANT TUNE control to setting indicated on antenna tuning and loading chart or LOGGING CHART according to desired operating frequency and type of antenna being used.</td>
</tr>
<tr>
<td>ANT TUNE meter</td>
<td>Indicates relative degree of mistuning between antenna and AM-3349/GRC-106. The unit is correctly tuned when meter indication is at centre zero.</td>
</tr>
<tr>
<td>ANT LOAD control</td>
<td>Used in conjunction with ANT TUNE control to match the antenna to 50Ω output of the final amplifier, according to the operating frequency.</td>
</tr>
<tr>
<td>ANT LOAD counter</td>
<td>Provides an indication of ANT LOAD control position. Initially set by ANT LOAD control to setting indicated on antenna tuning and loading chart or LOGGING CHART according to desired frequency and type of antenna in use.</td>
</tr>
<tr>
<td>ANT LOAD meter</td>
<td>Indicates relative degree of mistuning between antenna and AM-3349/GRC-106. The unit is correctly tuned when the meter indicates centre zero.</td>
</tr>
<tr>
<td>TEST METER</td>
<td>Monitors the parameters selected by the TEST METER switch when the AM-3349/GRC-106 is keyed in an operating mode.</td>
</tr>
</tbody>
</table>
### Table 2 - (Contd)

<table>
<thead>
<tr>
<th>CONTROL, INDICATOR, CONNECTOR</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>TEST METER switch</strong></td>
<td>Selects the parameters to be monitored by TEST METER.</td>
</tr>
<tr>
<td>Switch position</td>
<td>Equipment response</td>
</tr>
<tr>
<td>PRIM VOLT</td>
<td>Primary voltage supply by vehicle generating system.</td>
</tr>
<tr>
<td>LOW VOLT</td>
<td>Output voltage for low-voltage power supply.</td>
</tr>
<tr>
<td>HIGH VOLT</td>
<td>Output voltage from high-voltage power supply.</td>
</tr>
<tr>
<td>DRIVER CUR</td>
<td>Cathode current of driver amplifier tube.</td>
</tr>
<tr>
<td>GRID DRIVE</td>
<td>Signal level at the grid of final amplifier tubes.</td>
</tr>
<tr>
<td>PA CUR</td>
<td>Plate current of the final amplifier tubes.</td>
</tr>
<tr>
<td>POWER OUT</td>
<td>Power output from AM-3349/GRG-106.</td>
</tr>
</tbody>
</table>

**HV RESET switch**

High voltage overload relay is reset when switched from OPERATE to TUNE.

<table>
<thead>
<tr>
<th>Switch Position</th>
<th>Equipment response</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>TUNE</strong></td>
<td>a. Transmitter is keyed.</td>
</tr>
<tr>
<td></td>
<td>b. All modulating capabilities are removed and local carrier is inserted for tuning.</td>
</tr>
<tr>
<td></td>
<td>c. Sensitivities of the ANF LOAD and ANF TUNE meters are increased to permit matching of antenna to 50Ω output of the final amplifier, according to the selected operating frequency.</td>
</tr>
<tr>
<td><strong>OPERATE</strong></td>
<td>a. All circuits are connected for transmitting.</td>
</tr>
<tr>
<td></td>
<td>b. Keying of the radio set is accomplished at the RT-662/GRG.</td>
</tr>
<tr>
<td></td>
<td>c. If tuning is changed in this position, keying will be inhibited, making it necessary for the HV RESET switch to be turned back to the TUNE position for returning before keying the radio set.</td>
</tr>
</tbody>
</table>

**PRIM PWR switch**

Applies or removes primary voltage when the RT-662/GRG front panel SERVICE SELECTOR switch is in any position other than OFF or OVEN ON. Also acts as a low voltage circuit breaker, will automatically remove primary power when over loaded. To reset, switch OFF then ON again.

Antenna tuning and loading chart

Lists approximate settings of ANF TUNE and ANF LOAD counters for various operating frequencies and type of antenna. Chart listings vary according to vehicle and type of antenna. Ensure that the correct chart for the installation and type of antenna, is being used.
### Table 2 - (Contd)

<table>
<thead>
<tr>
<th>Control, Indicator, Connector</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logging Chart</td>
<td>Used to log the setting ANT TUNE and ANT LOAD counters for specified frequencies. Provides quick reference for future tuning and enables tuning to be accomplished without breaking radio silence.</td>
</tr>
<tr>
<td>Whip Connector</td>
<td>Used for connecting 15 ft whip antenna.</td>
</tr>
<tr>
<td>50 Ohm Line Connector</td>
<td>Used for connecting doublet antenna.</td>
</tr>
<tr>
<td>GRD Binding Post</td>
<td>Used for connecting AN/GRC 106 earth to vehicle.</td>
</tr>
<tr>
<td>ROVR ANT Connector</td>
<td>Used for connecting antenna to the RT-662/GRC receiver when the AN/GRC 106 is operating in the receive mode.</td>
</tr>
<tr>
<td>Control Connector</td>
<td>Used for connecting control functions to and from the RT-662/GRC.</td>
</tr>
<tr>
<td>RF Drive Connector</td>
<td>Used for connecting RF output from the RT-662/GRC to RF input of AM-3349/GRC 106.</td>
</tr>
<tr>
<td>Prim Power Connector</td>
<td>Used for connecting +27 Vac from the vehicle generating system.</td>
</tr>
</tbody>
</table>

### General Description

**RT-662/GRC**

**Transmit (Pig 3)**

25. During transmit, the audio input from the microphone, handset or radio teletype-writer terminal equipment is applied to the audio portion of the transmitter IF and audio module 1A5. In SSB, compatible AM, NSK or FSK operation, the audio input signals are regulated to a constant amplitude and applied to a series of audio amplifiers. In CW operation, a 2 kc/s signal is developed from the 1 kc/s pulsed input, from frequency dividers module 1A6, each time the key is closed, and applied to the same audio amplifiers. This 2 kc/s signal is keyed to provide the transmitted intelligence in CW operation. This portion of transmitter IF and audio module, 1A5, also provides the VOX switching and performs the primary keying function.

26. The amplified audio output from the audio portion of 1A5 is applied to the balanced modulator in receiver IF module 1A7. The 1.75 Mc/s output from frequency dividers module 1A6 is applied to the balanced modulator. Mixing these two inputs in the balanced modulator produces a modulated 1.75 Mc/s DSB, suppressed carrier IF output. This output passes through a crystal filter, which removes the lower sideband, establishes the bandwidth of the upper sideband, and further attenuates the carrier.

27. The 1.75 Mc/s USB IF output from the crystal filter, in receiver IF module 1A7, is applied to the IF portion of 1A5. This output is also applied to the receive IF circuits in all modes of operation. (During CW transmission, the receiver IF circuit is switched on to allow monitoring of the 2 kc/s tone.) This portion of 1A5 provides the necessary IF amplification stages which are controlled by level control signals (dc voltage) developed from either the Power Amplifier AM-3349/GRC 106 or from internal automatic level control (ALC) assembly 1A1A5 in the RT-662. The internal ALC signal is used only when the AM-3349/ GRC-106 is not used.

28. In compatible AM operation, the 1.75 Mc/s local carrier is re-inserted into the signal path in this portion of 1A5. The level of this signal is controlled by the average power control (APC) signal applied from the AM-3349/GRC-106.
Fig 3 - Block Diagram of RT-660/crc
29. The amplified 1.75 Mc/s IF output from the IF portion of 1A5 is applied to a low frequency (1st) mixer in the translator module, 1A6. The function of 1A6 is to convert the 1.75 Mc/s IF signal into the selected operating frequency. This is accomplished through a series of mixing processes. In the IF mixer, the 1.75 Mc/s IF is subtractively mixed with the 4.55 to 4.650 Mc/s injection signal from the 10 kc/s and 1 kc/s mixer and 1 kc/s synthesizer module, 1A4, to produce a 2.8 to 2.9 Mc/s second IF signal. This signal is applied to a medium frequency (2nd) mixer and subtractively mixed with the HI (32.4 to 33.3 Mc/s) or LO (22.4 to 23.5 Mc/s) injection from the 100 kc/s synthesizer module, 1A2. This mixing produces a third IF between 19.5 and 20.5 Mc/s (LC) or between 29.5 and 30.5 Mc/s (HI). The use of either high or low injection is determined by the settings of the IF RF-662/GRC front panel 1 Mc/s and 10 Mc/s (MC) controls. The HI/LO control signal from the MC/s synthesizer module, 1A9, controls the selection of appropriate filters. The HI or LO third IF signal is applied to a high frequency (3rd) mixer and is mixed with the 2.5 to 23.5 Mc/s injection signal from 1A9.

30. The RF output products from 1A8 are applied to RF amplifier module 1A12. This module consists of two electron tube stages of amplification with highly selective tuned input and output circuits. A transformer and a portion of the capacitance required by these tuned circuits are contained on a motor-driven turret that is activated by the front panel MG controls. Discs holding fixed capacitors that supply the remaining capacitance required in the tuned input and output circuits are positioned by the digital 100 kc/s and 10 kc/s (KC) controls. The highly selective tuned input and output circuits attenuate all harmonic outputs from translator module, 1A8, except the one that represents the exact setting of the MG and KC controls. This RF signal is amplified to a nominal 35 W peak-envelope-power (PEP) output and applied directly through internal ALC assembly 1A1A5 to the RF DRIVER coaxial socket on the front panel RF-662 for coupling to the Power Amplifier AM-3349/GRC 106.

31. The generation of the mixing frequencies is accomplished in frequency standard module, 1A3, frequency dividers module, 1A6, MG/s synthesizer module, 1A9, 100 kc/s synthesizer module, 1A8, and 1 kc/s synthesizer module, 1A4. The function of 1A3 is to produce an accurate and stable 5 Mc/s reference frequency upon which all other frequencies are based. 1A3 produces four outputs: 500 kc/s, 5 Mc/s, 50 Mc/s and 10 Mc/s. The 500 kc/s output is applied to 1A5, which uses it to develop four outputs: 1.75 Mc/s for modulation in all modes and local carrier in compatible AM, a 1 kc/s pulsed output for use in 1A5 and 1A6, a 2.45 to 2.57 Mc/s (10 kc/s) spectrum, for use in 1A5, and a 45.3 to 16.2 Mc/s (100 kc/s) spectrum for use in 1A2. The 10 Mc/s signal from 1A3 is applied to 1A5 to lock its output at the required frequency. The 5 Mc/s output is available for reference or external use. The 10 Mc/s output is applied to 1A2.

32. 1A4 produces two outputs: 4.55 to 4.650 Mc/s mixing frequency (output determined by the 10 kc/s and 1 kc/s (KC) controls), for use in 1A8, and a 7.1 Mc/s output for use in 1A2. In 1A2, the 7.1 Mc/s signal, the 10 Mc/s output from 1A5 and the 100 kc/s spectrum from 1A6 are mixed with the output from an oscillator, the frequency of which is determined by the setting of the 100 kc/s (KC) control. This mixing produces two bands of frequencies for use in the translator module 1A8. The selection of the high or low band is determined by the HI/LO signal from MG/s synthesizer module, 1A9. This HI/LO signal is also applied to 1A8. 1A9 also produces a band of mixing frequencies for use in 1A8.

RECEIVE

33. The received RF signal is applied to RF amplifier module 1A12 and to noise blanker assembly 1A1A6. The same circuits in module 1A12 are used in receive and transmit. The two tuned amplifier stages raise the level of the incoming RF signal and provide the selectivity required to reduce adjacent channel interference, increase image rejection and reduce cross-modulation. Manual and automatic control of the gain of the amplifier is provided by receiver IF module 1A7.

34. The amplified RF output from RF amplifier module 1A12 is applied to translator module 1A8, where it is converted to a 1.75 Mc/s IF signal by means of tripler conversion process. This conversion process is essentially the same as that described in para 29 except the order is reversed. The input is applied to the IF mixer, then the RF mixer and finally the IF mixer (3rd conversion). The mixing frequencies used are developed in the MG/s synthesizer module 1A9, 100 kc/s synthesizer module 1A2, and 10 kc/s and 1 kc/s synthesizer module 1A4 respectively. Final mixing results in a 1.75 Mc/s IF composite signal (which contains the modulating intelligence).

35. The 1.75 Mc/s IF composite signal is applied to a crystal filter in receiver IF module 1A7. The filter is used to establish the desired 3.2 kc/s bandwidth for the IF signal. An automatic gain control (AGC) voltage is developed and applied to RF amplifier module 1A12. An automatic gain control voltage is developed from 1A5 (for product detection) or the variable EPG signal (generated in 1A7) is used to modulate the 1.75 Mc/s IF composite signal. (The use of the variable EPG signal allows the operator to vary the tone ± 3.5 kc/s during CW operation). The demodulated audio information is amplified in receiver audio module 1A10. During CW transmit operation, the sidetone from receiver IF module 1A7 is applied to receiver audio module 1A10 to allow the operator to monitor the CW tone.
FIG 4 - FREQUENCY SCHEME
36. The output from 1A7 is applied to 1A10 through the AUDIO GAIN control, where it is amplified and applied to the AUDIO connectors on the front panel. A squelch circuit is provided in 1A10 to distinguish noise from voice during SSB or compatible AM operation. Module 1A10 provides two outputs: 1W for driving a loudspeaker and 10 mW for the headset or handset.

37. Frequency generation is accomplished during receive operation in the same manner as transmit with the following exceptions: the mixing processes are reversed; the 1.75 Mc/s from 1A6 is used for demodulation and the output from 1A4 can be interrupted by pulses from noise blanker assembly 1A16. Assembly 1A16 produces a blanking pulse during that period of time that the received RF signal contains ignition type (pulse) noise. Therefore, the audio output, from the receiver, is turned off for that period of time.

FREQUENCY SCHEME (Fig 4)

38. Fig 4 illustrates the frequency scheme used to translate any received RF signal between 2 and 29,999 Mc/s to a 1.75 Mc/s IF, and conversely, to translate the 1.75 Mc/s IF to an RF signal between 2 and 29,999 Mc/s (transmit).

39. The frequency conversion involves translator module 1A8, the MC and KC controls Mc/s synthesizer module 1A9, 100 kc/s synthesizer module 1A2 and 10 kc/s and 1 kc/s synthesizer module 1A4. The MC and KC controls select the correct crystals in the respective synthesizer modules and the HI/LO switching circuits in the correct sequence. The synthesizer modules inject the correct frequencies into 1A6 which separately mixes the three injection frequencies with the incoming signal to produce the 1.75 Mc/s IF (receive) or with the 1.75 Mc/s IF (transmit) to obtain the desired RF.

40. As an example, assume that the KC and MC controls are set at 07275 and the unit is in receive condition. The input to 1A8 from RF amplifier module (1A2 is a 7.275 Mc/s signal. The output from 1A9 (injection frequency to the RF mixer) is 12.5 Mc/s and the HI/LO switching circuits are in the LO condition. The output from the RF mixer is applied to filter FL1, which passes the sum of the inputs (19.775 Mc/s). This 19.775 Mc/s signal is applied to the MF mixer. The MF mixer injection frequency, from 1A2, is 22.600 Mc/s. The output from the MF mixer is applied to filter FL3, which passes the difference between the 19.775 Mc/s and 22.600 Mc/s frequencies. This 2.825 Mc/s signal is applied to the IF mixer, where it is subtractively mixed with the 4.575 Mc/s injection frequency from 1A4. The resulting 1.75 Mc/s is the operating IF signal.

41. Since the KC and MC controls provide for the tuning of RF amplifier module 1A12 and the injections from the synthesizer modules, any frequency between 2 and 29,999 Mc/s may be converted to the 1.75 Mc/s IF. In transmit, the action is reverse. Mixing takes place to convert the 1.75 Mc/s IF to the selected RF output.

POWER SUPPLIES

42. The power supply circuits for the Receiver-Transmitter RF-662/GRG are located in dc-to-dc converter and regulator module 1A14. These circuits are the 22V regulator circuit and the dc-to-dc converter circuit. Their operation is detailed in the circuit description section of this instruction.

Modules and Assemblies

43. The following modules and assemblies, form the Receiver-Transmitter, Radio RF-662/GRG which are prefixed by the numeral 1. Amplifier, Radio Frequency AM-3349/GRG-105 assembly reference designation are prefixed with the numeral 2.

a. Chassis and front panel assembly 1A1.
b. 100 Kc synthesizer module 1A2.
c. Frequency standard module 1A3.
d. 10 and 1 kc synthesizer module 1A4.
e. Transmitter IF and audio module 1A5.
f. Frequency dividers module 1A6.
g. Receiver IF module 1A7.
h. Translator module 1A8.  

j. MC synthesiser module 1A9.  
k. Receiver audio module 1A10.  
l. DC-to-DC converter and regulator module 1A11.  
m. RF amplifier module 1A12.  

**FREQUENCY STANDARD MODULE 1A3 (Fig 1001 and 1002)**  

44. The Frequency Standard sub-assembly produces an accurate, stable reference frequency upon which all frequencies within the system are based. Housed in this sub-assembly is a temperature controlled oven, the crystal oscillator, the frequency divider and the multiplier circuits. The following output frequencies are produced: 5 Mc/s, 10 Mc/s, 1 Mc/s and 500 Kc/s, all frequencies being referenced to the 5 Mc/s frequency standard. The oven used in this assembly is precision temperature controlled and is used to stabilize the frequencies of the crystal and oscillator-buffer amplifier circuitry (fig 1004). A booster heater is used for quick warm up. Thermostat S + S2 (lower right fig 1001) applies the full 27 Volts to oven winding H6-300 by-passing transistor Q1, after a fast warm up S1 opens (when oven temperature reaches 75°C) and the dynamic range of the proportional control circuitry then maintains the oven temperature. Thermostat S2 opens the 27V line if the oven temperature exceeds 90°C. The proportional control provides extremely precise temperature control without thermostat switching. The oven is maintained at a fixed temperature of approximately 85°C with a maximum variation of ± 0.05°C due to ambient temperature changes and variation in supply voltage. Since the temperature coefficient of the crystal is ± 0.2 parts per degree Celsius, an ultimate frequency stability of ± 1 part in 10⁶ is obtained.  

45. The circuit diagram of the proportional control oven circuit is shown in the lower section of fig 1004. A bridge, consisting of the two halves of transformer primary winding T1-A2, a thermostat R1-A1 is in the feedback loop to amplifiers Q1, Q2-A2. The resistors and thermostats have different temperature coefficients but at the operating temperature of the oven their resistances are equal. When the oven temperature is low, the bridge is unbalanced in such a way that positive feedback occurs. This results in an oscillation of approximately 10 to 100 kHz with an output proportional to the amount of feedback. If the signal is detected by Q3-A2 and fed to DC amplifier Q1 which controls the amount of current in the oven windings (emitter resistors R1-30Ω and R2-40Ω) thereby permitting a greater dynamic range and efficiency than can be obtained by heating the oven directly from ac. As the nominal oven temperature (85°C) is reached, the bridge approaches balance reducing the amount of feedback. If the oven temperature rises above the desired temperature, negative feedback occurs and oscillation ceases. In practice, the positive feedback is just enough to keep the oscillator power at an amplitude which will compensate for the heat power lost in the oven. A maximum output of approx 15 W is available during warm up, while at -40°C ambient, the oven draws approx 2W to maintain its temperature at 85°C.  

46. The oven assembly is encased in an insulated enclosure with sufficient foam material around it to minimize heat loss. The DC amplifier Q1 (oven control) is mounted in such a way so that its collector heat dissipation is used to supplement the heating power. Zener diode VR1-A2 maintains voltage supplied to Q1, Q2-A2 collectors at ± 18 V. Thermistor R13-A2 compensates for changes in ambient temperature. Resistor R7-A2 (temperature adjust) is used for setting up the correct oven temperature, and should only be readjusted when proper calibration facilities are available. Diode CR3-A2 is an isolation diode between the detector driver Q3-A2 and DC amplifier Q1 (oven control).  

**Oscillator and buffer (Fig 1001 - top)**  

47. The crystal Y1 (5.0 Mc/s) and the associated oscillator and buffer circuitry are housed within the temperature-controlled oven structure, thereby providing a fast warm up period and better results under temperature - stabilized conditions. The crystal is housed in an evacuated glass envelope having dimensions identical to an HC-6/U holder. The crystal oscillator uses a grounded base circuit, the feedback path being between the collector and emitter of Q1-A1 via T1, Y1, C5 and C6. Variable capacitor C6 (screwdriver adjustment at the top of the plug-in assembly) provides for frequency adjustment during calibration. This adjustment should only be made after the equipment has been switched on for 30 minutes and with calibration equipment which has a frequency stability equal to or better than the frequency standard employed in this equipment. Diodes CR1, CR2-A2 act as amplitude limiters for oscillations at the collector of Q1-A1. Zener diode VR1-A1 maintains the applied voltage to the bases of Q1, Q2-A1 at +7.5V.
Transistor Q2-A1 acts as a buffer amplifier isolating the 5 Mc/s oscillator from loading effects by follow up circuitry. The accurate 5.0 Mc/s signal produced by the oscillator and amplified by the buffer are fed via transformer T2-A1 to switch S1-A3 in the frequency standard module 1A3 (Fig 1002). The oscillator oven and the temperature control circuitry are housed in the same plug-in unit, whilst the generating circuitry for the 10 Mc, 1 Mc and 500 kc frequencies is located on the printed circuit boards adjacent to the plug-in oven unit.

Frequency Generation Circuitry (Fig 1002)

48. Switch S1-A3 is a screwdriver adjustment accessible through the top of module 1A3 cover and may be set in following positions.

a. INTERNAL position: Feeds the 5.0 Mc/s signal from the internal oscillator and buffer to the frequency multiplier Q4-A3, and amplifier Q2-A3 to provide a 5.0 Mc/s signal to the external jack on the front panel (engraved FRG STD). This accurate 5.0 Mc/s output can be used to drive another HT 662/9RG should its frequency standard be faulty, or this output may be used for checking the accuracy of the Xtal frequency standard, also as an accurate RF signal source for testing purposes.

b. EXTERNAL position: Accepts an external 5.0 Mc/s signal. This external signal then feeds the frequency generating circuitry to produce the 10 Mc, 1 Mc and 500 kc outputs. (Q1, Q3-A3 forms an amplitude limited for the incoming 5.0 Mc/s signal).

49. The 5.0 Mc/s signal is fed via S1-A3 to the bases of Q1-A3 and Q2-A3. The collector of Q1 is tuned to 10 Mc/s and forms a by 2 multiplier for the incoming 5.0 Mc/s signal. The 10 Mc/s output from T1-A2 is fed via R1 to R5-A2 in the 100 kc synthesizer module 1A2 (Fig 1020). The 10 Mc output at jack J1-A3 is nominally 50 ± 15 mV, and the 5 Mc output at J2-A3 (5 Mc 1M/33k ohm) 125 ± 20 mV. The 5.0 Mc signal from amplifier Q2-A3 is fed via T2-A3 to the RF input of the switcher, and also to the primary of tuned transformer T2-A2 and thence to the base of mixer stage Q3-A2. A second frequency 1 Mc/s (yet to be derived) is applied to the secondary of tuned transformer T2-A2, therefore two frequencies, 5 Mc/s and 1 Mc/s, appear to the non linear mixer Q3-A2 whose output will contain the usual sum and difference products. Transformer T3-A1 in the collector circuit of the mixer is tuned to 1 Mc. This transformer also serves as the output coupling device. The 1 Mc signal is now applied to multiplier stage Q2-A2 and its collector output is tuned to the fourth harmonic of 1 Mc i.e. 4 Mc/s, thereby providing the 4 Mc signal referred to previously.

50. This is a closed loop circuit and if the 5.0 Mc signal fails, there will be no output. The loop gain at the desired frequency of 1 Mc must exceed unity if oscillations are to be sustained in the 'regenerative' divider circuits. Random noise is assumed to start the initial oscillations when the circuit is first energized. The 1 Mc signal developed by the closed-loop oscillatory circuit has the same accuracy as the 5.0 Mc frequency standard, upon which the receiver-transmitter system is based. Transformer Q4-A2 is a locked 500 kc oscillator triggered by the 1 Mc signal from T3-A2. Q1 is not forward biased but relies on the negative half cycle of the 1 Mc signal to start its conduction, the collector of Q1 is tuned to 500 kc/s thereby synchronizing its output to every second cycle of the accurate 1 Mc signal. The 500 kc output derived from this circuit is applied via R5-A2 to E2-A1 in the Frequency Divider Module 1A6 (Fig 1006) and the 500 kc output level at J4-A2 is nominally 220 ± 30 mV. The 1 Mc signal from the regenerative divider is applied via N7-A2 to R2-A1 in the MO Synthesizer Module 1A9 (Fig 1048) and the 1 Mc output level at J2-A2 is nominally 550 ± 100 mV.

RADIO FREQUENCY AMPLIFIERS 1A12 (Figs 1003 to 1006)

51. The RF amplifier functions as a dual purpose unit. In the RECEIVE mode, signals from the antenna are amplified before application to the translator unit for conversion to the IF frequency. In the TRANSMIT mode of operation the RF drive signals are amplified before being applied to the Power Amplifier AM-3319/9RG 106.

Digital Tuning of the RF Amplifier

52. Variable selectivity, capable of being directly tuned with a high degree of precision is used in the RF amplifier. There are no variable tuning controls such as parallel-operated variable capacitors or moving iron slugs. Digital tuning is a technique required for rapid, simple, and convenient selection and tuning of the receive frequency by means of a set of controls arranged on a one-knob-per-digit basis. Digital tuning, as it is utilized by this receiver-transmitter is performed without the need for a digital-to-analog conversion process and, therefore, does not require the usual proportional control system.
55. The inherent simplicity of the system greatly enhances the overall reliability of the equipment as well as the electrical performance. The selective circuits in this receiver-transmitter are digitally tuned by variable capacity to permit a higher coil Q and more uniform Q over any tuned band. As an amplifier becomes non-linear when sufficient voltage is applied to its input, it is essential that as much selectivity as possible be placed before the first RF amplifier. To accomplish this, exact amounts of fixed capacity are switched into the tuned circuits to provide the tuning in a digital manner.

56. For any given frequency, the first two knobs on the front panel select a fixed-tuned megacycle strip by rotation of the megacycle turret. The third knob, representing the 100 kc digit, as it is rotated 0 through 9, switches fixed capacity into the tuned circuits. This is accomplished by rotating a small turret inside the main MC turret (Fig 106). There are ten pairs of these capacitors, decreasing in value of capacitance, for the ten kc digit. In a similar manner the 10 kc digit knob switches another group of ten capacitors to further decrease the capacitance across the megacycle coils. These select the 10 kc tuning points. The 1 kc knob does not operate the RF amplifier, since the tuned circuit bandwidths are sufficient to tune 1 kc increments.

57. The physical arrangement of the tuned circuits on a megacycle strip is termed "3 way stretch". To prevent unwanted coupling between input, interstage and output tuning, these circuits are not placed on the same strip. For example, the 2 Mc double tuned input circuit T1 and T2 (Fig 1008 and Table 3) is located at the bottom of the A6 MG strip, the interstage circuit 38 (Fig 1006) is in the middle of the A2 MG strip and the output circuit 44 (Fig 1006) is at the top of A2 MG strip. The same system is used for each Mc tuning strip. For a given input circuit, the interstage tuning is always located on a strip seven units further around the turret in a clockwise direction, and the output tuning is seven strips further on. This spaces the tuned circuits for any Mc band at the required distance to effectively prevent unwanted coupling.

58. Table 3 gives location of the particular tuned circuit in relation to band setting. Fig 5 is a simplified diagram showing the basic concept of the digital tuning as used in the receiver-transmitter. Fig 6 is a simplified circuit showing the arrangement whereby fixed capacitors are switched into circuit by the 100 kc and 10 kc digital controls.

RF Amplifier, Code Switch Operation

59. The purpose of the motor code switching system is to accurately position two turrets, one of which is the turret in the RF Amplifier sub assembly. This turret positions the megacycle tuning strips for each of 28 megacycle bands, ranging from 2 through 29 megacycles. The switching scheme places a ground on any one of 28 wires, one for each megacycle. This action completes the circuit to a relay which in turn positions its contacts to start a motor. Connected to the turret and rotated by the motor, is a switch with a notch, so positioned that when the notch reaches the proper contact, the ground path to the motor relay is again broken. This stops the motor to position the megacycle tuning strip.

60. Fig 7 shows a portion of the circuitry used to accomplish the turret positioning. Switch S5, section 3 rear is the megacycle selection switch, the second knob from the left on the front panel. S6, section 3 rear, does the switching for the second and third decades, that is, 10 through 19 Mc and 20 through 29 Mc. The first decade switch, 2 through 9 Mc is not shown. The switch as shown in Fig 7 has continuity through the wiper to Contact 17 which is the wire for the 10 Mc position. If the switch is moved to the 11 Mc position, the wiper passes through 18 and comes to rest on contact 19. As the switch is rotated further to 12, 13, etc., the wiper passes through 20 and 21, then to 22, etc. The same contacts connect to the wires for 15 through 19 Mc/e. The two wires also serve when the second decade is covered. This time, wires 2, 5, 8, 10 and 21 are covered by the upper wiper and wires 3, 5, 7, 9 and 11 are covered by the lower wiper. The first decade switch 2 through 9 Mc is not shown but operates in the same manner.

61. The proper decade is selected by switch S5, rear. This switch has a second function (ground pulse) which is described last. In addition, there is the extra wiper contacts. This switch is the 10's of Mc and is the first knob to the left on the system and is used to select the three 10's of Mc positions 0-1-2. Switch S6, section 3 rear, described above, displays the numerals 0 through 9, thus, the two switches in combination can display the megacycles 00 through 29. 00 and 0 are, of course, not used. The circuit path through the system for 10 Mc is as follows. The ground originates at contact 7 on switch S6, section 1 rear. This switch rotates with S6, section 3 rear and also has a ground pulse function. The switch always stops with a wiper on contact 3. From contact 3 the ground is applied to contact 6 on the 10's of megacycles switch, S5 rear. This switch selects the proper decade on switch S6.
59. (Contd)

Contact 2 is for the first decade, not shown. Contacts 3 and 4 select the second and third decades, respectively and the ground is applied from contact 6 to contact 3. This in turn connects to wire 15, a wiper contact on S6. The diagram shows the switch set for 10 Mc on contact 17. The ground wire now enters the cable and appears on contact 10, switch S9, front. Since S9 - rear, is mounted on the back of S9 - front, the holding rivets connect the two wipers together and the ground also appears on S9 rear. The contact on S9, rear, connects the ground to contact 7 on relay, K2, the motor relay. Switch S9 - front, revolving clockwise with the turret continues to revolve until the notch on its wiper reaches contact 10. At this time the ground path is broken and the motor stops. This positions the turret so that the 10 Mc strip is connected into the RF amplifier circuitry.

![Diagram of RF tuning](image)

**Fig 5 - Digital RF Tuning**
### Table 3 - Digital Tuning of the RF Amplifier (3 Way Stretch)

<table>
<thead>
<tr>
<th>Freq. No</th>
<th>Input</th>
<th>Interstage</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>A16</td>
<td>A23</td>
<td>A2</td>
</tr>
<tr>
<td>3</td>
<td>A17</td>
<td>A24</td>
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</tr>
<tr>
<td>29</td>
<td>A15</td>
<td>A22</td>
<td>A29</td>
</tr>
</tbody>
</table>
60. The action of the complete system is such, that any megacycle from 02 through 29 set up on the first two digit switches on the front panel, causes the turret in the RF amplifier to rotate and connect into the tuning circuitry the proper megacycle tuned circuits. Note that, while C0 and C1 can be set upon the two switches, C1 Mc is not used at a frequency in this system. When these positions are set up, the receiver remains tuned to the last setting of the frequency control knobs in the 2 megacycle position. For each of the 29 megacycle positions a second turret switch in the megacycle synthesizer is also positioned, through a gear system, by the same motor driving the RF amplifier turret. The purpose of this turret will be taken up in the section devoted to the Megacycle Synthesizers.
RF Amplifier Circuit Description (Figs 1005 and 1006)

61. The RF Amplifier is a dual purpose unit. It is used in both the receive and the transmit mode of operation. When a new frequency is set up on the front panel by the digital tuning controls, motor B1 operates to position the megacycle turret until the proper tuning strips are engaged. Motor B4 is energized by relay K2. The coding system places a ground on one of 28 wires. A special switch, which rotates with the turret, turns until it finds this wire, at which time it removes the ground to stop the drive motor. When K2 energizes to start the drive motor B1, contacts 6-8 open. This removes +27V from certain other circuitry which mutes the receiver-transmitter whenever a turret is moving. Contacts 2-5 start the motor and contacts 2-4 provide dynamic braking for the motor.

Receive Mode

62. The incoming signal enters the RF Amplifier at J7-A3 and is applied to the tuning transformer 1A1271 on the megacycle tuning strip selected. Chart C, on the schematic diagram, shows the component values for each megacycle tuning strip. On three of these strips a crystal V4 is connected across T2 to trap out certain mixer injection frequencies. When the RF Amplifier is used in the transmit mode of operation, strips A9, A10, and A11 have the above mentioned crystals. These crystals have no purpose in the receive mode of operation and can be ignored. The megacycle tuning strips provide a double tuning arrangement at the input. Capacitors on printed circuit board assemblies are selected and connected into the resonant tuned circuit by the 100 k and 10 k knobs on the front panel. These printed circuit boards, carrying the capacitors, are in the form of stacked turret switch wafers revolving inside the megacycle turret. Fixed capacitors C3, C40 and C32 are used in conjunction with the capacitors on A31 and A30 to correctly tune T1 to the desired frequency. When the 100 k knob and the 10 k knob are rotated, 0 through 9, the effective capacitance is reduced, step by step, to affect digital tuning of the megacycle strips. The 1 k knob does not operate in the RF Amplifier. Two capacitors are changed by the 100 k knob as shown in fig 1005. Chart B shows the capacitance values for the 100 k tuning points and Chart A shows the values for the 10 k tuning points. T2 is capacitively tuned in a similar manner to T1. From the input tuned circuits the signal is applied to the grid of 1A12V1, the first amplifier tube. A ferrite bead on the grid wire acts as a parasitic suppressor. Tube V4, located on the chassis, is grounded by the plate of the plate of each tube and 6.3 VAC is used as filament voltage. Decoupling on the +125VDC line is provided by 1A12M and 1A12C9. Several capacitors, C25, C26, C27 and C28 prevent RF from flowing in the 6.3AC filament line.

Transmit Mode

64. The operation of the RF Amplifier sub assembly in the transmit mode is exactly the same as for receive with one exception. The AGC voltage is disabled and does not control the gain of the tubes. In the chassis, relay K3 switches the input from receive to transmit. Relay K4 performs the same function for the output.

TRANSLATOR MODULE 1A8 (Figs 1007 and 1008)

65. The Translator Sub assembly, using injection frequencies from the three synthesizers, converts any frequency, 2 to 29,999 Mc, to the IF frequency of 1.75 Mc. In the transmit mode the IF frequency of 1.75 Mc is converted to any one frequency in the range 2 to 29,999 Mc.

Triple Conversion Translator Concept

66. The purpose of a translator in a super-heterodyne receiver is to convert the incoming RF signal to the IF frequency. At the stable, IF frequency consistent gain and good selectivity can be obtained if all incoming signals are changed to one common IF frequency. For the reception of signals in the 2.0 Mc to 30 Mc range, it is desirable to make the frequency change from RF to IF frequency in three distinct steps. This results in the best reduction of image frequencies and spurious responses. In superheterodyne receivers, where a nonlinear element is used to get a desired IF frequency signal from the mixing of the RF frequency and a local oscillator signal, interference from spurious external signals results.
in a number of undesired frequencies that may fall within the IF frequency band. Proper selection of the IF frequencies used and the methods of filtering can reduce these spurious responses to a minimum.

67. The translator sub assembly contains the mixer broadband filter combinations used in conjunction with synthesized injection frequencies to translate any of the 28,000 input frequencies to the output frequency of 1.75 Mc. Table 4 shows the frequency scheme to cover the range of 2.0 Mc to 30 Mc. This scheme fulfills three important considerations not found in most other arrangements:

a. The mixer outputs are such that relatively narrow broadband filters can be used, eliminating the necessity for variable tuned IF amplifiers.

b. The spurious crossover frequencies created during the mixing process can be kept to a low amplitude.

c. The injection or oscillator frequencies into each mixer are independently controlled by the digit knobs on the front panel, thus eliminating any complicated differential gearing or their electrical equivalent.

68. In the receive mode, the desired antenna signal is mixed to either one of two bandpass filters. The megacycle column in table 4 indicates the injection frequency which allows this. Notice that this frequency is changed each time the megacycle digit is changed. Consequently, the passband of the filter following this mixer is 1 Mc wide. One of the two filters is automatically selected when the megacycle knob is tuned, such that undesired mixer products can be sidestepped as the input frequency varies between 2.0 Mc and 30 Mc. These arrangements result in very few crossover products. The use of two filters reduces the number of injection frequencies into the first mixer. The same mixer frequency can be used two and three times. Also, an alternate injection frequency can be used whenever the first conversion signal contains a mixing crossover. Seventeen injection frequencies are used to cover the twenty-eight one megacycle increments between 2.0 Mc and 30 Mc.

69. The first conversion signal is converted to a frequency which will pass through a bandpass filter having a passband of 100 Kc and passing signals between 2.8 and 2.8 Mc. The mixing scheme flow chart, table 4, shows that the injection frequencies are arranged in two groups separated by 10 Mc. The frequency selected is automatic and is properly selected to reduce spurious responses to a minimum. If the megacycle mixing calls for the low filter, then the low injection frequencies are used in the 100 Kc column of the chart. Likewise, the high column 100 Kc injection frequencies are used when the high filter is used in the megacycle mixer. The second conversion signal is mixed with injection frequencies which convert to the 1.75 Mc IF frequency. These appear in the last column of the chart, table 4. Only a tuned transformer follows this last mixer as the IF amplifier tuned circuits perform the filtering function.

70. The frequency scheme chart can be used to determine the three injection frequencies required at the mixers to convert any antenna signal between 2.0 Mc and 30 Mc, to the 1.75 Mc intermediate frequency. It will be noted that although the sidebands are inverted in the second mixer, they are inverted again in the third mixer such that an upper sideband signal at the RF amplifier input produces an upper sideband at the 1.75 Mc output of the translator. Since the translator is used, without change, in either the receiver or the transmitter modes, an automatic switching scheme is used to activate only these stages required to activate the proper filter after the first mixer stage. A switching technique using semi-conductors is used, which permits signal path switching without the introduction of non-linearity usually associated with diodes. Basically the diode is forward biased to conduct and reverse biased to inhibit signal flow. The signal to be passed actually modulates the DC current of the conductive diode. The bias current is made such that the signal biasing is slight in comparison and thus only a linear portion of the conductivity curve is used. Since the third conversion, transistor node, is not followed by a tuned filter, a balanced diode mixer is used in order to keep Inter modulation distortion products to a minimum. All other mixer stages are transistors. These transistor mixer stages are properly linearized and gain stabilized such that they maintain gain equal to the insertion loss of the following filters.
### TABLE 4 - FREQUENCY INJECTION SCHEME

<table>
<thead>
<tr>
<th>MC OSC INJECTION</th>
<th>100 KC INJECTION</th>
<th>10 KC VFO</th>
<th>1 KC VFO</th>
<th>INJ. FREQ.</th>
</tr>
</thead>
<tbody>
<tr>
<td>LOW</td>
<td>HI</td>
<td>LOW</td>
<td>HI</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>17.5</td>
<td>22.4</td>
<td>32.4</td>
<td>6.590</td>
</tr>
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<td>3</td>
<td>16.5</td>
<td>22.5</td>
<td>32.5</td>
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</tr>
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<td>4</td>
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<td>6.570</td>
</tr>
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<td>30</td>
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HI-LO Filter Switching

71. The output from the first mixer in the receive mode or the third mixer in the transmit mode is passed through either one of two filters, depending upon the dictates of the frequency tuning scheme.

Receive Mode

72. In the translation or conversion process, the RF signal from the RF amplifier is mixed with one of 17 crystal oscillator injection frequencies. Depending upon the particular megacycle being received, the filtering process after the first conversion mixer requires one of two filters. Since the two filters differ by 10 Hz, an automatic switching system is used to select the proper filter. This is accomplished by four diodes arranged as input and output gates for the two filters.

73. Fig 8 is a simplified schematic showing the diodes and filters. The signal input is at point A. The signal must pass through one but not both filters to reach point B, the signal output. Plus 10 VDC is applied to each diode. Diodes A2CR4 and A2CR3 have +10V on their anodes. When this control line is at point C is grounded, the anodes of A3CR1 and A2CR3 are grounded through windings in the filter and resistors A5R2 and A5R1. Since there is +10V on the cathodes of A3CR1 and A2CR3, both diodes are back biased and no signal can pass through the LO BAND filter. The same ground is applied on the cathodes of A5R3 and A5R5 through the windings in the filter and resistors A5R3 and A5R1. These two diodes have +10V on their anodes and will conduct, allowing the incoming signal to enter and leave the HI BAND filter. A ground on the control line has, therefore, selected the HI BAND filter and rejected the LO BAND filter.

74. When the LO BAND filter is required, as determined by the frequency selection scheme, +20V is applied to the control line at point G. +20V now appears on the cathodes of diodes A3CR3 and A2CR5 through resistors A3R5 and A2R1, and windings in the filter. Since the anodes of these two diodes have only +10V applied, they are back biased and block the signal from passing through the HI BAND filter. +20V is, at this same time, applied to the anodes of A3CR1 and A2CR3 through resistors A5R2 and A5R1 and windings in filters. Since the cathodes have +10V applied and their is now +20V on their anodes, diodes A3CR1 and A2CR3 are forward biased and conduct, forming a low impedance path into and out of the LO BAND filter. A3L and A2L3 isolate the signal path from the +10V power supply. The switching voltage of +20VDC or ground at the control point C is obtained from a switching system in the megacycle synthesizer and depends on the crystal selected in that subassembly.

Transmit Mode

75. The action, in the transmit mode, is the same as in the receive mode except that the signal input and output points are interchanged.

TRANSLATION ARITHMETIC

Receive Mode

76. Assume that the incoming RF signal is 50.521 Mc. The following paras show the actual arithmetic involved in order to translate or convert this frequency to the intermediate frequency of 1.75 Mc. The chart with block diagram as shown in Table 4 is used. The first two digits are 05 indicating that the proper crystal is 14.5 Mc as found in column 2 opposite 5 Mc in the first column. It is important, at this point, to note that the 14.5 Mc crystal is in the column marked MC OSC INJECTION LOW. This dictates the use of the LOW column in the 100 kc digit conversion. This also indicates that the filter in use will be the LOW filter 19.5 to 20.5 Mc. By addition, 14.500 plus 05.321 equals 19.821 Mc. By addition, 14.500 plus 05.321 equals 19.821 Mc. This is within the passband of the low filter and the signal will be passed on to the second conversion mixer. The signal path is indicated in the block diagram at the top of the chart.

<table>
<thead>
<tr>
<th>Incoming RF signal</th>
<th>05.321</th>
</tr>
</thead>
<tbody>
<tr>
<td>Injection frequency (5 Mc)</td>
<td>+ 14.500 Mc</td>
</tr>
<tr>
<td>1st Conversion signal</td>
<td>19.821 Mc</td>
</tr>
</tbody>
</table>

The next digit to be considered is the 100 kc digit, 3, in this example. Column 4 indicates the 100 kc digit. Opposite digit 3, in column 5, a crystal frequency of 4,853 Mc is found. This frequency is not used directly in the translation process; it merely indicates the crystal in use in the 100 kc Synthesizer for digit 3 or 300 kc. It was noted that the crystal for the megacycle conversion is in the LOW column, therefore, the LOW column is used in the 100 kc conversion. In column 6, 22.7 Mc is the indicated injection frequency for digit 3. The first conversion signal is subtracted from the 100 kc injection frequency. By subtraction, 19.821 MC from 22.700 is 2.879 Mc or the second conversion signal.
FIG 8 - HI-LO FILTER SWITCHING
Injection frequency (digit 3) - 22,700 Mc
1st conversion signal - 12,821 Mc
2nd conversion signal - 2,579 Mc

To arrive at the injection frequency for the third conversion it is necessary to compute it from two sets of crystal frequencies, since the last two digits are combined and converted in one step. The two digits are the 10 kc digit and the 1 kc digit. These two digits in the example are 21. For the 10 kc digit, 2 in column 8, a crystal frequency of 6,570 Mc is found in column 9. For the 1 kc digit, column 8 is again used and after digit 1 a crystal frequency of 1,914 Mc is found in column 10. The difference of these two crystal frequencies is equal to 6,570 minus 1,914 or 4,629 Mc. Combining this injection frequency with the second conversion signal of 2,579 the difference is 4,629 minus 2,579 or exactly 2,050 Mc, the required intermediate frequency.

Injection frequency - 4,629 Mc
2nd conversion frequency - 2,579 Mc
3rd conversion frequency - 2,050 Mc

If the megacycle frequency is found to require a crystal in the HIGH injection column, then the HIGH injection column for the second conversion is used. It should be noted that in the first or megacycle conversion that the sum signal is not always used. For 22, 23, 27, 28 and 29 Mc the difference signal of the incoming RF frequency minus the injection crystal frequency is used. Column 14 requires some clarification. There are 100 injection frequencies to cover the digits 00 through 99. Column 14 shows the injection frequency for 0 and 9 each decade. It is useful in checking to see if the computed injection frequency is correct, since it must fall within the decade limits. For further examples see below:

RECEIVE TRIPLE CONVERSION IN RF TRANSLATOR SUBASSEMBLY

Example 1

Frequency selected - 16,273 Mc
1st conversion injection - (18 Mc)
1st conversion signal - 11,500 Mc

2nd conversion injection - (digit 2)
1st conversion signal - 29,773 Mc
2nd conversion signal - 4,273 Mc

3rd conversion injection -
2nd conversion signal -
IF signal -

.070 = 6,529 subtract
.003 = 1,913 subtract
.070 = 4,577 Mc

Add
HI filter 29.5 to 30.5 Mc

Subtract
PL 2

Filter 3
2.8 to 2.9 Mc

Subtract
TL Tuned to 1.75 Mc

To Receiver IF
Example 2

Frequency selected -
1st conversion injection -
1st conversion signal -

27.697 Mc
7.500 Mc
20.197 Mc

\[ \text{subtract} \]

23.000 Mc
20.197 Mc
2.803 Mc

\[ \text{subtract} \]

FL 1

\[ \text{LO filter} \quad 19.5 \text{ to } 20.5 \text{ Mc} \]

2.301 Mc
1.750 Mc

\[ \text{subtract} \]

FL 3

\[ \text{filter} \quad 2.8 \text{ to } 2.9 \text{ Mc} \]

3rd conversion injection -
2nd conversion signal -
IF signal -

4.553 Mc
2.803 Mc
1.750 Mc

\[ \text{subtract} \]

T1 Tuned to 1.75 Mc

To Receiver
IF

\[ .090 = 6.500 \text{ subtract} \]

\[ .037 = 1.207 \text{ subtract} \]

\[ 4.553 \text{ Mc} \]

Transmit Mode

77. In the transmit mode the translation process is reversed. Use the same chart shown in Table 4 but assume that the block diagram has the signal path shown in reverse. The data shown in the various columns is exactly the same. In transmit it is desired to translate or convert the 1.75 Mc IF frequency to any one of 28,000 RF frequencies. Using the same example, the arithmetic is shown to translate 1.75 Mc to the RF frequency of 87.321 Mc.

Since the process is reversed, the first conversion for transmit involves the last two digits or \( 21 \). Again the injection frequency must be computed from columns 9 and 10.

Crystal frequency (digit 2) - 6.570 Mc
Crystal frequency (digit 1) - 1.204 Mc
Injection frequency (21) - 4.553 Mc

Injection frequency (21) - 4.629 Mc
1.750 Mc IF frequency - 1.750 Mc
1st conversion signal - 2.879 Mc

In working backwards, it is now known immediately which column, HI or LOW for the 100 kc digit, should be used. Looking ahead to the megacycle digits it is noted that the crystal frequency for 05 Mc is 14.5 Mc and that this is in the LOW column. Therefore, the 100 kc digit conversion will use the injection frequency found in the LOW column.

Injection frequency (digit 3) - 22.700 Mc
1st conversion signal - 2.879 Mc
2nd conversion signal - 19.821 Mc
The injection frequency for 05 Mc (LOW) is found to be 14.5 Mc.

2nd conversion signal - 19.321 Mc
Injection frequency (5 Mc) - 14.500 Mc
3rd conversion signal - 05.321 Mc

05.321 is the desired transmit RF frequency.

Two more examples for the transmit mode are as follows:

TRANSMIT TRIPLE CONVERSION IN RF TRANSLATOR SUBASSSEMBLY

Example 1

Convert 1.75 Mc to 16.259 Mc

Crystal frequency (digit 5) 6.540 Mc
Crystal frequency (digit 9) 1.920 Mc
1st conversion injection 4.591 Mc subtract

1st conversion injection 4.591 Mc
1.75 Mc IF frequency 1.720 Mc
1st conversion signal 2.841 Mc subtract

PL 3

2nd conversion injection 22.600 Mc
1st conversion signal 2.841 Mc
2nd conversion signal 19.759 Mc

PL 1

LOW filter 19.5 to 20.5 Mc

2nd conversion signal 19.759 Mc
3rd conversion injection 3.500 Mc
3rd conversion signal 16.259 Mc

To RF AMPLIFIER
Example 2

Convert 1.75 Mc to 0.630 Mc

Crystal frequency (digit 2) 6.560 Mc
Crystal frequency (digit 0) 1.750 Mc
1st conversion injection
4.620 Mc subtract

1st conversion injection
1.75 IF frequency 4.620 Mc
1st conversion signal 2.850 Mc

2nd conversion injection
33.000 Mc subtract
1st conversion signal 2.850 Mc
2nd conversion signal 30.150 Mc

2nd conversion signal
3rd conversion injection
29.5 to 30.5 Mc
3rd conversion signal 0.630 Mc

Circuit Description of the Translator

78. The translator subassembly is basically a group of mixer-filters used to convert any one of 28,000 incoming RF signals to the IF frequency. In the transmit mode of operation, the IF frequency is converted to any one of the 28,000 RF frequencies. The translator subassembly is used in both the receiver and transmit modes of operation. The mixer stages for receive and transmit modes are separate; only the filters, following each mixer stage, are common to both functions in the subassembly. Switching signals for the receive-transmit modes are derived from the transmit-receive relay in the chassis. Switching signals for the HI-LO filter change are dependent on the frequency in use. These signals are derived from a switch in the Megacycle Synthesizer.

Receive Mode (Pages 1007 and 1008)

79. 1st Conversion Mixer and Filters. The receive signal from the RF amplifier is applied to voltage divider A3R6 and A3R6 (fig 1008) which attenuates the signal 6dB. Diodes A30R1 and A30R5 provide amplitude limiting to prevent overloading mixer stage A3Q1. The receive signal, applied to the base of A3Q1, mixes with the megacycle injection signal applied to its emitter. This injection signal is derived from the megacycle Synthesizer subassembly and enters the translator at J1, A1. Diode A30R6 protects the emitter-base junction of A3Q1 from excessive reverse bias. Mixer A3Q1 is activated by a ground applied to pin 5 of J1A in the receive mode.
This ground also turns on diode gate A3CR7 which is forward biased by +10VDC from zener diode A2VR1. This gate action allows the mixer products from A3Q1 to be applied to diode gates A3CR4 and A3CR3. Diode gate A3CR2 is back biased in the receive mode, since ground is applied through A37 to its anode. Its cathode is at a potential of +10VDC. Back biasing A3CR2 prevents signal voltage from being applied to transformer A3T1 which is a portion of the transmit signal path. Since the mixer products from stage A3Q1 are applied to both diode gates, A3CR4 and A3CR3, the one turned on controls the signal path to the correct filter FL1 or FL2. The Hi-Low filter switching is actuated by diode gate A2CR2 and resistor A2R2 and the transmission switch is selected by the Megacycle Synthesizer. Each filter has a pass band of 1 Mc. The signal, after passing through the proper filter, is gated out by either diode gate A2CR3 or diode gate A2CR5. (Fig. 1007), these two diodes are also a part of the Hi-Low filter switching. The signal passed by the filter in use is the 1st conversion signal. The +10VDC which is constantly applied to the Hi-Low filter switching circuitry is derived from dropping resistor A2R2 and zener diode A2VR1.

2nd Conversion Mixer and Filter

80. The 1st conversion signal, selected by either filter FL1 or FL2 and gated by A2CR3 or A2CR5, is now applied to the diode gate A2CR2. With A2CR2 gated "open" the 1st conversion signal reaches the base of the 2nd conversion mixer A2Q1. The 100kc injection frequencies enter the subassembly at J1A-4A from the 100 kc Synthesizer. These signals are applied to the emitter of A2Q1 and the mixer products of this stage are applied to filter FL3. Diode gate A2CR1 is non-conducting in the receive mode and prevents application of the output of A2Q1 to the base of mixer, A2Q2, which is a part of the transmit circuitry. Application of +10VDC or GND to pins 3 and 5 of J1A controls the action of diode gates A2CR1 and A2CR2. The operation of these gates is similar to that described for gates A3CR2 and A3CR3. The application of +10VDC to pins 3 and 5 of J1A also activates either receiver mixer stage A2Q1 or transmit mixer stage A2Q2, depending on mode, by applying bias to the bases of these two transistors. The mixer products from stage A2Q1 are applied to filter FL3 which has a bandwidth of 100 kc. Frequencies between 2.8 Mc and 2.9 Mc are passed. These signals are the 2nd conversion signals and, after gating by A2CR2, reach the base of mixer stage A1Q2. Diode gate A1CR1 is activated by application of +10VDC or GND to pin 3 of J1A. This also activates the mixer stages A1Q2 or A1Q1. In the receive mode +10V is applied to the base of A1Q1 which cuts this stage off. At this same time +10V activates A1CR1 and the mixing potential is developed at its base and emitter. The + potential applied to A1CR1 cathode is derived from the collector of A1Q1. Injection signals from the 10 and 1 kc Synthesizer are applied to the emitter of A1Q2. These enter the unit at J1A-4A. The mixer products of stage A1Q2 will contain the 1.75 Mc IF frequency. These signals are applied to tuned transformer A1T1. A1T1 and a crystal filter reject all mixer products except the 1.75 Mc IF frequency. The crystal filter is contained in the receive IF subassembly.

TRANSMIT MODE

1st Conversion Mixer and Filter

81. In the transmit mode the translation or conversion of the 1.75 Mc IF signal to any one of 28,000 RF frequencies, between 2 and 30 Mc, is accomplished in reverse order to that in the receive mode. The same bandpass filters are used, as well as the same injection frequencies for each conversion. The 1.75 Mc IF frequency enters the subassembly at J1A-4A (Fig 1007) and is applied to divider A1R1-A1R2. The signal then is applied to the base of mixer stage A1Q1. The 10 and 1 kc Synthesizer injection signals reach the emitter of A1Q1 from J1A-A1 through capacitor A1C1. A ground applied to pin 5 of J1A activates mixer stage A1Q1 by controlling the base bias divider circuit, A1BR-A1R3. As described in the receive mode, diode gate A1CR1 is non-conducting which prevents the mixer products of A1Q1 from reaching A1Q2, which is a part of the receive signal path. The mixer products are applied to filter FL1 which passes signals between 2.8 and 2.9 Mc. These are the 1st conversion signals.

2nd Conversion Mixer and Filters

82. Diode gate A2CR1 is in the conducting mode allowing the 1st conversion signals to be applied to the base of 2nd conversion stage A2Q2. Application of +10VDC to pin 5 of J1A activates stage A2Q2. Application of +10VDC to pin 5 of J1A de-activates A2Q1 which is part of the receive signal path. The 100 kc injection signals from the 100 kc Synthesizer enter the transistor at J1A-4A and are applied to the emitter of stage A2Q2 through capacitor A2R3,
82. (Contd)

The mixer products in the collector circuit of A2Q2 are applied to diode gates A2QR3 and A2QR5. Diode gate A2QR2 is in the non-conducting mode and prevents the signals from being applied to the base of A2QT. Gating of the mixer products from A2Q2 by diodes gates A2QR3 and A2QR5 is automatic and selects the proper filter, either FL1 or FL2. The output of the filters is controlled by diode gates A3QR8 and A3QR3. These diode gates are part of the HL-L0 switching system already described. The signals from FL1 or FL2 are the second conversion signals.

3rd Conversion Diode Mixer

83. The signals from the filter are now applied to diode gates A3QR7 and A3QR2. Gate A3QR7 is non-conducting which prevents the signal from being applied to A3Q1. Diode gate A3QR2 is conducting and applies the signal to transformer A3T1. A3T1 passes all signals between 19.5 Mc and 30.5 Mc. The 2nd conversion signals are applied from A3T1 to balanced diode mixer A3QR8-A3QR5. The megacycle injection signals enter the subassembly at J1B-A1 and are applied through capacitor A304, resistor R358, and resistors A3R9-A3R10, to the diodes of mixer A3QR8-A3QR5. The injection and 2nd conversion frequencies will tend to be at any point in the 2nd conversion due to the balanced circuitry. The sum and difference signals predominate and are obtained from the secondary of transformer A3T2. This transformer is a broadband type passing frequencies between 2 and 30 Mc. The RF frequencies from A3T2 are amplified by the direct coupled amplifier A3Q2-A3Q3. This dual amplifier uses a feedback circuit through A3Q1C and A3Q2C. The feedback circuit stabilizes the gain and broadens the frequency response range. The output is taken from transformer A3T3 and leaves the subassembly at J1B-A1. The tuned circuits of the RF Amplifier select the proper RF frequency from the mixer products of balanced mixer A3QR8-A3QR9. Numerous decoupling circuits are used throughout the subassembly to prevent RF frequencies from reaching power supplies or switching circuits.

RECEIVER IF, AGC, AND AUDIO SUB ASSEMBLY MODULE A47

The Step Type AGC System

84. Conventional AGC systems used in AM receivers are not extremely efficient when used in single sidetone reception. In SSB transmission, no carrier is present to establish a signal strength level, the AGC system must establish its control voltage from the information contained in one sideband. This information varies greatly in amplitude and, with normal voice operation, is intermittent. A second problem is intermodulation distortion when the bias of amplifiers is increased in order to control their gain. The basic design of an SSB AGC system is to reduce, or entirely eliminate, the interdependency of discharge and hang time. A sample of the received signal is taken from the IF path and applied to a tuned amplifier. Two outputs are taken from the amplifier, identical in frequency and character, but different in amplitude by twenty percent. The larger of the two signals (Ei) is applied to a timing detector having a fast rise time and a definite prescribed discharge time. The lower amplitude signal (Eo) is applied to a similar detector having a fast rise time and an extremely long discharge time. The two DC output voltages of these detectors are compared in a switch. As long as Ei remains above Eo, the AGC output voltage will remain flat even in the absence of input signal. Depending upon the pre-established discharge time constant of the timing detector, voltage Ei will at sometime drop to a value less than Eo, at which time the comparison switch will discharge both detector outputs to ground, thus causing the AGC voltage to drop to near zero. If, during the process, new signal information is received in the IF amplifier strip, this circuit rapidly injects itself as the sign information and repeats the above described process. Fig 9 illustrates the action that takes place.

85. Aside from the problem of derivation of an adequate control voltage, there is yet another problem; the generation of intermodulation distortion in the amplifiers whose gains are being controlled. For optimum AGC operation, the input function of the semiconductor amplifiers is reduced, hence, it would seem that the ability of the stage to handle the increased signals, without generation of an appreciable amount of intermodulation distortion, is somewhat limited. Intermodulation distortion is the creation of distortion products based on the sum and difference frequency of harmonics of the desired signals. If signals equal to Ei and Eo were present to a non-linear element having second and third order curvature, the difference frequency of 1 kc could re-modulate each frequency to develop distortion products at 999 kc and 4002 kc. Since all of these signals are within the passband, selectivity is of no assistance. Reducing emitter current to control gain is accompanied by a reduction in power handling capability. As signal input is increased and the gain of the transistor is reduced, distortion tends to rise. The best solution to the problem is to preserve the linearity of the stage and to leave intact the dynamic range of the amplifier, by finding other methods of controlling gain.
85. (Contd)

Removal of the by-pass capacitor from across the emitter resistor of a transistor amplifier results in decreased gain due to negative current feedback. Since the linear range of the amplifier is increased, distortion is reduced with increase of signal. A transistor can be used as a variable impedance which is a function of a DC current change. This DC controlled impedance can be connected in series with the emitter by-pass capacitor to effectively control the gain by varying the degree of feedback. Fig 10 presents a block diagram of the AGC system.

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**Fig 9 - AGC Response to SSB or CW Signals**
FIG 10 - BLOCK DIAGRAM OF AGC SYSTEM IN THE RT 662/8GC
AGC Circuit Description (Fig 1010)

86. The AGC system used in the receive mode of operation is a step type which does not require the presence of the carrier with the received signal. The IF signal is taken from a tap on transformer A171 and is amplified in two stages, A2Q1 and A2Q2 (Fig 1010). These two stages are associated only with the AGC circuitry. The output from stage A2Q2 is divided into two signals, a full 100% signal and an 80% signal. The 80% signal is derived by tapping down on the collector load of stage A2Q2, (tuned transformer A2T2). The 100% signal is rectified by diode A2Q8R and is amplified in DC Amplifier A2Q3. The DC voltage derived from this amplifier charges capacitor A2Q9. Capacitor A2Q9 and resistor A2Q10 form a time constant having a fast rise time and a definite prescribed discharge time. The voltage on this circuit is applied to the base of switch stage A2Q4. The 80% signal is rectified by diode A2Q8R and the resulting DC is filtered by capacitor A2Q3. Resistor A2B9 is the load resistor which conducts forward biases diode A2Q3 and charges capacitor A2Q9. This capacitor will charge rapidly but has a long discharge time, since the only resistance across it is the high resistance of the circuitry. Diode A2Q3 prevents discharge through components on the anode side, since it becomes back biased to this voltage. This voltage on A2Q9 is applied to the emitter of switch stage A2Q4. For the duration that the voltage on A2Q9 is applied to the emitter of this stage, the voltage on time constant circuit A2Q9-A2Q10 drops below that on A2Q9, transistor switch A2Q4 conducts heavily. When A2Q4 saturates, all elements drop very close to ground potential. This grounding both the gain control circuits and start to discharge rapidly. If, during this time, new information is received in the IF Amplifier, the system recovers itself based on the amplitude of the new information. The DC voltage on time constant circuit A2Q9 is the AGC voltage. Stages A2Q5 and A2Q6 are direct coupled emitter followers. They act as an impedance transformer which provides a high impedance across time constant circuit A2Q9 so as not to decrease the discharge time. From the low impedance side of the transformer, the DC is applied to AGC attenuator A2R14. This control sets the AGC voltage applied to the IF amplifier. This same value of plus AGC voltage is applied through diodes A2Q4 and A2Q5, to RF AGC attenuator A2R14. The forward voltage drop across the two diodes in series provides a threshold above which AGC voltage is applied to the amplifier stage A2Q8. AGC gain is limited by front panel control R1. This control provides a small plus DC voltage which, applied to A2Q4, is used to over-ride the normal AGC voltage applied to the base of A2Q7. This allows the RF manual gain control to de-sensitize the IF Amplifier. Stage A2Q7 is used to invert the positive AGC voltage to a negative voltage of greater amplitude. This is necessary since it is applied to grids of some of the tubes in the IF Amplifier. The negative voltage from the collector of A2Q7 is applied through diode A2Q27 to pin 5 of J1. The diode is necessary, since the voltage from A2Q7 swings slightly positive. The diode prevents more than a fraction of a volt (positive) from reaching the tube grids. A portion of the RF AGC voltage is applied to pin 7 of J1. This negative voltage is used as a signal strength indication by an 8 meter on the front panel. Diode A2Q35 is not needed for the 8 meter application, it is used in the transmit mode.
87. (Contd)
The output from the voltage divider is coupled by capacitor A103 to the base of 1.75 Mc IP amplifier A102.

88. The gain of 1.75 Mc amplifier A102 is controlled by AGC degenerator A103. AGC degenerator A103 acts as a variable resistive-degenerative element in series with emitter bypass capacitor A105. The base voltage for AGC degenerator A103 is developed from the 20-volt dc supply line by voltage divider A106, A107, A108 and the collector-to-emitter resistances of AGC attenuator A104. With weak received signals, the output from the step AGC circuit will be zero, causing AGC attenuator A104 to be cutoff. This provides maximum shunt resistance (less attenuation), biasing AGC degenerator A103 into saturation, and effectively grounding emitter bypass capacitor A105. Therefore, the output from 1.75 Mc IP amplifier A102 will be maximum. As the signal strength increases, AGC attenuator A104 will conduct. The amount of conduction will be controlled by the received signal strength (above AGC threshold). The shunt resistance will decrease as the rate of conduction increases, decreasing the amount of signal applied to the base of 1.75 Mc IP amplifier A102. As the rate of conduction of AGC attenuator A104 increases, the dc voltage present at the collector will decrease. Therefore, the bias level on AGC degenerator A103 will decrease, decreasing its rate of conduction. This will increase the impedance in series with emitter bypass capacitor A105, providing increased degeneration to decrease the gain of 1.75 Mc IP amplifier A103 at a nearly constant level for variations in the level of the input signal. The output from 1.75 Mc IP amplifier A102 is developed across the tuned circuit consisting of transformer A107 and capacitor A105. From here, the IP signal is coupled by capacitor A107 to the base of 1.75 Mc IP amplifier A104, and by capacitor A1043 to the base of 1.75 Mc IP amplifier A105.

89. The 1.75 Mc IP amplifier, A105, raises the level of the 1.75 Mc signal and develops it across the tuned circuit consisting of capacitor A105 and the primary of transformer A107. Transformer A107 couples the 1.75 Mc signal to connector J1A3 for application to the IF OUT connector on the front panel of the RT-662/GRC. This allows the 1.75 Mc signal to be used for external purposes. The 1.75 Mc IP amplifier A104 raises the level of the 1.75 Mc signal and develops it across tuned circuit A109-A102. A102 uses a push-pull output winding to couple the signal to the product detector.

The Product Detector (fig 1010)

90. The product detector is used to recover the audio information from the receive IF signals. The input to the product detector is the 1.75 Mc IF output from IP amplifier A104. The input signal is applied to the bases of transistors A228 and A229, which are connected in a balanced mixer configuration. Base bias for transistors A228 and A229 is developed by voltage divider A110, A117, and is applied through the secondary of transformer A112. The collector voltage for transistors A228 and A229 is applied through the primary of transformer A112. In all modes of operation, except CW, dipoled gate A309 (fig 1040) is forward biased by the voltage developed by voltage divider A309, A314. This allows the 1.75 Mc present at connector J1A4 to be coupled through diode A309 to attenuator A3011, A3012 by capacitor A3013. Resistor A3011 sets the level of the 1.75 Mc signal that is coupled by capacitors A2214 and A2213 to the emitters of transistors A228 and A229. During CW operation, the output from the BFO circuit is applied to the emitters of transistors A228 and A229 in lieu of the 1.75 Mc injection present at connector J1A4. The 1.75 Mc IF and the 1.75 Mc injection or BFO signals are mixed by transistors A228 and A229, (fig 1040) resulting in an output consisting of the sum of the two signals, and the difference between the two signals (the desired audio). Capacitors A2215 and A2216 bypass the sum of the two signals. Since the circuit is balanced, the 1.75 Mc outputs from transistors A228 and A229, developed across the primary of transformer A223, are 180 degrees out of phase with each other. This results in the cancellation of both the 1.75 Mc injection or the 1.75 Mc IF. Transformer A223 has an audio frequency response that will attenuate any of the RF signals not previously cancelled. The difference between the two signals (the desired audio), is coupled by capacitor A2217 to the base of amplifier A2210. Amplifier A2210 raises the level of the audio signals and develops them across collector resistor A2212. The output from amplifier A2210 is coupled by capacitor A2220 to pins 29 and 30 of connector J1 for application to receiver audio module 1A10 and the AUDIO GAIN control on the RT-662/GRC front panel.

BFO Circuit Description

91. In the CW mode of reception, a BFO injection frequency of 1.752 Mc ± .0035 Mc is created. This is applied to the product detector instead of the usual 1.750 Mc in other receive modes. This is necessary because the CW signal transmitted by the AM/GRC-105 is always 2 kHz above the indicated frequency on the tuning controls. In all modes of reception except CW, 1.75 Mc is injected into the product detector.
This injection frequency is derived from the Frequency Divider subassembly and is applied to diode gate A3CR5. (Fig 1009). In all modes, except CW, this gate is forward biased to pass the injection signal. Diode gate A3CR4 is back biased to prevent loss of signal through the EFO circuitry. In the CW mode diode gate A3CR5 is back biased and A3CR4 is forward biased. This allows the EFO injection frequency to be applied to the product detector. The EFO injection frequency is derived from the difference frequency of two crystal oscillators. (Fig 1009), A3C4 is a crystal oscillator having a frequency of 7 Mc, as controlled by crystal A3H1. A3Q2 and associated circuitry is also a crystal oscillator having a center frequency of 8.752 Mc, as controlled by crystal A3Y2. This stage is also used as a mixer and the 7 Mc signal from A3Q2 is injected into its base circuit. The difference product of the two oscillators is selected by the tuned circuit in the collector of A3Q2. This signal having a centre frequency of 1.752 Mc is applied to isolation emitter follower A3Q3 from which it is applied to diode gate A3CR4. This injection signal is attenuated by A3R1 before application to the product detector. This same attenuator acts on the 1.750 Mc signal from gate A3CR5 in the other receive modes.

So that the operator may adjust the EFO injection frequency over a small frequency range, the frequency of crystal A3Y2 can be pulled a small amount. This is accomplished by a variable capacitor A3CR4. The mode of this diode has a small positive bias as determined by the drop across diodes A3Q2 and A3Q3 in series, which can be varied by a front panel control, and is applied to the cathode of A3CR4. Since the voltage variable capacitor is back biased, the difference of the two positive voltages, its effective capacitance will be controlled such that the frequency of the crystal A3Y2 can be varied by a few kilocycles higher in frequency. This is accomplished, as the front panel control increases the back bias, by increasing the positive bias applied to the cathode of A3CR4. As the back bias increases the capacitance becomes smaller. Capacitor A3Q8 is in series with the variable capacitor to ground. Its effect can be ignored as its impedance is small at the frequency of 6.752 Mc. Variable resistance A3R4 is in series with the front panel control and can be used to set up the range of frequency variation desired. Inductance A3L3 can be used to adjust the center frequency about which the EFO frequency can be varied. This circuit is activated only in the CW mode of reception. Application of +200Vdc to pin 10 of J4 accomplishes this.

THE BALANCED MODULATOR (Fig 1009)

93. The balanced modulator is used to create the sidebands and to suppress the carrier in SSB transmission. The desired sideband can then be selected by a suitable filter. The function of the balanced modulator, as used in this equipment, is to combine the 1.75 Mc IF frequency with the modulating signal in such a manner that the side frequencies or mixer products of the modulation process are obtained without passing the 1.75 Mc carrier.

94. Since the modulating process is a mixing process, the side frequencies obtained will consist of the mathematical sum and difference of the two original frequencies. A spectrum analysis of these output signals shows that they consist of an upper and a lower sideband equally displaced on each side of the original carrier frequency. A similar set of sidebands will appear displaced about the second harmonic and also about some other harmonics of a higher order. The original carrier frequency will not appear in the output, since the circuit is balanced to this frequency. The desired sidebands consist of a series of pulses whose polarity and repetition rate are determined by the switching or carrier voltage and whose amplitude is controlled by the audio or modulating signal. To suppress the 1.75 Mc carrier voltage to as low a value as possible, it is necessary to balance the circuit for both resistance and capacitance. Both the modulating frequency and the carrier frequency voltages are applied to the center tap of a balanced transformer. The diodes A and B are selected to have the same characteristics, especially in their forward conducting resistance. The resistances in the circuit are arranged symmetrically with A3R4 (Fig 1009) connected so as to allow a resistive balance to be made. Capacitor A3C7 is connected across the side having the lowest distributed capacitance to ground. It can be created to balance the capacitance at the carrier frequency. The transformer A3T2 is tuned to the carrier frequency. Balance is achieved at the carrier frequency and, as the voltages are equal and of opposite phase on each half of the circuit, the carrier frequency will not appear across the primary of A3T2 and hence does not appear in the secondary.

95. When an audio modulating voltage is present the two diodes conduct alternately and thus upset the balance of the circuit at the frequency of the mixer products. The circuit is balanced only to the carrier frequency and not to the sidebands. Therefor, these frequencies appear across the primary and secondary of transformer A3T2. The diodes will also conduct in proportion to the amplitude of the audio signal frequency and therefore they control the amplitude of the sideband frequencies.
96. In summary, then, the action of the balanced modulator is to produce two sidebands, with the original carrier frequency suppressed at the output. An upper sideband is produced which is the sum of the carrier frequency and the audio signal frequency and the lower sideband produced is the difference of the carrier frequency and the audio signal frequency. Note that the output of a balanced modulator contains both sidebands as no filtering action takes place in the device.

Circuit Description of the Balanced Modulator and USB Crystal Filter (Fig 1009)

97. A transmit function is included in the Receiver IF Subassembly. This is the balanced modulator and USB filter circuitry. During transmit operation, the 1.75 Mc output from frequency dividers module 1A6 is applied to connector J4A4, from which it is coupled to the collector of 1750 kc switch ALG2. In transmit, pin 9 of connector J1 has 20 volts dc applied. This 20 volts dc is used to bias 1750 kc switch ALG2 on. When the switch turns on, it presents a small series resistance to the main audio channel. Therefore, the output in combination with resistor ALR1 forms a voltage divider to set the level of the 1.75 Mc coupled to the center-tapped primary of transformer ALZ2.

98. The 1.75 Mc output from 1750 kc switch ALG2 is applied to the center-tap on the primary of transformer ALZ2. The audio input from transmitter IF and audio module 1A5 is applied to pin 3 of connector J1, from which it is applied to the center-tap of the primary of transformer ALZ2. The audio and 1.75 Mc inputs are mixed by backward diodes ALVR1 and ALGR. Resistor ALR1 and potentiometer ALR4 are used to resistively balance both arms of the balanced modulator circuit. Capacitor ALR7 is used to balance any reactive components in the circuit. Therefore, the circuit is set so that both arms are balanced.

99. When the set is placed in tune condition, a ground is applied to pin 13 of connector J1 from the AM-33A/GR-106 power amplifier in order to effectively turn off the balanced modulator in this condition. This ground is applied to the base of 1750 kc switch ALG2, shutting it off, thus blocking the 1.75 Mc injection at the collector. When the RF-652/GRG goes to receive operation, ground is applied to pin 9 of connector J1, shutting 1750 kc switch ALG2 off to turn off the balanced modulator. When the 20 volts dc is initially applied (transmit mode), capacitor ALG2 will charge through resistors ALR1 and ALR3. The voltage on capacitor ALG2 is the voltage applied to the base of 1750 kc switch ALG2. Therefore, since the base voltage is increasing exponentially, 1750 kc switch ALG2 will be turned on exponentially. This delays the IF output from the RF-652/GRG, preventing the AM-33A/GR-106 power amplifier from being overdriven before the automatic level control signals have time to apply their control.

100. During transmit operation, ground is applied to pin 2 of connector J1 and 20 volts dc is applied to pin 9 of connector J1. The ground is applied to the anode of diode ALGR4, and the cathode of diode ALGR3. The 20 volts dc is applied to the cathode of diode ALGR4, and the anode of diode ALGR3. Therefore, diode ALGR3 will be forward biased. The output from buffer amplifier ALG1 is coupled by capacitor ALG9 to diode ALGR3. Since diode ALGR3 is forward biased, the signal will pass and be coupled to filter PL1. Filter PL1 removes the lower sideband component of the signal and further attenuates any of the 1.75 Mc carrier that was not cancelled by the balanced modulator circuit. The upper sideband 1.75 Mc IF is applied to connector J4A4 for application to transmit IF and audio module 1A5.

Receiver Audio Subassembly 1A10

101. The Receiver Audio Subassembly contains two audio amplifiers and the squelch control circuitry.

General

An audio squelch circuit is one that suppresses receiver background noise when no signal is coming through the receiver system. The operation of the squelch control circuit is based on the power distribution curve of voice power to voice frequency. Most of the voice power is concentrated in the range from 400 to 600 cps.
Noise energy is more nearly equally distributed throughout the audio range. By diverting the audio signal through both a low pass filter and a high pass filter, one will pass essentially voice signals and the other will pass essentially noise signals. In this manner it is possible to develop control signals to operate the squelch functions.
102. In the audio output circuit a "Sensor" is used as a small, low power temperature sensitive resistor having a positive temperature-coefficient (fig 1011-B11) and is particularly suited for bias compensation against temperature changes. Fig 11 is a simplified block diagram of the Receiver Audio Subassembly.

Circuit Description of the Receiver Audio Subassembly (fig 1011)

103 The Receiver Audio Subassembly provides two outputs. One at 10 mW for headphone use and another at 2 watts for loudspeaker use. Since the audio input can contain noise as well as voice, a squelch circuit is employed in this subassembly to mute background noise in the absence of a received voice signal.

104. The audio output from receiver IF, module 4A7 is applied to pin 12 of connector J1 through the AUDIO GAIN control on the RT-662/GRC front panel. The AUDIO GAIN control is used to vary the level of the audio signal coupled by capacitor A2C1 to the base of aqulch gate A2Q3. If the SQUELCH switch is set at OFF, a ground will be present at pin 15 of connector J1. This ground will be applied to emitter resistor A2R5, to complete the emitter circuit and allow an output from squelch gate A2Q3 to be developed.

105. If the RT-662/GRC is being operated in the CW or PSK mode of operation, a ground is applied to pin 5 of connector J1. This ground will be applied through diode A2CR2 to terminate emitter resistor A2R5. If the SQUELCH switch is set at ON, the squelch circuit will compare the voice level to the noise level. If the voice is predominant, squelch switch A2Q4 will be biased on, effectively terminating emitter resistor A2R5 to ground through the small collector-to-emitter resistance of squelch switch A2Q4. If the incoming signal is predominately noise, squelch switch A2Q4 does not conduct. Therefore, resistor A2R5 will be open and the input will not be allowed to pass (will be squelched). In order that the operator can be aware of the presence of signals when the unit is squelched, a bypass path is provided through resistors A2R2 and A2R1. Therefore, the operator is aware that the set is operating. If it is necessary to receive signals that are below the squelch threshold, the SQUELCH switch can be set at OFF to allow the full audio output to be available. Resistor A2R2 is normally set to provide a squelched to non-squelched ratio of 20 dB at the audio outputs.

106. If emitter resistor A2R5 is grounded, the audio signals present at the base of squelch gate A2Q3 will be developed across emitter resistor A2R5. The audio is then coupled by capacitor A1G2 to the base of 10 mW output amplifier Q4 and to the base of audio driver Q2. Capacitors A2G6 and A2G7 are used to block dc from the input and equalize the low frequency response of the two channels. Resistors A2R11 and A2R12 are used to compensate for the amplifier input requirement so that each of the two channels can simultaneously produce its required output from a common source.

107. The audio signal is raised to a level of 10 milliwatts by output amplifier Q4. Inductor L1 is used to provide frequency dependent degeneration, in order to provide roll-off of frequencies above the 3500 Hz voice range. Collector-to-base feedback (through resistor R8) is used to improve the stability and minimize the distortion of 10 mW output amplifier Q4. The output from 10 mW output amplifier Q4 is developed across the primary of transformer T1. Transformer T1 couples the audio signals to pin 14 of connector J1 for application to the AUDIO connectors on the RT-662/GRC front panel. The 10 milliwatt output is used to drive the handset H-227/U or handset H-53/PT. Capacitors C5 and C6 are used to bypass signals above 3500 Hz. Transformer T1 transforms the output impedance of amplifier Q4 to the desired 500 ohms for matching the impedance of the H-53/PT and H-227/U.

108. Audio driver Q2 raises the audio signals to a level sufficient to drive 2 watt push-pull output amplifier Q3 (A and B). Degeneration (developed by resistor R8) and collector-to-base feedback (through resistor R5) are used to improve the stability and minimize the distortion of audio driver Q2. The output from audio driver Q2 is developed across the primary of transformer T2. Transformer T2 couples the signal to the bases of 2 watt push-pull output amplifier Q3. Base bias for 2 watt push-pull output amplifier Q3 is developed from the 20 volts d.c. supply by the temperature compensated voltage divider consisting of resistors R10 and R12 and sensor R11. Collector-to-base feedback (through capacitors C6 and C7) is used to provide roll-off for frequencies above 3500 Hz. The 2 watt push-pull output amplifier, A3, raises the level of the audio signals to 2 watts. This output is applied to pin 15 of connector J1 for application to the AUDIO connectors on the RT-662/GRC front panel. This output is used for driving the loudspeaker LS-165/67.
109. The audio output from receiver IF module A7, which is applied to the AUDIO GAIN control, is also applied to pin 6 of connector J1. From pin 6 of connector J1, the audio is coupled by capacitor C101 to a voltage divider consisting of resistor A121 and the collector-emitter resistance of A12 to a voltage divider consisting of resistor A121 and the collector-emitter resistance of A12. The collector-emitter resistance is inversely proportional to the level of the signal input, as determined by the output from AGC dc amplifier A143. The voltage divider provides a nearly constant output, which is coupled by capacitor A120 to the base of AGC AF amplifier A143. Resistor A122 is used to isolate the output voltage from the input impedance of AGC AF amplifier A143 in order to ensure maximum control range. The audio output from the voltage divider is raised in level by AGC AF amplifier A142, which is coupled by capacitor A104 to the base of AGC AF amplifier A143. Degeneration (developed by resistor A106) and collector-to-base feedback (through resistor A145) are used to improve the stability and minimize the distortion of AGC AF amplifier A142.

110. AGC AF amplifier A144 further raises the level of the audio signal and develops it across the primary of transformer A145. Collector-to-base feedback (through resistor A146) is used to improve the stability and minimize the distortion of AGC AF amplifier A144. Transformer A145 couples the audio output from AGC AF amplifier A144 to high-pass filter A2L1, A1401, and an AGC feedback circuit consisting of A1402, A1403, and AGC attenuator A1404 and AGC dc amplifier A143. This circuit forms a closed AGC loop with AGC audio amplifier A142 and A144. Zener diodes A1402 and A1403 provide clipping for any peaks that exceed their firing points.

111. The audio output from AGC AF amplifier A144 is detected by AGC rectifier A1401. This voltage is filtered by capacitor A1406 and used as a dc signal for AGC dc amplifier A145. The dc output from A1401 is coupled to the base of AGC audio amplifier A141. The dc output from A1401 is coupled to the base of AGC audio amplifier A141. The signal signal is then amplified by AGC audio amplifier A141. This will decrease the input to AGC AF amplifier A142. Similarly, the signal decreases, the collector-to-emitter resistance of AGC attenuator A141 increases, increasing the signal level at the base of AGC AF amplifier A142. Since this is a closed loop, the input of AGC AF amplifier A142 is maintained at a nearly constant level after the initial stabilization.

112. Low-pass filter A2L1, A1010 allows only the portion of the input frequencies approximately between 500 and 600 Hz to pass to the base of voice sensing detector A145. The positive portions of the applied signals will be rectified by detector A145. Therefore, voice sensing detector A145 will act as a half-wave rectifier. This positive dc output is filtered by capacitor A1406 and coupled to one end of resistor A2R10 (SQUELCH SENS control).

113. High-pass filter A2GL, A2L2 allows only the portion of the input frequencies above approximately 1200 Hz to pass to the cathode of noise sensing detector A2R3. Noise sensing detector A2R3 rectifies the negative portions of the signals. This negative dc potential is filtered by capacitor A205 and applied to the other end of resistor A2R10 (SQUELCH SENS control). Since voice energy is concentrated primarily in the 500-600 Hz range and the received noise energy is equally distributed throughout the audio range, the two filter circuits allow discrimination of voice input from noise input conditions. In the absence of voice input, approximately equal signals will pass through the two filters, with the result that the dc output at the wiper of resistor A2R10 will be insufficient to cause squelch switch A2Q2 to conduct. When voice is present, most of its energy will pass through the low-pass filter causing an increased positive dc output on the wiper of resistor A2R10. If the voice level is sufficiently above the ambient noise, the resulting dc output at the wiper of resistor A2R10 will be sufficient to cause conduction in squelch switch A2Q2. Resistor A2R10 is set so that ratio between the voice and noise must be of a predetermined value, before squelch switch A2Q2 will conduct.

114. If the S + N ratio is at a predetermined value and voice is predominant, the voltage on the N-wiper of resistor A2R10 will forward bias squelch switch A2Q2. Squelch switch A2Q2 will conduct and its output will be filtered by capacitor A2Q2. If the SQUELCH switch is set at ON, squelch switch A2Q2 will be biased on and conduct. When squelch switch A2Q2 conducts, emitter resistor A2R3 will be grounded through the small collector-emitter resistance of squelch switch A2Q2, allowing the audio to pass to the amplification circuits as previously described. If the noise predominates, the voltage at the wiper of resistor A2R10 will not be sufficiently positive to bias squelch switch A2Q2. Therefore, resistor A2P will not be grounded. This keeps squelch gate A2Q3 non-conducting forcing the audio signals to pass through resistance divider A2R1 and A2R2 and be squelched.
THE NOISE BLANKER, MODULE 1A6 (Fig 1012)

General

115. The Noise Blanker subassembly is a part of the chassis. Its purpose is to reduce the effect of impulse type noise by gating the output of the translator subassembly just before the pulse arrives and slightly longer than the pulse duration. It is imperative that noise be removed before the IF filter such that ringing does not further stretch the noise pulse, and before the AGC detector to prevent noise from activating the AGC.

116. The noise blanker is designed to reduce impulse noise only. Impulse noise, because of the short duration of the pulses compared with the time between them, must have high amplitude to contain much average energy. Hence, noise of this type, strong enough to cause much interference, generally has an instantaneous amplitude much higher than that of the signal being received. The approach used here is to silence or mute the receiver during the duration time of any individual pulse. The listener will not hear the "hole" because of its short duration, and very effective noise reduction is obtained. In passing through selective receiver circuits, the time duration of the impulses may be increased because of the of the circuits. Thus, the more selectivity ahead of the noise reducing device, the more difficult it becomes to secure good impulse type noise suppression.

117. Therefore, the signal plus noise is diverted into a separate channel close to the input end of the receiver. A decision based on the relative amplitude of noise to signal is made and if the presence of noise pulses is determined, a regenerated pulse is formed to gate the signal path of the receiver further along the path. The gating must occur before the original noise pulse reaches the point where the signal path is interrupted. This requires that the bandwidth of the blanker channel be wider than the bandwidth of the receiver up to the point of gating.

118. The noise blanker is designed to operate on impulse noise only. In general, this type of noise will be "ran made" and may be generated by internal combustion-engine ignition systems, by power line discharges, by diathermy machines, by motor brush sparking, and by other electrical devices. Fig 12 shows a simplified diagram of the Noise Blanker subassembly.

**Fig 12 - Block diagram of the Noise Blanker assembly**
Circuit Description of the Noise Blanker (fig 1012)

119. In most systems of this nature a clear channel outside of the tuning range of the receiver is used to sense the presence of noise. It is assumed that the noise is also present at the frequency to which the receiver is tuned. A separate tuned RF Amplifier is used to select the noise band and amplify the noise pulses. The amplified pulses are then used in a balanced gate to open the signal path of the receiver without re-introducing noise.

120. The noise blanker used in this receiver actually senses the noise within the RF band in use, and thus, takes advantage of the normal antenna. The noise blanker does not employ an RF Amplifier with tuned stages as this would tend to lengthen the noise pulses and make noise suppression harder to achieve. Instead, the signal plus noise is fed directly from the antenna to a wide band amplifier. The circuitry produces a fixed width pulse for every noise pulse at the input. This pulse is then used to block the injection signal from the 10-1 kc synthesizer to effectively mute the receiver.

121. From J6 on the receiver front panel the antenna signal is applied to a resistor voltage divider. This divider is made up of resistor R10, R16 shown in A7 in the chassis, (fig 1025) and resistor R1 on the Noise Blanker schematic (fig 1012). A small part of the antenna signal is applied to the amplitude limiter CR1-CR2. Only signals such as noise peaks, which are much greater in amplitude than the average signal noise level, will be sensed by this circuit. The output from the limiter is fed to the noise of video amplifier Q1. The output from video amplifier Q1 is coupled to the base of video amplifier Q2 by capacitor C5. Video amplifier Q2 is identical to video amplifier Q1, except for the increased stability obtained by the by-passed emitter resistor R9. Diodes CR3 and CR4 prevent peaks in the output from video amplifier Q1 from overloading video amplifier Q2.

122. The output from video amplifier Q2 is coupled by capacitor C9 to diode CR5. Diode CR5 detects the positive portion of the output from video amplifier Q2. Limiter CR6, CR7 eliminates any pulse still present in the signal. The output from diode CR5 is raised in level by two successive identical pulse amplifiers (Q3 and Q4). The output from pulse amplifier Q4 is coupled by capacitor C10 to diode CR8. Diode R19 and capacitor C16 create a positive going and a negative going pulse from the square wave. The positive portion of the pulse is shorted to ground through diode CR9. The output from diode CR8 is applied to one-shot multivibrator Q5, Q6.

123. One-shot multivibrator Q5, Q6 will produce a negative pulsed output each time a noise pulse is present in the received signal. This pulse will have a fixed width regardless of the width of the trigger pulse. The width of this pulse is 50 microseconds ± 50 microseconds. This square wave pulse is integrated by resistor R28 and capacitor A1C20 (in the 10 and 1 kc synthesizer subassembly fig 1022) so as to slightly slope the sides of the square wave. This is done to prevent ringing in the gating circuit of the 10 and 1 kc synthesizer. This pulse is applied to connector A1J2, from which it is applied to 10- and 1-kc synthesizer module 1A4. The output pulse width from one-shot multivibrator Q5, Q6 (fig 1042) is such that the output from transistor module 1A8 will be disabled slightly before the pulse arrives and slightly longer than the duration of noise pulse. Noise BLANKER switch 1A4A2 applies regulated 20 volts do or grounded to noise blanker 1A4A5 to control its on/off operation.

TRANSMITTER IF AND AUDIO SUBASSEMBLY 1A5 (Figs 1013 to 1015)

Functions

124. The functions accomplished in the Transmitter IF and Audio Subassembly are as follows:

a. Amplify and regulate the Audio signal applied to the balanced modulator.

b. Produce the 2 kc injection signal required for CW transmission.

c. Provide a Vox capability.

d. Develop control voltages for and amplify the transmit IF Signal.

e. Perform the primary transmitter keying.

Automatic Level Control

125. Control of the power output of the final RF Power Amplifier, AM3348/CRG, is accomplished by a closed loop system of which the transmitter IF and Audio Subassembly is a part. Peak power control (PPC) and average power control (APC) are used to automatically maintain the desired power output from the transmitting system. The control signals are applied to the Transmitter IF Amplifier stages for this purpose.
126. In the AN/GEC-106 system, two separate means of automatic power level control are employed. One, the Peak Power Control, is designed to adjust the system gain to prevent the Power Amplifier stages from being overloaded on modulation peaks, while the second control, the Average Power Control, is designed to keep the long term average power output constant. The control functions are accomplished by feeding DC voltages back to two variable-gain stages in the Transmitter IF and Audio subassembly, a part of Receiver-Transmitter, RT-662/GRC.

127. To effectively perform their separate control functions, the PPC and APC DC control signals must have specific characteristics. The PPC DC Control voltage is processed such that it has a fast attack, but slow release; the time constants being chosen to make the PPC able to react to sudden modulation peaks but to "hang on" between pulses coming at a syllabic rate. Thus, the control voltage finds a level that preserves the final power output stage to be driven to full power on modulation peaks.

128. The APC DC control is a control device that restricts the average power output of the power amplifier to a level which it can maintain continuously. Since the linear power amplifier is designed for single sideband or multiplexed data transmission, it must be capable of high peak power output. This output must be maintained with good linearity, therefore, the tubes must not saturate or be emission limited. For the above reasons the APC DC control circuit has a long time constant such that it does not react to high peaks, but rather to the real average power. Automatic control is desirable because a simple potentiometer method would require that the operator constantly monitor power output. The gain of the transmitter varies both with temperature and with transmitted frequency. Once the system has been adjusted to a particular power output, this level should remain constant. The APC circuitry accomplishes this.

129. Since duty cycle varies with the particular mode of transmission, it is evident that one adjustment for average and peak power output will not be satisfactory. Provision is made so that different values of average and peak power can be realized depending on the mode of operation; fig 13 is a simplified block diagram which illustrates the control loop involved for both PPC and APC.

**PPC and APC Control Circuits**

**General**

130. The PPC and APC control circuitry in the subassembly processes the modulated DC output from the operate ALC (automatic level control) circuit in the AM-3349/GRC-106 Power Amplifier. Since each mode of transmission requires a different value of control voltage, a divider network is provided in the chassis of the receiver-transmitter. (Fig 1026) Fig 14 provides a simplified schematic of the control and divider circuit.

**Control and Divider Circuit**

131. After passing through a suitable decoupling circuit the DC signal is applied to two divider networks. The APO network is composed of control potentiometer R14 and resistors R4, R5, and R6. Switch S4 selects the desired portion of the APC signal from the divider network according to the mode of transmission in use.

132. The PPC network is composed of control potentiometer R15 and resistors R21, R20 and R19. All modes of transmission take a signal from the junction of R15 and R20. In the CW mode an additional resistor, R19, is added to the voltage divider string. Fig 14 through 17 are simplified diagram showing the circuitry in the chassis for each switch position.

133. This divider network converts the operate automatic level control (CALC) circuit from the PA to the proper level for application to the PPC and APC circuitry. The PPC signal is applied to pin 8 of connector J1 (Fig 1014), from which it is applied through resistor A3R13 to the base or emitter follower A3Q4. Any RF signals present in the input are bypassed by capacitor A3C4. Emitter follower A3Q4 provides isolation between the divider network on the chassis and the peak detection circuit (capacitor G5 and resistor R5).

134. The output from emitter follower A3Q4 is used to charge capacitor A3C5, providing the signal for a second emitter follower A3Q5. The charge time constant for capacitor A3C5 is very small, allowing it to charge to the peak level of the applied signal. The discharge path is through resistor A3R8. The discharge time constant is long compared to the frequency of the applied signal, but is short enough to follow the syllabic rate to maintain the average talk power and still hold the peak envelope power within the design limits. This action tends to compress the RF voice signal and thereby change the peak-to-average ratio to improve system performance.
FIG. 13 - BLOCK DIAGRAM OF CONTROL LOOP FOR APC AND PPC
The voltage on charged capacitor A3C6 is the DC signal for emitter follower A3Q2. A3Q2 provides isolation between the modulation wiper and the APC filter circuit (resistor A3R5 and capacitors A3C5 and A3C6). As emitter follower A3Q2 is turned on by the DC signal on capacitor A3Q2, capacitor A3C6 will rapidly charge through the small collector-to-emitter resistance of emitter follower A3Q2. The discharge path for these capacitors is through resistor A3R5. The RC time constant of the discharge path is very long compared to the frequency of the applied signal. Therefore, the voltage of charged capacitors A3C3 and A3C6 will be maintained at a nearly constant level for a given output from the AM-3349/GRC-106. This voltage is used as the DC signal for emitter follower A3Q3.

A3Q3 provides the required isolation between APC attenuator A1Q4 and the APC filter circuit. The output from emitter follower A3Q3 is applied to the base of APC attenuator A1Q1, determining the amount of attenuation for the IF signal applied to the RF amplifier A2Q5. This closes the IF loop between the AM-3349/GRC-106 output and the RF-662/GRC input to prevent the peak power of the transmitted signal from exceeding a predetermined level.

During transmit operation, the APC signal is applied to pin 4 of connector J1 for application to the receiver level meter. The receiver level meter then provides an indication of the amount of APC signal required to control the RF power output level. In the receive mode of operation, the output from the RF APC circuit in the receiver IF subassembly is applied to the APC level meter. Diode A3C8 provides the path to ground for this negative APC signal. Resistor A3R10 isolates the APC voltage from the emitter of RF amplifier A3Q5. The similar path to ground for the APC signal is located in the RF receiver IF subassembly. Fig 10 shows this circuitry.

When the RF-662/GRC is used alone or if the AM-3349/GRC-106 is not functioning, the output from internal APC assembly A1A5 is applied through pin 6 of connector J1 and diode A3C8, to the base of emitter follower A3Q4. This signal is then used to generate the APC signal required in the previous example. When the RF-662/GRC is operated with the AM-3349/GRC-106 functioning, the output from the RF APC circuit on the chassis will reverse bias diode A3C8 and override the output from internal APC assembly A1A5.

APC Control Circuitry

The input to the APC circuit is the output from the receiver IF subassembly. This signal has the positive peaks of the detected signal riding on a DC level. It is applied to pin 7 of connector J1, (Fig 10)(a) from which it is applied to the base of emitter follower A3Q4. A3Q4 is in the voltage divider network on the chassis from the modulation wiper. Capacitor A3C1 is an RF bypass for any RF signals that may be present in the signal. The output from emitter follower A3Q4 is applied to the modulation wiper.

The modulation wiper consists of resistors A3R2, A3R3, A3R4, and A3R12, diode A3C8, and capacitors A3C2 and A3C3. The function of the modulation wiper is to average the peaks of the applied signal, produced by the APC output which is proportional to the average power output from the AM-3349/GRC-106. During operation, the modulation wiper will set the average level and ignore the presence of modulation. This ensures that the power level of transmission will remain the same. Capacitor A3C2 charges on the positive-going slope of the applied signal, through resistor A3R3. The time constant of resistor A3R3 and capacitor A3C2, in combination with the division action of resistors A3R3 and A3R4, is such that capacitor A3C2 charges to the average level of the applied peaks. On the negative-going slope of the applied signal, the voltage of charged capacitor A3C2 will forward bias diode A3C8 and the parallel combination of resistors A3R2 and A3R12. (Ground is present at pin 24 of connector J1 during transmit operation). The discharge constant is very short, allowing the capacitor to rapidly discharge as the negative-going slope of the applied signal goes toward zero. This ensures that the charge created by the next positive-going slope starts near zero, thereby preventing the APC voltage from creeping up and allowing the APC loop to decrease the average power output from the AM-3349/GRC-106.

The voltage on charged capacitor A3C2 is the signal for emitter follower A3Q2. A3Q2 provides isolation between the modulation wiper and the APC filter circuit (resistor A3R5 and capacitors A3C5 and A3C6). As emitter follower A3Q2 is turned on by the DC signal on capacitor A3Q2, capacitor A3C6 will rapidly charge through the small collector-to-emitter resistance of emitter follower A3Q2. The discharge path for these capacitors is through resistor A3R5. The RC time constant of the discharge path is very long compared to the frequency of the applied signal. Therefore, the voltage of charged capacitors A3C3 and A3C6 will be maintained at a nearly constant level for a given output from the AM-3349/GRC-106. This voltage is used as the DC signal for emitter follower A3Q3.

A3Q3 provides the required isolation between APC attenuator A1Q4 and the APC filter circuit. The output from emitter follower A3Q3 is applied to the base of APC attenuator A1Q1, determining the amount of attenuation for the IF signal applied to the RF amplifier A2Q5. This closes the IF loop between the AM-3349/GRC-106 output and the RF-662/GRC input to maintain the average power level of the transmitted signal at a predetermined value.

During receive operation, pin 24 of connector J1 has 20 volts DC applied to it. This 20 volts is divided by resistors A3R12 and A3R2 and is used to charge capacitor A3C6, thus providing an APC output from emitter follower A3Q2. Therefore, when the RF-662/GRC is keyed by the voice input (vox or push to vox operation), there will be APC control for the initial peaks, preventing the AM-3349/GRC-106 from being overdriven. Once
keyed, ground is applied to pin 24 of connector J1, providing a discharge path for capacitor A302. The circuit will then be controlled according to the average power output from the AM-3349/GRC-106 as previously explained.

143. When the RT-662/GRC is operated without the AM-3349/GRC-106, the output from internal ALC assembly 4A4A5 is applied from pin 6 of connector J1 through diode A3CR6 to generate the necessary AFO signal as previously explained. When the RT-662/GRC is operated with the AM-3349/GRC-106 functioning, the output from the divider network on the chassis is of sufficient level that it will reverse bias diode A3CR6 and over-ride the internal ALC signal.

FIG 14 - ALC SWITCHING IN RT-662/GRC ON SSB-NSK

CR7 AND CR8 ARE ISOLATING DIODES
CR7 AND CR8 ARE ISOLATING DIODES

FIG 15 - ALC SWITCHING IN RT 662/GRC ON FSK
CR7 and CR8 are isolating diodes

FIG 16 - ALC SWITCHING IN RT-660/ARC ON AM
**Fig 17 - ALC Switching in RT-662/GRC on CW**

CR7 and CR8 are isolating diodes.
FIG 16 - PPC and AGC METER CIRCUITRY

METER USED AS ALC METER IN TRANSMIT

METER USED AS S METER IN RECEIVE
Circuit Description of the Transmit IF Amplifier (Fig 104, 105)

144. The transmit IF amplifier controls and amplifies the SSB signal from the crystal filter following the balanced modulator. This is done in order to provide a constant input, at the desired level, for use in the transitor subassembly. The transmit IF amplifier consists of two stages, one of which is controlled by the peak power control (PPC) circuitry and the other is controlled by the average power control (APC) circuitry. In the compatible AM mode of transmission, the local 1.75 Mc carrier is reinserted in the second stage of the amplifier.

145. The 1.75 Mc IF output from SSB crystal filter is applied to connector J4A3. (Fig 104). From connector J4A3, the 1.75 Mc IF signal is coupled by capacitor A1C3 to a variable voltage divider consisting of resistor A1R3 and the collector-to-emitter and base-to-emitter resistances of PPC attenuator A1Q1. The voltage divider is controlled by the DC output voltage from the PPC circuit. This DC voltage is applied across the temperature compensated voltage divider consisting of resistors AR1 and A1R2, thermistor A1R3, and diode A1C4. Capacitor A1C2 places an AC short between collector and base, causing both the collector-to-emitter resistance and the base-to-emitter resistance to form a part of the total shunt resistance for controlling the level of the IF signal input to transmit IF amplifier A1Q3. Diode A1C6 provides temperature compensation for PPC attenuator A1Q1. The output from the voltage divider is coupled by capacitor A1G6 to the base of transmit IF amplifier A1Q3.

146. The gain of transmit IF amplifier A1Q3 is controlled by PPC degenerator A1Q2. PPC degenerator A1Q2 acts as a variable impedance element in series with emitter bypass capacitor A1G7. The base voltage for PPC degenerator A1Q2 is developed from the 20 volt DC supply line by voltage divider A1R6, A1K7, A1R8. A decrease in the transmitted IF signal level decreases the PPC voltage level, causing PPC attenuator A1Q1 to conduct less, increasing the shunt resistance (less attenuation). This will bias PPC degenerator A1Q2 into saturation, effectively grounding emitter bypass capacitor A1G7. Therefore, the output from transmit IF amplifier A1G3 is maximum. As the PPC voltage increases, the conduction of PPC attenuator A1Q1 will increase. The amount of conduction will be controlled by the IF output signal level. The shunt resistance will decrease as the rate of conduction increases, decreasing the amount of signal applied to the base of transmit IF amplifier A1Q2. As the rate of conduction increases, the amount of signal applied to the base of transmit IF amplifier A1Q3. As the rate of conduction of PPC attenuator A1Q1 increases, the DC voltage present at the collector will decrease. Therefore, the base voltage on PPC degenerator A1Q2 will decrease, reducing its conduction. This will increase the impedance in series with emitter bypass capacitor A1G7, providing increased degeneration and reduction in gain of transmit IF amplifier A1Q3.

147. PPC attenuator A1Q1 and PPC degenerator A1Q2 together provide greater than 40 db of control to maintain the peak output from transmit IF amplifier A1G3 at a level determined by the peak power control circuitry. The output from transmit IF amplifier A1G3 is coupled to another voltage divider consisting of resistor A1R20 and the collector-to-emitter and collector-to-base resistance of APC attenuator A1Q4 by capacitor A1G5. The amount of control provided by the variable voltage divider depends on the DC output from the APC circuit. Therefore, the output from the voltage divider depends on the DC output from A1Q4 to the base of transmit IF amplifier A1Q6. The gain of transmit IF amplifier A1Q6 is determined by the amount of degeneration developed by the collector-to-emitter resistance of APC degenerator A1Q5. The theory of operation for transmission stages A1Q1, A1Q5, and A1Q6 is identical to that for the corresponding stages A1Q4, A1Q2, and A1Q3. The output from transmit IF amplifier A1Q6 is coupled by transformer A1G2 to connector J4A1 for application to the transitor subassembly.

148. In SSB, CW, PSK, or NAK modes of transmission, pins 9 and 10 of connector J1 will be open. Therefore, the 20 volts DC supply voltage present at pin 1 of connector J1 will be applied through resistor A1R9 to the cathodes of diodes A1CR6 and A1CR7. Since their anodes are at 10 volts DC (developed from the 20 volts DC by voltage divider A1R18, A1R15 and applied through isolating resistors A1R22 and A1R17), they will be reverse biased. These diodes, in the back-biased mode, ensure that any 1.75-Mc leakage will be at least 50 db down from the 1.75-Mc IF signal. During compatible AM operation, the 1.75-Mc local carrier is gated back into the IF signal. The 1.75-Mc output from the frequency divider subassembly is applied to connector J4A2, from which it is applied to AM CARRIER ADV A1A14. AM CARRIER ADV A1A14 is used to set the injection level. During compatible AM transmission, ground is applied to pin 9 of connector J1, from which it is applied through diode A1Q2 to the cathodes of diodes A1CR6 and A1CR7. Since the anodes of A1CR6 and A1CR7 are at 10 volts DC, they will be forward biased, allowing the 1.75-Mc local carrier to pass and be coupled by capacitors A1C12 and A1C16 into the main signal path at the junction of resistors A1R21 and A1R20. When the radio set is in tune condition, a ground from the AM-33Mc/9QRC-106 is applied at pin 10 of connector J1. Diodes A1CR2 and A1CR3 are isolating diodes. A1CR3 isolates the
ground on pin 10 from the AM ground line on pin 9. A1CR2 isolates the ground on pin 9 from the tune ground line on pin 10. These grounds are never applied simultaneously.

149. The tune ground applied through diode A1CR3 has the same effect as the AM ground applied through diode A1CR2. In this case, however, there is no IF input at J1A3, since only a carrier is needed for tuning purposes.

Circuit Description of the Audio Amplifier and the Audio AGC System (Fig 10.5)

150. The primary purpose of the audio section of the Transmitter IF and Audio Subassembly is to amplify the applied audio information to a power output as required. The power output of this circuit is varied by varying the collector-to-emitter resistance of the AGC audio amplifier A2Q1. This resistance is varied by the AGC loop, which changes the DC voltage at the base of the AGC amplifier A2Q1 as the signal level changes. The output from the voltage divider is coupled by capacitor A2Q7 to the base of the AGC amplifier A2Q2. Resistor A2R7 isolates the voltage divider from the input impedance of the AGC amplifier A2Q2 in order that maximum control range can be obtained from the AGC amplifier A2Q1.

151. The audio intelligence is applied to either pin 17 or pin 16 of connector J1. Pin 17 is the input for carbon microphones and pin 16 is the input for dynamic microphones. Capacitor A2C1 is used to block the microphone bias from being applied to the AGC amplifier A2Q1. Resistors A2R2 and A2R4 provide a voltage divider to reduce the higher transmit audio signal to a lower level. Resistors A2R5 provides the 50-ohm termination for the carbon microphone. Resistor A2R6 provides the 600-ohm termination for the dynamic microphones. Resistor A2R6 and transistor audio attenuator A2Q1 form a variable voltage divider to maintain the level of audio at the base of the AGC amplifier A2Q2 at a nearly constant level. The attenuation effect of the voltage divider is varied by varying the collector-to-emitter resistance of the AGC audio attenuator A2Q1. This resistance is varied by the AGC loop, which changes the DC voltage at the base of the AGC amplifier A2Q1 as the signal level changes. The output from the voltage divider is coupled by capacitor A2Q7 to the base of the AGC amplifier A2Q2. Resistor A2R7 isolates the voltage divider from the input impedance of the AGC amplifier A2Q2 in order that maximum control range can be obtained from the AGC amplifier A2Q1.

152. Audio amplifier A2Q2 raises the level of the audio signal and develops it across resistor A2R25. Resistor A2R25 is used to provide collector-to-base feedback to improve the stability and minimize the distortion of audio amplifier A2Q2, and is also part of the biasing circuit. The output from amplifier A2Q2 is direct coupled to the base of audio amplifier A2Q3. Amplifier A2Q3 raises the level of the audio intelligence and develops it across resistor A2R26 and emitter resistor A2Q4. Resistor A2R26 provides emitter bias and A2Q4 is the emitter resistor bypass capacitor. Resistor A2R30 provides collector-to-base feedback to improve the stability and minimize the distortion of amplifier A2Q2. The output from voltage divider A2R31, A2R32 is coupled by capacitor A2C8 to pin 19 of connector J1 for application to the balanced modulator. The output from the collector of amplifier A2Q3 is direct coupled to the base of audio amplifier A2Q4.

153. Audio amplifiers A2Q4, A2Q5 provide a point for sampling the audio signal to develop the AGC and also provides isolation between the AGC loop (A1CR2 through A2C1, A2Q6, A2Q1) and the audio amplifiers (A2Q2, A2Q3) to prevent distortion from the full wave rectifier circuit from feeding back into amplifier A2Q3. The amplified output from the collectors of amplifiers A2Q4 and A2Q5 is developed across the primary of transformer A2T1. The output from amplifier A2Q4, which is developed across the unby-passed portion of the emitter load (resistor A2R28), is coupled by capacitors A2C3 and A2C6 to the base of AF amplifier A2Q6. Transformer A2T1 couples the output from amplifiers A2Q4 and A2Q5 to a full-wave rectifier circuit consisting of diodes A2CR2 through A2CR5. The resulting DC voltage is filtered by capacitor A2C7 and applied to the base of AGC DC amplifier A2Q6. Resistors A2R21 and A2R20 and transformer A2R54 form a temperature-compensated load for transformer A2T1 to maintain the input to the full-wave rectifier at a nearly constant level regardless of variations in temperature. AGC DC amplifier A2Q6 raises the current level of the DC signal. The output from AGC DC amplifier A2Q6 is filtered by capacitor A2C4 and is applied to the base of transistor audio attenuator A2Q1. As the audio input level at the AUDIO connectors increases, the collector-to-emitter resistance of the transistor audio attenuator A2Q6 increases. Therefore, the variable shunt resistance maintains the audio output from audio amplifier A2Q3 at a nearly constant level, regardless of the fluctuations in output level at the AUDIO connectors.

154. During CW operation, 20 volts DC is applied to pin 13 of connector J1. This voltage is applied to the center tap on the secondary of transformer A2T1, heavily forward biasing diodes A2CR2 and A2CR3, thus biasing AGC DC amplifier A2Q6 into saturation. This is turned off when the audio input level at the AUDIO connectors increases, the collector-to-emitter resistance of the transistor audio attenuator A2Q6 increases. Therefore, the variable voltage divider will provide maximum attenuation to any inputs from the microphones, thereby minimizing leakage into audio amplifiers A2Q2 and A2Q3. Figure 15 provides a simplified block diagram of the audio section of the Transmitter IF and Audio Subassembly.
**Fig 19 - Block Diagram of Audio Section of the Transmitter IF and Audio Assembly**

**Keying Circuito Including Vox Operation (fig 1015)**

155. The primary keying of the Receiver-Transmitter and the Power Amplifier is accomplished in this subassembly. In Vox operation the transmitter keying is initiated by voice signals into the microphone. Some of the audio from the speech amplifier is amplified and rectified, and the resultant DC signal is used to activate the required relays to key the transmitter. Thus the transmitter is on at any and all times that the operator is speaking but is off during the intervals between sentences. The voice-controlled circuit must have a small amount of "hold" built into it so that it will hold in between words, but it should turn on rapidly at the slightest voice signal coming through the speech amplifier. When the radio set is being operated in the SSB or AM modes of operation, it can be keyed by three possible methods: PUSH TO VOX, PUSH TO TALK, or VOX, as determined by the VOX switch on the RT-662/GRC front panel. During the CW or FSK modes of operation, the keying is accomplished using the key, KX-116/U and radioteletypewriter terminal equipment, respectively. During both CW and FSK operation, the VOX switch is disabled.

156. The emitter output from audio amplifier A2Q5 is raised in level by AF amplifier A2Q8 and developed across collector load resistor A2R38. Collector-to-base feedback is produced and base bias supplied by resistor A2R33 to improve the stability and minimize the distortion of audio amplifier A2Q8. The output from amplifier A2Q8 is coupled by capacitor A2R23 to the base of VOX detector A2Q9. The level of the applied signal is set by resistor A2R1, which determines the VOX threshold (minimum voice level which will initiate the VOX keying function). Capacitor A2Q24 is a bypass for frequencies above the range of maximum voice energy (approximately 400-600 c/s). In VOX operation, a ground is applied through the SERVICE SELECTOR and VOX switches on the RT-662/GRC front panel to pin 27 of connector J4. This ground is applied to the emitter of VOX detector A2Q9, removing the back bias developed by resistors A2R13 and A2R14. Therefore, the voice input signals above the VOX threshold bias VOX detector A2Q9 on, causing it to go into saturation. This provides a low impedance discharge path for capacitor A2Q25 (through the small collector-to-emitter resistance of VOX detector A2Q9) to initiate the VOX keying function. Initially, and whenever voice is not being transmitted, the 27 volt dc which is regulated to 20 volts dc by zener diode A2VR3, will forward bias VOX switch A2Q10. Therefore, capacitor A2Q25 charges, the emitter voltage of VOX switch A2Q10 will increase until it is of sufficient level to cause 12 volt zener diode A2VR4 to conduct. At this time, slightly less than 13 volts dc is present on both the emitter and base, preventing VOX switch A2Q10 from conducting. When
12-volt zener diode A2V24 is conducting, transmit-receive switch A2Q11 will be forward biased, causing the collector voltage to drop and prevent 12-volt zener diode A2VR5 from conducting. Therefore, transmit-receive switch Q1 will be off. This prevents the collector of relays 1A1K1, 1A1K3, 1A1K4, and 1A1K5 from having a path to ground; therefore, the relays will remain de-energized. When the voice level applied to VOX detector A2Q9, exceeds the VOX threshold, VOX detector A2Q9 conducts. This allows capacitor A2Q25 to discharge through the small collector-to-emitter resistance of A2Q9, forward biasing VOX switch A2Q10. (The emitter has been at approximately 15 volts.) As A2Q10 conducts, the emitter voltage will drop and prevent zener diode A2VR5 from conducting. This will cut off transmit-receive switch A2Q11, causing the collector voltage to rise toward 20 volts DC and cause 12-volt zener diode A2VR5 to conduct. This forward biases transmit-receive switch Q1, effectively placing the collector-to-emitter resistance at ground due to its lower resistance. This ground is applied through diode A2GR18 to pin 31 of connector J1, from which it is applied to relays 1A1K1, 1A1K3, 1A1K4, and 1A1K5 to energize them and place the RF-662/GRC in transmit condition. This ground is also applied to pin 32 of connector J1 for application to the AN-3343/GRC-106 to initiate the keying functions. Zener diode A2VR2 prevents transients, produced by de-energizing relays 1A1K1, 1A1K3, 1A1K4, and 1A1K5, from being applied to the collector of transmit-receive switch Q1. The radio set will remain keyed for 500 milliseconds after the completion of the down-sweep. This hang time is provided to prevent pauses in normal speech from repeatedly keying and unkeying the radio set. The hang time is the time required for capacitor A2Q25 to recharge through VOX switch A2Q10 to the point where VOX switch A2Q10 cuts off. Fig 20 is a block diagram of the VOX circuitry.

157. PUSH TO VOX: The sequence of operation for PUSH to VOX operation is the same as that for VOX operation, with the following exception. Pin 27 of connector J1 is at ground only when the push-to-talk switch on the Handset H-33/PT or Microphone M-29/U is depressed, rather than the permanent ground applied during VOX operation. Voltage divider A2R3/A2M1 reverse biases switch A2Q9, preventing the voice from keying the radio set until the push-to-talk switch is depressed. When the push-to-talk switch is released, there is no hang time.

158. PUSH TO TALK: When operating in push to talk, a ground is applied to pin 29 of connector J1 each time the push-to-talk switch on the Handset H-33/PT or Microphone M-29/U is depressed. This ground is applied to the base of relays 1A1K1, 1A1K3, 1A1K4, and 1A1K5 of the VOX circuit of the radio set. When the push-to-talk switch is released, there is no hang time.

159. CW and FSK: When operating in the CW or FSK modes of operation, the front panel of the VOX switch is disabled. The SERVICE SELECTOR switch applies a ground to pin 22 of connector J1. This ground is applied through diode A2QR7 to the base of A2Q8 and through diode A2GR8 to the collector, thus cutting off any audio from capacitor A2Q9. In CW operation, the key KV-116/U places a ground at pin 30 of connector J1 each time the key is depressed. This ground is applied to the base of VOX switch A2Q10 through diode A2GR11. Therefore, capacitor A2Q25 will discharge through the small forward resistance of diode A2GR11 to turn on VOX switch A2Q10. The radio set is then keyed as previously explained. At the termination of the message, the radio set will remain keyed for approximately 500 milliseconds. This hang time is provided to prevent the radio set from going into receive operation during a normal message pause. In FSK operation, ground is applied to pin 29 of connector J1 by the radioteletypewriter terminal equipment. The keying then accomplished in the same way as for push-to-talk operation.

2 KC Generator (fig 1015)

160. In the AN/GRC-106 system, the transmitted CW signal is always 2 kc higher in frequency than the indicated frequency on the frequency setting control of the RF-662/GRC. This 2 kc signal is used to key a part of the circuitry of the 2 kc generator in the Transmitter and Audio Subassembly. This 2 kc signal is then applied to the balanced modulator where an upper side band of 1.752 kc is created. This frequency is then converted as usual to any RF frequency between 2 and 30 mc.

161. In the receive node the incoming signal will be translated down in frequency to an IF frequency of 1.752 Mc. In the product detector an injected carrier of 1.752 Mc is used. Since this injected carrier can be varied by the operator over a small range, the tone of the received CW signal can be varied to suit the individual operator. The 2 kc signal is derived from a frequency spectrum available in the Frequency Divider Subassembly. (fig 1017)
FIG 20 - BLOCK DIAGRAM OF VOX CIRCUITRY
162. The 1-kc spectrum output from frequency divider module 1A6 is applied to connector J1A1. In the absence of ground at pin 30 of connector J1, the 20 volts d causes 3.3-volt zener diode A2Q11 to conduct, forward biasing 1-kc pulse switch A2Q12. Since 1-kc pulse switch A2Q12 is conducting, except when the key KY-166/U is depressed (ground on pin 30 of connector J1), the 1-kc pulse input will be attenuated by the small collector-to-emitter resistance of 1-kc pulse switch A2Q12. When the key KY-116/U is depressed, ground is applied to pin 30 of connector J1. This ground is applied to the cathode of diode A2CH20, causing it to conduct and reduce the 20 volts d supply voltage below the firing point of 3.3-volt zener diode A2V31. Therefore, when the key KY-116/U is depressed, 1-kc pulse switch A2Q12 becomes non-conducting and the 1-kc pulse input will be allowed to pass to the triple section filter.

163. The triple section filter is tuned to pass only the second harmonic of the 1-kc pulse input. This 2-kc signal is applied to the base of CW 2-kc switch A2Q7. During CW operation, the SERVICE SELECTOR switch applies a ground to pin 14 of connector J1. This ground is applied to the cathode of diode A2CH6, completing the emitter circuit for CW 2-kc switch A2Q7 which raises the level of the 2-kc signal and develops the resulting output across collector load resistor A2R27. Resistor A2R8 is used to provide collector-to-base feedback to improve the stability and minimize the distortion of CW 2-kc switch A2Q7 as well as being the base bias resistor. A small amount of degeneration is provided by the unbypassed, small forward, resistance of diode A2CH6 to improve the stability of CW 2-kc switch A2Q7. The output from CW 2-kc switch A2Q7 is coupled by capacitor A2C7 to the base of AF amplifier A2Q6. Capacitor A2C1 and resistors A2R15 and A2R16 form an equalizing network to keep the 2-kc tone at the same level as the voice input. The 2-kc tone enters the regular audio channel at the base coupling capacitor A2C7.

Internal Automatic Level Control Circuitry (Fig 1013)

164. The Internal ALC subassembly is located in the chassis. Its function is to provide control signals to the PFC and APC circuits in the Transmitter IF subassembly whenever the Power Amplifier AM-3343/EGC-106 is not being used. The internal ALC produces a DC output corresponding to the peak voltage output from the AM-3343/EGC. The normal automatic level control (ALC) signals from the AM-3343/EGC-106 override the signals from this subassembly when normal system operation is used.

155. The output from the RF Amplifier (in the transmit mode) is applied to capacitor C1. Diode CR1 detects the positive envelope of the excitation signal. Inductance L1 and capacitors C2 and C4 filter the output from CR1. This DC signal is coupled to emitter follower Q1. Q1 presents a high impedance across the detector and filter to prevent loading of this circuit, its low impedance output is further filtered by inductances L3 and capacitors C5 and C7. The DC control signal is applied to diodes A3CH4 and A3CH5 in the Transmitter IF and Audio subassembly. When no signals from the ALC in the Power Amplifier AM-3343/EGC-106 are present, these diodes will not be back biased. Therefore, the internal ALC control signals will be applied to the normal PFC and APC circuits.

THE FREQUENCY DIVIDER AND SPECTRUM GENERATOR 1A6 (Pages 1015 and 1017)

General

166. The frequency divider and spectrum generator subassembly contains the frequency dividers and spectrum generators required to produce reference frequencies which are used within the frequency synthesizers.

Circuit Description for the Divider and Spectrum Generator Subassembly

157. This subassembly produces several frequency spectrums required by the synthesizer subassemblies. It also produces the 1.75 kc IF signal used by several other subassemblies.

100-kc Divider and Spectrum Generator

168. The function of the 100-kc divider and spectrum generator is to provide the spectrum of frequencies required in the 100-kc synthesizer subassembly. This circuit also triggers the 10-kc divider circuit. (fig 1016) The input to the 100-kc divider circuit is the 500-kc output from frequency standard module 1A3. This sinusoidal signal is applied to emitter follower A1F1, where it is stepped up and coupled by capacitor A1CH1 to the base of pulse shaper A1Q1. The negative portions of the 500-kc signal are of sufficient magnitude to drive pulse shaper A1Q1 into saturation. This results in the collector of pulse shaper A1Q1 being effectively switched between zero and the supply voltage level. Diode A1G1 provides temperature compensation for pulse shaper A1Q1 and aids in the shaping of the output pulses.
FIG 21 - BLOCK DIAGRAM OF FREQUENCY DIVIDER AND SPECTRUM GENERATOR
The positive pulsed output from pulse shaper A1Q1 is differentiated by capacitor A0C5 and the input impedance of astable multivibrator A1Q2, A1Q3.

169. Multivibrator A1Q2, A1Q3 is an astable (free running) multivibrator until synchronized by the 500-kc trigger pulses. Assume that a positive trigger pulse is applied to the base of transistor A1Q2 and that both transistors A1Q2 and A1Q3 are cut off. The collector of transistor A1Q2 and the base of transistor A1Q3 are at the supply voltage level (7.5 volts dc) at this time. The input pulse will forward bias transistor A1Q2, causing it to conduct. The resulting collector current develops a voltage drop across resistor A1R6, decreasing the base bias of transistor A1Q3. Since the emitter of transistor A1Q3 is at the supply voltage level, transistor A1Q3 will be forward biased and conduct. This causes the collector of transistor A1Q3 to go from zero to approximately 6.5 volts dc. (The 1-volt voltage drop will be caused by the small forward resistance of diode A1C5 and the emitter-to-collector resistance of transistor A1Q3.) The base bias voltage divider for transistor A1Q2 (resistors A1R5, A1R6, A1R7) will now have 6.5 volts dc (transistor A1Q3 collector voltage) on one end and the 7.5-volts dc supply on the other end. This causes transistor A1Q2 to go to and be held at saturation. Capacitor A1C7 now charges through two paths. One path is through resistor A1R1, transistor A1Q2, and resistor A1R6. The other path is through resistor A1R8, transistor A1Q3, and diode A1C3. As the charge on capacitor A1C7 increases, the emitter bias on transistor A1Q2 increases, decreasing the base bias. This reduces the collector current of transistor A1Q2, causing the collector to go positive. Therefore, the base bias on transistor A1Q2 will go positive, decreasing the forward bias. This decreases the collector current of transistor A1Q3, decreasing the amount of bias applied to the base of transistor A1Q3 by base bias voltage divider A1R5, A1R6, A1R7. This further reduces the forward bias of transistor A1Q2. The resulting regeneration brings transistors A1Q2 and A1Q3 out of saturation and continues until they are both cut off. Capacitor A1C7 now starts to discharge through resistors A1R10, A1R9, and A1R8. During the start of the discharge period, the trigger pulses are still applied to the base of transistor A1Q2, and are not or of sufficient magnitude to turn it on. When transistors A1Q2 and A1Q3 are cut off, the base bias on transistor A1Q2 is determined by voltage divider A1R5, A1R6, A1R7, A1R9, A1R10. The emitter voltage is the charge on capacitor A1C7. Therefore, capacitor A1C7 has to discharge to such a value that when a positive trigger pulse is applied to the base of transistor A1Q2, it starts to conduct. The time constant of the RC network consisting of capacitor A1C7 and resistors A1R9, A1R9, A1R10 is fixed. The resistor A1R9 can be adjusted to set the bias on the base of transistor A1Q2 to allow every fifth pulse, after the initial trigger pulse, to turn transistor A1Q2 on. When this occurs, the collector voltage on transistor A1Q2 will again decrease, and the regeneration process will be repeated. Thus, the process of regeneration occurs before the natural period has been completed as a result of the application of every fifth trigger to the base of transistor A1Q2. This results in an output (at the collector of transistor A1Q3) that is exactly one-fifth of the input trigger pulse rate. The resulting 100-kc signal present at the collector of transistor A1Q3 is applied to the 10-kc divider circuit. Capacitor A1C10 prevents any degeneration from occurring in the circuit as a result of the small forward resistance or diode A1C3. Capacitor A1C10 cuts off the application of the pulse to the collector of transistor A1Q3 to base of transistor A1Q2. The 100-kc pulsed output from transistor A1Q3 is developed across voltage divider A1R9, A1R10, and is coupled by capacitor A1C11 to the base of pulse amplifier A1Q4. Pulse amplifier A1Q4 and key oscillator A1Q5 form a keyed oscillator circuit that will produce a sinusoidal burst of frequencies. When the key is turned on, the oscillator circuit will produce a sinusoidal burst of frequencies. This results in a spectrum of frequencies between 15.3 and 16.2 Mc centered around the free running frequency of oscillator A1Q5. This frequency spectrum is coupled by transformer A1T2 to connector J1A-A4 for application to 100-kc synthesizer module 1A2.

170. The function of the 10- and 1-kg divider and spectrum generator is to produce one of the spectra required in the 10- and 1-kg Synthesizer subassembly. This circuit also produces the trigger pulses for the 1-kg divider, the 1.75 Mc generator and the vernier frequency function.
The input to the 10-kc divider circuit is the 100-kc triggering pulse from the 100-kc divider circuit. This pulsed signal is differentiated by capacitor A202 and the input impedance of bistable multivibrator A2Q2, A2Q2. Bistable multivibrator A2Q4, A2Q4 produces one output pulse for every two input pulses. The positive pulses are directed to the saturated transistor of multivibrator A2Q4, A2Q2 by steering diodes A2CR1 and A2CR2. This turns off the saturated transistor and starts the required regenerative process. Resistor A2R2 references the anodes of steering diodes A2CR1 and A2CR2 at the same potential as the emitters of transistors A2Q1 and A2Q2 and provides the return path for capacitor A2Q2. The resulting 50-kc pulsed output is developed across voltage divider A2R6, A2R9 and is coupled by capacitor A2Q11 to the 1.75-Mc generator. The 50-kc pulsed output from bistable multivibrator A2Q4, A2Q2 is also developed across resistor A2R10 and is applied to bistable multivibrator A2Q3, A2Q4.

171. The 50-kc pulsed signal is differentiated by capacitor A2C5 and the input impedance of bistable multivibrator A2Q3, A2Q4. Bistable multivibrator A2Q3, A2Q4 functions the same as bistable multivibrator A2Q4, A2Q2 previously described, to produce a 10-kc pulsed output across voltage divider A2R16, A2R17. This 10-kc pulsed output is applied to the 1-kc divider circuit and is coupled by capacitor A2D20 to the base of pulse amplifier A2Q7.

172. When the FREQ. VERNIER control is at OFF, pulse amplifier A2Q7 (Fig. 1017) and keyed oscillator A2Q8 function as a keyed oscillator in the same manner as pulse amplifier A1Q4 and keyed oscillator A2Q3, previously described. This circuit produces a spectrum of frequencies between 2.48 and 2.57 Mc, which are separated by the 10-kc keying rate. The output from the keyed oscillator is coupled by transformer A2R3 to connector J1B-A1 for application to 10- and 1-kc synthesizer module IAl.

173. When the FREQ. VERNIER control is in an ON position, keyed oscillator A2Q8 functions as an amplifier. The feedback path for keyed oscillator A2Q8 is through transformer A2Q3, capacitor A2C25, diode A2CR8, and capacitor A2C27. When the FREQ. VERNIER control is placed in an ON position, 20 volts dc is applied through pin 1 of connector J1A via decoupling components A2L13, A2R10, and resistor A2R37 to the anode of diode switch A2CR9. This will forward bias diode A2CR9, applying approximately 15 volts dc to the cathode of diode A2CR8. The forward bias of diode A2CR9 is only 9 volts dc (as determined by voltage divider A2K1, A2R44, A2R43), since A2C28 will be reverse biased. This will then block the feedback path of keyed oscillator (amplifier) A2Q8, preventing it from functioning as an oscillator. The output from oscillator A2Q9 will then be gated to the keyed oscillator (amplifier) A2Q6 by pulse amplifier A2Q7 at the 10-kc keying rate. The resonant circuit for oscillator A2Q9 consists of 2.53-Mc crystal A2T2, inductor A2L2, and voltage variable capacitor (VVC) A2CR10. The center point of VVC A2CR10 is set by the dc voltage level established by the temperature compensated voltage divider A2R47, A2R50, A2R8, A2R43, A2R49, and the FREQ. VERNIER control on the RT-662/GRU front panel. Resistor A2R49 provides adjustment to compensate for differences in the voltage variable capacitors used. The wiper of the FREQ. VERNIER control is connected to pin 2 of connector J1A and the control is connected to pin 4 of connector J1A. The other end of the FREQ. VERNIER control goes to A2R13, which is a 20-volts dc compensating network to 20 volts dc. This allows the voltage at pin 2 of connector J1A to be varied above and below the reference point established by the 20 volts dc on pin 1 of connector J1A. Therefore, the resonance of the tank circuit may be varied plus or minus 500 c/s by changing the center point of a VVC. This same varible voltage is applied from the wiper to one end of the FREQ. VERNIER control to make it non-linear. Capacitor A2R13 is chosen to establish non-linearity in the FREQ. VERNIER. Therefore, the non-linear voltage across resistors A2R19 and A2R13 and the FREQ. VERNIER control will compensate for the non-linearity of VVC A2CR10. Resistor A2R12 is an isolating resistor. Base bias for oscillator A2Q9 is established by voltage divider A2R39, A2R41. Capacitors A2C28 and A2C30 form the reactive voltage divider for the feedback required to sustain oscillations in oscillator A2Q9. Capacitor A2C30 is a temperature compensating capacitor. Resistor A2R28 is the emitter current limiting resistor. The 2.53-Mc plus or minus 600 c/s output from oscillator A2Q9 is coupled by capacitor A2C22 to the anode of diode A2CR9. Since diode A2CR9 is forward biased in the vernier condition, the output from oscillator A2Q9 is coupled by capacitor A2C27 to the base of keying oscillator (amplifier) A2Q8. Pulse amplifier A2Q7 will gate this signal through keying oscillator (amplifier) A2Q8 at the 10-kc keying rate. This will produce the desired 2.48- to 2.57-Mc spectrum. The spectrum points which are separated exactly by the 10-kc keying rate are variable plus or minus 600 c/s, depending on the setting of the FREQ. VERNIER control. The collector of pulse amplifier A2Q7 is switched between 0 and 20 volts dc by the synchronizing signal. This switching signal in applied to the anodes of diodes A2CR5 and A2CR6. Diode A2CR7 always has 20 volts dc applied to its anode. The potential difference between anode and cathode of this reference diode (A2CR7) is approximately 1 volt dc. When the switching voltage is at zero volts, diodes A2CR5 and A2CR6 will be forward biased and diode A2CR7 will be reverse biased. When the switching voltage is at 20 volts dc, diodes A2CR5 and A2CR6 will be forward biased and diode A2CR7 will be reverse biased.
Diodes A2CR5 and A2CR6 (when forward biased) effectively place an ac short across the tank circuit while diode A2CR7 removes the ground at the tap of transformer A2T3. Therefore, diode A2CR7, in conjunction with diodes A2CR5 and A2CR6, prevent ringing in the tank circuit as a result of the effective switching of the ac short.

**The 1-kc Divider Circuit (Fig 1017)**

174. The function of the 1-kc divider circuit is to produce the 1-kc pulse to be used in the 10- and 1-kc Synthesizer subassembly. The circuit also produces the 1-kc pulse required in the Transmitter IF and Audio subassembly for CW keying. The input to the 1-kc divider circuit is the 10-kc triggering pulse from the 10-kc divider circuit. The pulse signal is differentiated by capacitor A3Q2 and the input impedance of bistable multivibrator A3Q1, A3Q2. Bistable multivibrator A3Q1, A3Q2 functions exactly like bistable multivibrator A2Q1, as previously described, to divide the 10-kc pulse input by two. The 5-kc pulsed output from bistable A3Q1, A3Q2 is fed to bistable section A4Q1, A4Q2. Bistable multivibrator A4Q1, A4Q2 functions exactly like bistable multivibrator A1Q2, A1Q3, previously described, by dividing the 5-kc pulsed signal by five. The resulting 1-kc pulsed output contains the required 21 to 35-ke harmonics that are used in the 10- and 1-kc synthesizer module 1A4. This is applied to 10- and 1-kc synthesizer module 1A4 through connector J14-A1. The 1-kc pulse output is also applied through resistor A1R18 to connector J14-A2 to the 2-kc generator for CW operation.

**The 1.75-Mo Generator (Fig 1016)**

175. The function of the 1.75-Mc generator is to produce the 1.75-Mc local carrier for use in the Transmitter IF and Audio subassembly and the Receiver IF subassembly.

176. The input to the 1.75-Mc generator is the 50-kc pulsed output from the 10-kc divider circuit. This signal is applied to a keyed oscillator circuit consisting of pulse amplifier A2Q5 and keyed oscillator A2Q6. This keyed oscillator circuit functions exactly like the key oscillator circuit in the 100-kc divider circuit (A1Q4 and A1Q5) to produce a spectrum of frequencies centered around 1.75 Mc, which are separated by the 50-kc keying rate. The keying pulse synchronizes the 1.75-Mc free running frequency of oscillator A2Q6, ensuring that the exact 1.75-Mc output is always present in the spectrum. The spectrum output from the keyed oscillator circuit is filtered by crystal A2Y1, allowing only the 1.75-Mc spectrum point to be developed across the tank circuit consisting of capacitor A2C19 and the primary of transformer A2T2. Capacitor A2C16 provides a means of adjusting the series impedance to the applied spectrum and, thereby, the amplitude of the spectrum. The circuit consisting of crystal A2Y1, capacitors A2C15 and A2C19, and transformer A2T2 forms a filter which is rather narrow. Capacitor A2C18 is adjusted so that the impedance of capacitor A2C18 and the bottom half of the primary of transformer A2T2 equals the impedance of the higher capacitance of crystal A2Y1 and the upper half of the primary of transformer A2T2. Therefore, the 50-kc pulsed signal, which is developed across the two halves of the primary of transformer A2T2, will be of the same amplitude, but 180 degrees out of phase with each other. This prevents any signal except the desired one from appearing in the 1.75-Mc output.

**THE TRANSLATOR-SYNTHESIZER PROCESS**

**General**

177. The purpose of the synthesizers is to produce digitally selected frequencies corresponding to the desired channel injections. These are the injection frequencies into the RF translator circuits which were explained previously. These frequencies from the synthesizers must be free from spurious signals, and must reflect the accuracy and stability of the master frequency standard. Because the frequency scheme lends itself to digital frequency selection, the synthesizer outputs for the megacycle, 100 kc, 10 kc, and 1 kc injection frequencies can be considered separately. Submodular arrangement permits the shielding of frequencies in the synthesizer process that must be isolated from the other portions of the receiver-transmitter.

178. Fig 22 is an overall block diagram of the translator-synthesizer arrangement. The translator portion is at the top of the diagram. It should be noted that the injection frequencies are the same in transmit as in the receive mode and that the only difference is in the order in which the conversions are made are in the translator itself. The arrows in this portion of the block diagram show the receive signal path. Reversal of the arrows will indicate the transmit signal path.
FIG. 22 - BLOCK DIAGRAM OF
2 - BLOCK DIAGRAM OF SYNTHESIZER
The MC Synthesizer 1A9

179. The purpose of the MC Synthesizer is to furnish injection frequencies to the translator subassembly in order to perform the conversion for the megacycle digits of the selected RF frequency. Fig 23 is a block diagram of the MC synthesizer.

![Block Diagram of MC Synthesizer]

**Fig 23 - Block Diagram of MC Synthesizer**
Error Correction in the NC Synthesizer

180. The crystals used in the NC Synthesizer Subassembly are off the shelf items and their errors are always on the low side in frequency. A phase lock circuit is used to pull the crystals into agreement with the frequency standard.

181. The purpose of the NC synthesizer electronic subassembly is to furnish the proper frequencies to the RF translator in order to perform the first of three conversions in translating the incoming RF signals to the 1.75 Mc signal. (In the transmit mode this conversion becomes the third, since the order is reversed and the 1.75 Mc IF signal is converted to any one of 28,000 RF frequencies).

182. Seventeen loose tolerance crystals are used and are switched into the oscillator circuit according to the setting of the frequency control unit. Since some crystals are used two or three times to produce the proper frequencies, only seventeen are required to cover the 28 megacycle digits. Since this synthesizer contributes directly to the tuning of the receiver-transmitter, a high degree of frequency stability is required. The error of the crystals is always on the low frequency side, so that a phase lock arrangement can pull the crystal frequencies into agreement with the frequency standard. The crystal selection switch is driven by the same motor gear system used for the RF Amplifier turret.

183. A locked crystal oscillator is used for these injections. This method removes many of the major disadvantages of a closed loop system. It permits digital switching without a "hunting" oscillator capable of false locking. Since the oscillator is crystal controlled, the maximum error of the oscillator, under unlocked conditions, is crystal tolerance. This ensures that, in case of catastrophic failure of the phase locking circuit, the received or transmitted signals will be within the allocated channel, although not at the precise frequency desired, and communications can still be maintained.

184. The control loop functions as follows. For explanation, assume that the 16.5 Mc crystal is locked to the standard frequency. A 1 Mc signal obtained by frequency division in the frequency standard subassembly is converted to a damped exponential pulse which drives a relatively flat spectrum between 1 and 25 Mc. This spectrum is applied to a mixer, where it is mixed with the 16.5 Mc crystal oscillator signal. The crystal error is approximately 0.01 percent lower than the desired locked frequency.

185. Assuming that the free running oscillator is at 16.498 Mc or 2 kc low, the oscillator mixes with the 15,000 and 18,000 Mc spectrum points and produces two intermediate frequencies of 498 and 1502 kc. These signals are amplified in the 1500 kc IF amplifier and envelope detected. The detected DC voltage varying at a 1 kc rate (the difference between the two IF frequencies of 498 and 1502 kc) is applied to a variable capacity diode with its polarity such that it moves the frequency of the oscillator towards 16.500 Mc. As the frequency corrects towards zero error, the 4 kc audio frequency becomes lower in frequency until it approaches zero. At this time the two 1500 kc IF signals arrange their phases in such a way that just the correct amount of DC control voltage is present to maintain the oscillator at zero error. The crystal is then locked to 16.500 Mc with the accuracy of the frequency standard.

186. Any of the required NC injection frequencies between 2.5 and 23.5 Mc can be selected by simply switching the correct crystal in the oscillator. Since oscillator error is phase corrected, trimmers and tuned coils are not required to adjust crystal frequency. Because a flat megacycle spectrum is used for phase comparison, there is always a spectral point 1.5 Mc above and below the desired frequency. No tuning or selection of spectral points is required and a fixed 1.5 Mc IF is always used. Fig 24 is a block diagram of the phase lock circuit.

Circuit Description of the Megacycle Synthesizer (fig 1018 and 1019)

187. The Megacycle Synthesizer subassembly produces the injection frequencies between 2.5 and 23.5 Mc for injection into the Translator. This subassembly also produces the Hi/Lo switching information for the 100 kc Synthesizer and the Translator subassemblies.

Injection Frequency Generation

188. The 2.5 to 23.5-Mc band of injection frequencies is produced by oscillator A3Q1, A3Q2. (fig 1019) The frequency output from oscillator A3Q1, A3Q2 is determined by one of seventeen crystals (A41 through A517), which are automatically switched into the circuit by the digital tuning circuit according to the setting of the NC controls on the RF-662/800 front panel. Due to the wide range of frequencies used, it is necessary to switch a
FIG 24 - BLOCK DIAGRAM OF THE PHASE LOCK CIRCUIT
capacitor (A5C1 through A5C17) for each crystal into the feedback network in order to produce a uniform output level. The selected capacitor and capacitor A7DB form a reactive voltage divider. The signal at the output of oscillator A3Q1, A3Q2 is applied back to this divider through resistor A3R15 and thermistor A3R17. Thermistor A3R17 compensates the amount of feedback as the temperature changes. The output from oscillator A3Q4, A3Q5 is limited to the forward voltage drop of diodes A3CR2 and A3CR3. The output from oscillator A3Q1, A3Q2 is locked to the exact frequency required by voltage variable capacitor (VVC) A3CR1. The dc control voltage for VVC A3CR1 is the output voltage from dc amplifier A2Q3. Capacitor A3Q6 is a temperature compensating capacitor, providing compensation for variations in crystal frequency as the temperature varies. The output from oscillator A3Q1, A3Q2 is coupled by capacitor A3Q6 to isolation amplifier A2A1Q1 and emitter follower A3Q7. Emitter follower A3Q7 prevents the circuits of translator module 1A3 from loading the output from oscillator A3Q1, A3Q2. The output from emitter follower A3Q7 is coupled to G1A2 through capacitor G2, resistor R14 and the parallel tuned circuit G10 and L2. Thermistor R16 and resistor R16 form a temperature compensating network across resistor R13. The parallel tuned circuit is resonant at 51M\(\text{c}\). This reduces the sixth harmonic of the 8.5 M\(\text{c}\) crystal to effectively eliminate spurious frequencies in the receiver-transmitter. A further benefit from the use of these components is that the output of the module is much flatter over the span of frequencies generated by the 17 crystals.

The Phase Lock Loop

The phase lock loop is used to generate a dc voltage proportional to the frequency error of oscillator A3Q1, A3Q2. This dc voltage is applied to voltage variable capacitor A3CR1 to keep the crystal oscillator locked to the frequency standard.

The 1-M\(\text{c}\) output from frequency standard module 1A3 is applied to connector J1A1, (fig 1016) from which it is applied through resistor A1R2 to autotransformer A1T1. Resistor A1R2 prevents loading of the 1-M\(\text{c}\) input signal. The level of the 1-M\(\text{c}\) signal is raised by autotransformer A1T1, which is tuned to 1-M\(\text{c}\) by capacitor A1C1, and is applied to a clipper circuit consisting of diode A1CR2 and resistor A1R3. The positive portion of the 1-M\(\text{c}\) signal is removed and the resulting negative pulses are coupled by capacitor A1C2 to the base of pulse amplifier A1Q1. The negative going pulses drive pulse amplifier A1Q1 into saturation, producing a positive-going pulse with a fast rise time at the collector of pulse amplifier A1Q1. The base of pulse amplifier A1Q1 attempts to go more positive than the emitter, diode A1CR3 will become forward biased. This clamps the base voltage, preventing excessive reverse bias on the base-to-emitter junction of pulse amplifier A1Q1. The positive pulsed output from pulse amplifier A1Q1 is coupled by capacitor A1C6 to the base of pulse shaper A1Q2, driving it into saturation. The positive pulsed input to pulse shaper A1Q2 is differentiated by capacitor A1C1 and the input impedance to pulse shaper A1Q2. Capacitor A1C6 is used to compensate for frequency roll-off at the higher frequencies and maintain a uniform spectrum output from pulse shaper A1Q2. The negative pulsed output from pulse shaper A1Q2 is coupled to the base of pulse shaper A1Q3 by capacitor A1C6. The negative pulsed input to pulse shaper A1Q3 is differentiated by capacitor A1C6 and the input impedance of pulse shaper A1Q3. The shape of the waveform is determined mainly by the value of capacitor A1C6. Pulse shaper A1Q3 is a class C amplifier which produces a sharp amplified output pulse. Diode A1C2B4, like diode A1C3, is used as a protective device to clamp the positive portions of the input signal. The positive-going output signal is developed across inductor A1L1. The value of inductor A1L1 is chosen so that the output signal will have a correct bandwidth and amplitude. A nearly uniform amplitude from 1 to 25 M\(\text{c}\). The negative portions of the output signal are removed by the clipping circuit, consisting of diode A1CR5 and resistor A1R17. The positive pulsed output from pulse shaper A1Q3 is coupled by capacitor A2C2 to the base of mixer A2Q1.

The output from oscillator A3Q4, A3Q5 is coupled by capacitor A2A1Q1 to the input of isolation amplifier A2A1Q4. The output of isolation amplifier A2A1Q4 is coupled by capacitor A2C3 to the base of mixer A2Q1. Isolation amplifier A2A1Q4 prevents any of the pulsed output from pulse shaper A1Q3 from being fed back to oscillator A3Q4, A3Q2 and producing unwanted spurious signals. The double-tuned output circuit (transmitter A2T1, capacitor A2C6 and transformer A2T2, capacitor A2C8) for mixer A2Q1 is tuned to 1.5 M\(\text{c}\). Therefore, the oscillator output will be subtractively mixed in mixer A2Q1 with those two spectrum points of the pulsed output from pulse shaper A1Q3 that will produce two tones close to 1.5 M\(\text{c}\). This results in a two-tone output from mixer A2Q1, the envelope of which is varying by twice the error of the output from oscillator A3Q4, A3Q2. For example, assume that the input from oscillator A3Q4, A3Q5 should be 2,500000 M\(\text{c}\), but is 500000 M\(\text{c}\) (100 cycle error). This signal will mix with the 1-M\(\text{c}\) and 4-M\(\text{c}\) spectrum points, resulting in two tones: 1,500000 M\(\text{c}\) and 4,999900 M\(\text{c}\). Therefore, the envelope of the two tone signal will be varying at a 200 cycle rate. The output from mixer A2Q1 is coupled by capacitor A1C7 to another tuned circuit (A2T2, A2C8), which in combination with the tuned output of
miller A2Q1, provides the selectivity required to attenuate all mixer products of mixer A2Q1 except those at or near 1.5 Mc. The output from this tuned circuit is coupled by capacitor A2Q2 to the base of IF amplifier A2Q2. A small amount of degeneration, to stabilize the gain of IF amplifier A2Q2, is provided by the temperature compensated network consisting of resistor A2R1 and thermistor A2R2. The output from IF amplifier A2Q2 is developed across the tuned circuit consisting of capacitor A2501 and the primary of transformer A2T5, from which it is coupled to diode A2CR1. Diode A2CR1 envelope detects the two-tone output from IF amplifier A2Q2. Assuming the same error as before, the output from diode A2CR1 would be a DC level varying at 200 c/s. This signal is applied to the emitter of dc amplifier A2Q3. The input level to dc amplifier A2Q3 is set by resistor A2R15. Thermistor A2R20 provides temperature compensation for the base and emitter biasing circuits. The output from dc amplifier A2Q3 is applied to VVC A3CR4, a level determined by the amount of error of the crystal. This output is a DC level, which is varied by the error (ac) voltage. The ac output of dc amplifier A2Q3 varies the capacitance of VVC A3CR by varying the applied voltage about the DC reference, thus, sweeping the frequency of oscillator A3Q1, A3Q2 accordingly. Since the loop is closed, this sweep frequency will decrease with time due to the decrease in the oscillator error as it is swept. When the error signal has been reduced to one that is within the pull-in capture range of the oscillator, the oscillator will be locked exactly at the desired frequency. At this time, only the DC level will be applied to VVC A3CR1 to hold the oscillator in lock. If the phase of the oscillator begins to drift, the DC reference on VVC A3CR1 will shift accordingly to hold the oscillator locked to the 1-Mc reference signal. Inductance A3 L3 and capacitor A3 C2 form a series tuned circuit resonant at 1.5 Mc. Any 1.5 Mc signal still remaining on the DC control voltage is effectively shunted to ground. Varicap CR1 is back biased by +20V through resistor R2.

HI/LO Information

192. The HI/LO information is generated by switch A6S1G. (fig 1019) The position of the switch is determined by the setting of the HI-66/EOR front panel H/L controls. The LG digit selected at the front panel determines whether a HI or LO output should be produced in order that the pre-determined mixing process can be satisfied. Either 20 volts DC (HI) or ground (LO) is applied to pins 1 and 2 of connector J1 by switch A6S10. This information is applied to 100-kc synthesizer module A2 to select the correct band of frequencies and to translator module A8 to select the corresponding filtering.

100 kHz Synthesizer 1A2

General

193. The 100 kHz synthesizer produces two sets of injection frequencies. These are automatically switched according to the frequency scheme by the HI/LO band information source. The unit also corrects the crystal errors by a drift cancelling technique.

194. The 100 kHz synthesizer produces the injection frequencies for the 100 kc digit conversion. It corrects its own errors but carries the errors of the 10-1 kc synthesizer, as part of a larger error correction loop. Block diagram fig 25 illustrates the basic system used in the 100 Kc synthesizer. The switching indicated is done by diode gates or by activating or deactivating a portion of the circuitry.

100 kHz Synthesizer Error Correction

195. A drift cancelling technique is used in the 100 kc synthesizer subassembly. Double mixing cancels the error of the switched crystal oscillator as compared to the reference frequency. This system eliminates locked oscillators so that failures within the control system will not cause out of channel operation. The error correction system is presented by an arithmetical example, assuming a crystal error.

196. Assume that the crystal in use is crystal Y10 for the digit 9. If exactly correct, this crystal would be 5.453 Mc. Assign an error of 250 cycles on the low frequency side, making the crystal 5.452750 Mc. The only spectrum point, with which this crystal will mix and produce a mixer product near 10.747 Mc, is 46.2 Mc.

\[
\begin{align*}
\text{Spectrum point} & \quad 16,200,000 \\
\text{Crystal} & \quad 5,452,750 \quad \text{Subtract} \\
\text{Mixer product} & \quad 10,747,250
\end{align*}
\]
Fig 25 - Block diagram of 100 kc synthesizer
Filter
A2F4 (10.747 ± crystal errors)
10.747250
10 & 1 kc error signal
+7.440000 Add
17.847250
Filter
A3Y2 (17.847 ± crystal error)
17.847250
Balanced Mixer A1CR3
Crystal
Injection Frequency
+5.152750 Add
23.300000

This injection frequency, for the digit 9, is exactly correct even though the crystal was
in error by 250 cycles. This is brought about by the fact that the crystal frequency was
both subtracted and added in the computation. This would also have come out correctly had
the crystal been in error on the high frequency side. This system will also work in high
band since this operation merely adds 10 Mc which already has the accuracy of the frequency
standard.

197. This automatic error cancellation scheme will also take place for small crystal
frequency drift due to temperature. The accuracy will be the same as that of the frequency
standard from which the spectrum point derived its accuracy. Note that this arrangement
correction only the errors due to the crystals in the 100 kc synthesizer. It was assumed that
the 7.4 Mc addition contained no errors. Actually the 7.4 Mc signal is carrying the com-
bined errors of the crystals in the 10 and 1 kc synthesizer. This error correction for the
10 and 1 kc synthesizer is detailed in the circuit description of the relevant sections.
Fig 26 is a block diagram illustrating the above error correction.

Circuit Description of the 100 kc Synthesizer (figs 1020 and 1021)

198. The function of the 100 kc Synthesizer Subassembly is to produce two bands of
frequencies, in 100 kc increments, for injection into the translator. One band includes the
frequencies, 22.4 to 23.3 Mc, and the other includes the frequencies, 32.4 and 33.3 Mc.
These injection frequencies are necessary to perform the second conversion (transmit and
receive).

Injection Frequency Generation

199. The 22.4 to 23.3 Mc band of frequencies is produced by mixing the output from the
switched crystal oscillator A4Q1 (fig 1020) with a 17.847 Mc signal. This 17.847 Mc signal
is produced by mixing the output from the switched crystal oscillator A4Q1 with a spectrum
point of the 100 kc spectrum from the frequency divider subassembly A6 (fig 1016). The
resulting product is then mixed with the 7.4 Mc and output from the 10 and 1 kc synthesizer
subassembly A4. (fig 1022) The 32.4 to 33.3 Mc band of frequencies is produced by mixing
the output from the switched crystal oscillator A4Q1 with a 27.847 Mc signal. This 27.847
Mc signal is produced by mixing the 17.847 Mc signal with a 10 Mc frequency from the fre-
quency standard subassembly A4. (fig 1022) Switched crystal oscillator A4Q1 produces any
one of ten frequencies between 4.253 and 5.453 Mc, in 100-ke steps. The frequency produced
is determined by the selection of one of ten crystals (A4X1 through A4X10). The output
from oscillator A4Q1 is coupled by capacitor A4C6 through resistor A2X20 to the emitter of
isolation amplifier A2A4Q1. This stage is a grounded base configuration. The output is
also gated through diode A1CR1 or A1CR2, (fig 1021) depending on the required band of
frequencies.

200. The gate (A1CR1 or A1CR2) through which the output from oscillator A4Q1 passes
is determined by the HI/LO switching voltage. This voltage is dependent upon whether the HI or
LO band of injection frequencies is the required output from 100-ke synthesizer A2. Zener
diode A3YR regulates the 20-volts dc supply voltage to 10 volts dc. This dc voltage is
applied to the anode of diode A1CR1 and the cathode of diode A1CR2. When the LO band of
mixing frequencies is required, 20 volts dc is applied through current limiting resistors
A1R2 and A1R3 to the anode of diode A1CR2 and the cathode of diode A1CR1. This will forward
bias diode A1CR2 and reverse bias diode A1CR1. When the HI band of mixing frequencies is
required, ground is effectively applied to the anode of diode A1CR2 and the cathode of diode
A1CR1. This causes diode A1CR2 to be reverse biased and diode A1CR1 to be forward biased.
FIG 26 - 100 KC SYNTHESIZER ERROR CORRECTION

ELECTRICAL AND MECHANICAL ENGINEERING INSTRUCTIONS (AUST)

TELECOMMUNICATIONS H 172

100 KC INJECTION
22.4 MC TO 23.3 MC

ADDITIVE MIXER

SWITCHED XTAL OSCILLATOR
4.553 MC TO 5.453 MC

SUBTRACTIVE ERROR MIXER

7.1 MC ADDITIVE MIXER

7.1 MC INPUT

10.747 MC FILTER

15.3 MC

SPECTRUM OUTPUT

16.2 MC

KEYED OSCILLATOR SPECTRUM GENERATOR

100 KC KEYING PULSE

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204. When the HI band of mixing frequencies is required, diode A1C82 is forward biased, allowing the output from oscillator A1Q1 to pass. This signal is coupled by capacitor A1Q4 to mixer A1C84. Mixer A1C84 consists of two matched backward diodes that form a balanced circuit with the primary of transformer A1T1. These diodes are not used as zener diodes, but are used because of their low forward conduction voltage. The output from oscillator A1Q1 is mixed with the 27.847 Mc signal which is applied to the center-tap of transformer A1T1 (Fig. 1024) to produce a band of frequencies between 32.4 and 33.3 Mc. Mixer A1C82, due to its balanced condition, will attenuate the 27.847 Mc signal. Most of the output from oscillator A1Q1 will be dropped across the matched backward diodes. The output from mixer A1C84 is coupled through transformer A1T1 and capacitor A1C7 to the base of amplifier A1Q1. When the HI band of mixing frequencies is required, the ground present on the HI/LO control line is applied to resistor A1R7, terminating it. The supply voltage is applied to resistors A1R5 and A1R1. Therefore, the supply voltage will be developed across voltage divider A1R7, A1R9 to provide the proper bias for amplifier A1Q1. When the LO band of mixing frequencies is required, the HI/LO control line has 20 volts dc on both ends, reverse biasing amplifier A1Q1. The mixing products from mixer A1C84 are raised in level by amplifier A1Q4 and are applied to the tuned filter circuit. The tuned filter circuit has a passband from 32.4 to 33.3 Mc, eliminating all harmonic and mixing products, except the desired output. The output from the tuned filter is coupled by capacitor A1C22 to the base of amplifier A1Q5. When the HI band of mixing frequencies is required, the base bias voltage divider A1R29, A1R24 is terminated with the ground on the HI/LO control line. When the LO band of mixing frequencies is required, 20 volts dc is present on both ends of the voltage divider to reverse bias amplifier A1Q3. A small amount of degeneration is provided by resistor A1R27 to stabilize the operation of amplifier A1Q3. A trap circuit is placed in the emitter circuit of amplifier A1Q3 to eliminate any of the 27.847 Mc that was not cancelled out by balanced mixer A1C84 or attenuated by the tuned filter. At 27.847 Mc, trap circuit A1C88, A1L4 will provide increased degeneration. The output from amplifier A1Q3 is coupled to the base of wide band amplifier A1Q5 through tuned transformer A1T7 and capacitor A1C32.

205. When the LO band of mixing frequencies is required, diode A1C82 is forward biased, allowing the output from oscillator A1Q1 to pass. The LO band circuits are identical to the HI band circuits except for the switching voltages and frequencies that are used. Balanced mixer A1C84 mixes the output from oscillator A1Q1 with the 17.847 Mc signal. The mixing products are amplified by amplifier A1Q2 and applied to a tuned filter circuit which is raised in level by amplifier A1Q4 and applied to wideband amplifier A1Q5. Amplifier A1Q4 has a trap circuit in the emitter to attenuate any 17.847 Mc that was not cancelled out by balanced mixer A1C84 or attenuated by the tuned filter. Amplifier A1Q2 is turned on when the LO band of mixing frequencies is required, by the presence of 20 volts dc at both ends of the voltage divider and to emitter resistor A1R4, turning off amplifier A1Q2. When the LO band of mixing frequencies is required, 20 volts dc from the HI/LO control line is applied to emitter load resistor A1R28 to forward bias amplifier A1Q2. When the HI band of mixing frequencies is required, ground is applied to the emitter resistor, reverse biasing amplifier A1Q4. Diode A1C82 protects amplifier A1Q4 from excessive base-to-emitter (reverse) bias. This is done in order to maintain the reverse bias on the base-to-collector junction to prevent distortion of the input signal to wide band amplifier A1Q5 when the HI band path is used.

206. Wide band amplifier A1Q5 raises the level of the 22.4 to 23.5 Mc or 32.4 to 33.3 Mc signals. The output from wideband amplifier A1Q5 is coupled by capacitor A1C2 to the base of emitter follower A1Q4. Emitter follower A1Q4 provides impedance matching between 100-ko synthesizer module 142 and translator module 146. (Fig. 1007) The output from emitter follower A1Q4 is coupled by capacitor A1C2 to connector J1A4 for application to translator module 146.

17.847 Mc Generation

207. The 17.847 Mc signal is produced by substractively mixing the output from oscillator A1Q1 with the 100-kc spectrum output from the frequency divider subassembly 146. This produces a 10.747 Mc signal which is additively mixed with the 7.4 Mc output from the 10 and 1 kc synthesizer subassembly 144. (Fig. 1025) The output from oscillator A1Q1 (Fig. 1026) is coupled by capacitor A2C10 to the emitter of isolation amplifier A2Q4. Isolation amplifier A2Q4 is used to prevent any of the spectrum frequencies from mixer A2Q4 from being applied to the other output circuit paths of oscillator A1Q1. The output from isolation amplifier A2Q4 is developed across transformer A1T3, from which it is couple by capacitor A2C18 to the base of mixer A2Q4. The 15.3 to 16.2 frequency spectrum output from frequency divider module 146 is applied to connector J1A5, from which it is coupled by capacitor A2C2;
to the emitter of mixer A3Q4. Mixer A3Q4 mixes the signal from oscillator A4Q1 with each of the spectrum points. The resulting mixing products are developed across a tank circuit, consisting of capacitor A2Q20 and the primary of transformer A2T2, which is tuned to 10,714 Mc. The output from filter A2FL1 is capacitively divided to the tuned tank circuit consisting of capacitors A2CQ7 and A2CQ4 and the primary of transformer A2Q4. The 10.714 Mc output is coupled by capacitor A3Q20 to the base of mixer A3Q2.

205. The 7.1 Mc output from 10- and 1-kc synthesizer module 1A4 is applied to connector J4A2 from which it is coupled by capacitor A3CQ7 to the emitter of mixer A3Q2. Mixer A3Q2 mixes the 10.714 Mc with the 7.1 Mc signals and develops the resulting mixing products across the tuned circuit consisting of the primary of transformer A3T4 and capacitor A3CQ16. This circuit is tuned to 7.847 Mc, the desired additive product. The amount of desired output from mixer A3Q2 is controlled by the dc output of the AGC circuit. The base bias for mixer A3Q2 is developed by voltage divider A3R3, A3R4, A3R5 from the 20 volts dc applied to resistor A3R3 and the AGC voltage applied to resistor A3R4. The gain of mixer A3Q2 will vary as the base bias is varied by the AGC voltage.

206. The output from mixer A3Q2 is coupled to a crystal filter circuit consisting of transformers A3T3 and A3T5, capacitors A3CQ3 and A3CQ4, and crystal A3Y2. Crystal A3Y2 is tuned in series with a 7.5 Mc resonant at 7.847 Mc but is worked so that it is series resonant at 7.847 Mc. Capacitor A3CQ4 is adjusted to balance the filter circuit and to prevent any undesired signal from passing through the filter circuit. The output termination of the crystal filter circuit is the tuned tank consisting of the primary of transformer A3T3 and capacitor A3CQ3. The output of the crystal filter is applied to balanced mixer A1CR3, and also is coupled by capacitor A3Q8 to the base of mixer A3Q4.

27,847 Mc Generation

207. The 27.847 Mc signal is produced by mixing the 17.847 Mc with the 10 Mc output from the frequency standard subassembly 1AJ. (fig. 1002)

208. Mixer A3Q4 (fig. 1020) is turned on when the desired injection frequency to transistor subassembly 1AJ is in the HI band. This is accomplished by applying the ground from the HI/LO control line to resistor A3R8 to terminate it. Therefore, the 20 volts dc supply voltage will be developed across base bias voltage divider A3R7, A3R8. If the LO band of injection frequencies is required, 20 volts dc is applied to both ends of this voltage divider, reverse biasing mixer A3Q4, shutting it off. The 10-Mc output from frequency standard module 1AJ is applied via connector J4A1 to the anode of diode A3CQ2. If the LO band of injection frequencies is required, the 20 volts dc is also applied through resistor A3R4 to the anode of diode A3CQ4, forward biasing it. Therefore, the 10-Mc signal will be shunted to ground. If the HI band of mixing frequencies is required, the HI/LO control line will apply ground to resistors A3R5 and A3R6. This will forward bias diode A3CR1. Therefore, the 10-Mc signal will pass and be coupled by capacitor A3CQ8 to the emitter of mixer A3Q4. Mixer A3Q4 mixes the 17.847 Mc signal and develops the resulting mixing products across the tuned circuit consisting of capacitor A3CQ1 and the primary of transformer A3T2. This circuit is tuned to the 27.847 Mc additive mixing product.

209. The output from mixer A3Q4 is coupled to a crystal filter circuit consisting of transformers A3T3 and A3T5, capacitors A3CQ3 and A3CQ5, and crystal A3Y2. This circuit functions identically to the 17.847 Mc crystal filter circuit to provide the required 27.847 Mc output. The 27.847 Mc output from the crystal filter circuit is applied to balanced mixer A3CR3.

AGC Circuit

210. The AGC voltage developed by this circuitry is applied to mixer A3Q2 (fig. 1020) to hold the output constant.

211. The injection frequency output from emitter follower A2Q1 (fig. 1021) is coupled to the base of AGC amplifier A2Q3 by capacitor A2Q3. AGC amplifier A2Q3 raises the level of the input from emitter follower A2Q1 and develops it across inductor A2L3 which is used to adjust for the difference in levels between the HI and LO bands of injection frequencies. Therefore, inductor A2L3 can be set to provide uniform output for both the HI and LO bands. Resistor A2R5 produces degeneration to increase the bandwidth and provide additional stability for AGC amplifier A2Q3. The bias for dc amplifier A2Q2 is developed by the temperature compensated voltage divider consisting of resistors A2R10, A2R13, A2R17, and A2R18 and thermistor A2R2. Diode A2R12 will detect the negative portions of the output from AGC amplifier A2Q3 and charge capacitor A2Q3. As the signal strength increases, the base bias on amplifier A2Q2 will become more negative, thus cutting down its rate of conduction. DC
amplifier A2Q2 will also invert the negative voltage on its base, since its collector voltage is positive. The output from dc amplifier A2Q2 is filtered by capacitor A2C9 to eliminate ripple and prevent any low frequency oscillation in the AOC loop. As the output gain varies, the conduction of dc amplifier A2Q2 varies. This in turn controls the base bias of mixer A5Q2, and therefore, the stage gain of mixer A3Q2. Since this circuit forms a closed loop with all other circuits of 100-kc synthesizer module 1A2, the gain of all circuits will reach a steady state condition. Therefore, the output from emitter follower A2Q4 will reach a constant value.

![Block Diagram]

**FIG 27 - BLOCK DIAGRAM OF BASIC SYSTEM FOR 10 KC AND 1 KC SYNTHESIZER**
Circuit Description for the 10 and 1 kc Synthesiser (Figs 1022, 1023)

212. The 10 and 1 kc Synthesiser Subassembly produces the injection frequencies for the 10 kc and 4 kc digits conversion. These are used in the translator subassembly for the third conversion receive or the first conversion transmit. It also produces an error signal, which is used for error cancellation.

Injection Frequency Generation

213. The injection frequencies are produced by subtractively mixing the outputs of two crystal oscillators.

214. Crystal oscillator A1Q2 (Fig 1022) produces any one of ten frequencies between 6.59 and 6.59 Mc, in 0.5-ke steps. The frequency produced is determined by the selection of one crystal oscillator (A1Q4 to A1Q10) using the 10-ke (X2) switch A1M1, on the front panel of the 6-662/680. The output from oscillator A1Q2 is amplified by diodes A1Q1 and A1Q2. A small reverse bias is applied to these diodes by resistors A1R2 and A1R3 to maintain a higher crystal Q over the environmental range. The output from oscillator A1Q2 is coupled by capacitor A1C76 to the base of mixer A1Q5 and is coupled by capacitor A1Q6 to the base of isolation amplifier A1Q3.

215. Crystal oscillator A1Q5 produces any one of ten frequencies between 1.940 Mc and 1.949 Mc in 1-ke steps. The frequency produced is determined by the selection of one of ten crystals (A1Y1 to A1Y10) using the 1-ke (X) switch A1M1, on the front panel of the 6-662/680. The output from oscillator A1Q5 is limited by diodes A1C82 and A1C89. Diodes A1C82 and A1C89 are slightly reverse biased by the voltage from divider A1M34, A1M35 to maintain a higher crystal Q over the environmental range. The output from oscillator A1Q5 is coupled by capacitor A1Q3 to the base of keyed amplifier-spectrum generator A1Q4 and by capacitor A1C22 to the base of emitter follower A1Q7. Voltage divider A1R30, A1C25 provides a low impedance to the output from oscillator A1Q5 and high impedance to 1-ke feedback from keyed amplifier-spectrum generator A1Q4 to minimise the amount of 1-ke pulses appearing in the 10- and 1-ke output. The output from emitter follower A1Q7 is coupled by capacitor A1C14 to emitter of mixer A1Q5. Emitter follower A1Q7 prevents oscillator A1Q5 from being loaded by mixer A1Q5.

216. The 1.940- to 1.954 Mc signal is subtractively mixed with the 6.59- to 6.59 Mc signal in mixer A1Q5 to produce the 4.551- to 4.559 Mc band of injection frequencies. The output circuit for mixer A1Q5 is a triple-tuned bandpass filter. The filter removes only the difference between the 3.59 to 6.59 Mc and 1.940- to 1.954 Mc signals (4.551 to 4.559 Mc in 1-ke steps). The filter has a bandwidth of slightly greater than 100 kc to allow for temperature drift of the filter, but has sufficient selectivity to attenuate any frequency outside the bandpass. Capacitors A1C13 and A1C18 are an integral part of the filter and couple the signal between the sections of the filter. The output from the triple-tuned bandpass filter is coupled by transformer A1T2 to connector J1B-A3 for application to translator subassembly 148. (Fig 1007)

217. The NOISE BLANKER switch is set ON and ignition type (pulsed) noise is present in the received signal, the pulsed output from noise blanker assembly 14A6 will be present at connector J1B-A2. (Fig 1022) This signal (negative pulse) will be coupled to the base of A1Q6. If no pulses are present, noise blanker A1Q6 is not conducting and diode A1C86 is forward biased through resistor A1R23. This places the low side of tank circuit A1C16, A1L2 ac ground, allowing the 10- and 1-ke signal to pass. When the pulses are present, noise blanker A1Q6 is switched into saturation. Therefore, the collector noise blanker A1Q5 is effective at the supply voltage level, causing diode A1C87 to be forward biased. The saturation voltage drop of noise blanker A1Q6 and the forward conduction voltage drop of diode A1C87, combined, is less than the voltage drop of diode A1C86. This places a non-conducting condition on diodes A1C86. Noise blanker A1Q6 and diode A1C87 place the top of the tank circuit at ac ground potential when they are saturated by a blanking pulse. Therefore, the injection to translator subassembly 148 is momentarily removed, thereby turning off the received signal for the duration of the pulse. In addition, diode A1C86 is used to reference filter section A1L2, A1C18 at a nearly constant dc level at all times. This prevents the filter section from ringing when the pulsed output from noise blanker A1Q5 is applied and removed. Resistor A1R24 limits the current flow through noise blanker A1Q6.

Error Signal Generation

218. The errors of two sets of crystals are combined into a 7-1 Mc error signal. This signal is fed into the 10-ke synthesiser where it enters an error cancellation loop involving a path through several subassemblies.
The output from oscillator A1Q2 (fig 1022) is coupled by capacitor A1Q5 to the base of isolation amplifier A1Q4. The output from isolation amplifier A1Q4 is developed across the LC tank circuit consisting of inductor A1L3 and capacitor A1C24, from which it is coupled by capacitor A2Q1 to the base of mixer A2Q4. The output level from isolation amplifier A1Q4 is such that it will not affect the conversion gain of mixer A2Q4. Therefore the tuning of tank circuit A1L3, A1C24 is not critical. Isolation amplifier A1Q4 prevents mixer A2Q4 from loading oscillator A1Q2 and also prevents any of the 10-ke spectrum from appearing in the 10- and 1-ke output. The 10-ke spectrum output from frequency divider module A6 is applied to connector J1A-A1. From here it is coupled by capacitor A2Q3 to the emitter of mixer A2Q4. The 6.59- to 6.59-ke output from oscillator A1Q2 is additively mixed with the 10-ke spectrum (2.45 to 2.57 ke). The output circuit for mixer A2Q4 is tuned to 9.07 ke, attenuating some of the other mixing products. The 9.07 Mc signal is applied to crystal filter A2PFL, to attenuate (more than 50 db) all mixing products except the desired 9.07 Mc. The 9.07 ke output from filter A2PFL is coupled by capacitor A2Q8 to the base of mixer A2Q2.

The 1-ke pulsed output from the frequency divider subassembly A6 (fig 1037) is applied to connector J1A-A2. (fig 1022) From here it is coupled by capacitor A1Q3 to the base of pulse amplifier A1Q4. With no pulse input, pulse amplifier A1Q4 is biased to saturation. The positive portions of the 1-ke input will drive pulse amplifier A1Q4 into cutoff. This effectively switches the collector of pulse amplifier A1Q4 from 20 to zero volts at a 1-ke rate. This pulsed output is used to gate keyed amplifier-spectrum generator A1Q3 on and off at the 1-ke keying rate. The output from the keyed amplifier-spectrum generator is tuned to 1.97 Mc. The output from oscillator A1Q8 (1.940 to 1.949 Mc) is additively mixed in the primary of transformer A1T1 with the harmonic of the 1-ke pulsed input (21 to 30 ke) that will produce a 1.97 Mc output. Diodes A1CR3 and A1CR4 provide a complete short across the primary of transformer A1T1 (while in the forward biased condition) at the 1-ke keying rate. Diode A1CR5 is used to place the top of transformer A1T4 at ground potential and to reference the tuned circuit at the dc supply voltage, thereby preventing the tuned circuit from ringing as the short is switched in and out of the tuned circuit. The output from keyed amplifier-spectrum generator A1Q3 is tuned for 1.97 Mc to attenuate the other mixing products. This signal is applied to filter A2PFL2, which attenuates (more than 60 db) all the spectrum points except the desired 1.97 Mc. The 1.97 Mc output from filter A2PFL2 (fig 1023) is coupled by capacitor A2Q8 to the base of mixer A2Q2.

Mixer A2Q2 additively mixes the 1.97 Mc signal with the 9.07 Mc signal to produce the desired 7.1 Mc output. The output from mixer A2Q2 is coupled by capacitor A2C1 to the base or amplifier A2Q3. The gain of mixer A2Q2 is controlled by the A2C voltage applied to resistor A2R7. Amplifier A2Q3 raises the 7.1 Mc signal to a level suitable for use in 100-ke synthesizer module A2. The output from amplifier A2Q3 is coupled by transformer A2T3 to connector J1B-A1.

The output from amplifier A2Q3 is coupled by capacitor A2C1 to the base of amplifier A2Q5. Amplifier A2Q5 raises the level of the 7.1 Mc signal and develops it across the tuned tank circuit A2R4 and A2C6. The base of detector-dc amplifier A2Q5 is referenced near the dc supply voltage level by diode A2CR1, thereby controlling the biasing of detector-dc amplifier A2Q5. When the 7.1 Mc signal swings positive, diode A2CR1 conducts more, causing the base-to-emitter junction of detector-dc amplifier A2Q5 to be even more reverse biased. When the 7.1 Mc signal swings negative, diode A2CR1 conducts less, forward biasing detector-dc amplifier A2Q5. The 7.1 Mc signal will be half-wave rectified by detector-dc amplifier A2Q5, filtered by capacitors A2C20, A2C21, and A2C22 and applied to resistor A2R7 to control the gain of mixer A2Q2. The output level of the 7.1 Mc signal is determined by the amount of forward bias on detector-dc amplifier A2Q5. This closed loop circuit will stabilize and ensure a constant 7.1 Mc output from mixer A2Q2. Resistor A2R18 provides a dc path for A2CR1. Capacitor A2C18 is the RF bypass for resistor A2R18. Resistor A2R17 is used to adjust the load for the secondary of transformer A2T4 and the amount of signal to be detected, thereby adjusting the output level of the 7.1 Mc signal.

**Error Correction for the 10- and 1-Kc Synthesizer**

The general principle of error correction for the 10- and 1-ke Synthesizer Subassembly is the same as that employed in the 100-ke Synthesizer. However, the error correction loop involves other subassemblies. These are the 100-ke Synthesizer and the Translator.

The crystals used in the oscillators of the 10- and 1-ke synthesizer are loose, "tolerance", and are not necessarily accurate when compared to the frequency standard. They are brought into agreement with the frequency standard by a drift cancelling technique. These crystals are used as switched oscillators in conjunction with bandpass filters in a circuit which compares the free running crystal frequency to a spectrum of frequencies based...
on the standard frequency. A double mixing process cancels the error of the switched oscillator compared to the reference frequency. This system eliminates locked oscillators so that failure within the control system will not cause out-of-channel operation. The method of operation for the 10- and 1-ke error cancelling loop is similar to that of the 100-ke synthesizer.

225. The error components of both the 10-ke and the 1-ke oscillators are combined in a mixer, producing an output of approximately 7.1 ke. If no error exists in either the 10-ke or the 1-ke oscillator, the output frequency will be exactly 7.1 Mc. This signal, carrying the combined errors of the 10- and 1-ke oscillators, is routed to the 100-ke synthesizer subassembly where it is added to the injection frequency generated by this synthesizer. Block diagram, Fig 28 shows path of the signal through the translator-synthesizer subassemblies.

226. The error cancelling loop is basically the same as that used in the 100-ke synthesizer. However, the path leads through the 100-ke synthesizer where the 7.1 Mc signal adds the errors of the 10- and 1-ke synthesizer crystals to the 100-ke injection signal. Note that this 100-ke injection signal is already corrected for any errors of the crystals in the 10-ke synthesizer. In the 100-ke synthesizer, 10 Mc may also be added depending upon the megacycle frequency. This in no way changes the results.

227. The injection signal, carrying the errors on the 10- and 1-ke crystals is now applied to the second conversion mixer. The second conversion mixer product now contains these same errors. This signal is now converted to the 7.75 Mc IF frequency (receive mode assumed) in the third conversion mixer. In this conversion the second conversion signal and the injection signal from the 10- and 1-ke synthesizer are combined. The injection signal carries the same combined crystal errors but having the opposite sign. The error is cancelled with the resulting 7.75 Mc IF signal free of error. It should be noted that the system not only cancels crystal error but also continuously corrects for frequency error due to temperature change.

228. In summary, for any given RF frequency the 10- and 1-ke synthesizer produces two signals. These are an injection signal (7.1 Mc + crystal error) and an error signal (7.1 Mc + crystal error). The 7.1 Mc signal is carried by the 100 ke injection signal to the translator. The conversion signal also contains the error. The two signals finally meet in the third conversion where error is cancelled because the two signals contained the same error but of opposite sign. Block diagram, Fig 28, shows only the basic elements of the system.

CIRCUIT DESCRIPTION DC TO DC CONVERTER 1A1 (FIG 1024)

General

229. The DC to DC converter subassembly converts the 27V supply voltage to the DC and AC voltages required by the RF amplifier subassembly. It also contains the circuitry for a regulated +20V supply, used throughout the receiver-transmitter.

230. This type of converter consists basically of a self-oscillating system which supplies both the feedback required and the primary input to the transformer. Fundamentally, current flows in the collector circuit in excess of that flowing in the other collector circuit. Due to small differences in the push-pull circuitry one of the transistors starts to conduct first. When this happens, the current flowing in the winding connected to the collector of this transistor induces a current in the other windings of the transformer. The polarity of the voltage from the winding feeding the base of the "on" transistor is such that this transistor is driven further into conduction until saturation is reached. Let the "on" transistor be Q2. The winding, connecting to the base of Q1, supplies an out-of-phase feedback signal effectively keeping Q1 cut-off.

231. When Q2 saturates both junctions are forward biased and the transistor has very low resistance. Heavy current flows, since nearly the entire supply voltage is dropped across the collector winding. This heavy current continues to flow until the core of transformer T1 saturates. When T1 saturates, the flux density of the core can no longer increase and the coupling between windings decreases. The positive feedback to the base of Q2 fails and its collector current can no longer be supported. This current falls rapidly and at the same time the feedback to the base of Q1 reverses to drive Q1 into saturation. Q2 is cut-off and the cycle of events repeats itself except that polarity of the current in the primary of T1 is now reversed. This action is regenerative and the current flow in the primary of T1 is essentially a square wave. Repetition rate is dependent upon the primary inductance of the transformer and upon the transistor characteristics. The frequency of this converter is approximately 4500 cycles.
Fig 28 - Block diagram of error correction in translator-synthesizer sub assembly
232. Several precautions must be taken in a circuit of this kind. Basic current must be limited to prevent transistor burn-out. Resistors R1 and R2 are provided for this function. Quite often spikes will appear across the emitter-collector of the transistor. Transient suppression must be provided for, since a spike should occur the allowable voltage across the non-conducting transistor might be exceeded. It can be shown that the base of the conducting transistor is at a potential of approximately 0.5V. In fact all three elements of the conducting transistor are so close to ground that their low impedance effectively short-circuit any transients in this circuit. In the case of the non-conducting transistor it can be shown that the base is at a potential of approximately twice the supply voltage plus the feedback voltage. Since any transients add to this voltage, it is possible to destroy this transistor, if no precautions are taken. Capacitors C1 and C2 are used as a storage device which absorbs the energy released when the transformer flux collapses during switching. Assurance that the oscillator will start under full load at low temperatures must be provided. Diodes A2CR1 and resistor A2R2 assure that the bases of the transistors will be driven positive by the full supply voltage when power is first applied. This starts oscillation rapidly. As soon as base current flows the diode clamps the base return to ground.

233. The 54 volts ac output from do-to-do converter switch Q1, Q2 is stepped down in transformer winding 1-5, filtered, and applied to pins 1 and 9 or connector J1. This stepped down voltage is the 6.3 volts as required for the filaments of amplifier tubes 1A12V1 (fig 1005) and 1A12V2 (fig 1006). The 54 volts ac is stepped up by transformer winding 5-12, full wave rectified by diodes A3C, through A3CR1, filtered and applied to pin 6 of connector J4. This voltage is the positive 125 volts dc output for the plates and screens of amplifier tubes 1A12V1 and 1A12V2. The 54 volts ac is stepped up by transformer winding 7-8, full wave rectified by diodes A3C, through A3CR5, regulated by 33 volt zener diode A3VR1 when SERVICE SELECTOR switch is at STANDBY, filtered, and applied to pin 14 of connector J1. This voltage will be nominally -30 volts dc but will vary +10% with like variations in the 27 volts dc plate voltage power input. This voltage is the -30 volts dc used to develop the A6G voltage used in RF amplifier module 1A142 during receive operation. During standby, this voltage will result in the full scale deflection of the front panel Signal level meter to allow the operator a means of ensuring that do-to-do converter module 1A11 is functioning. When the RF-662/3RC is tuning, this -35 volts dc is used to bias the RF amplifier tubes to cut-off to prevent over-dissipation in their screen circuits.

+20V Regulator Circuit

234. A stable voltage of +20 volts is used in most subassemblies. The circuit (top of fig 1024B) reduces the +27 vdc supply voltage and regulates it at +20 volts, this circuit regulates for both line and load changes.

235. The 27 volts dc is applied to the collector of transistor 1A1Q1 on the chassis (fig 1025) and is the effective collector-to-emitter resistance of transistor 1A1Q1. This voltage, derived from a constant 20 volts dc to 27 volts dc to 20 volts dc to the 27 volts dc power input. This voltage is the base voltage required by the external circuit. The value of the series resistance is determined by the rate of conduction of transistor 1A1Q1, which is controlled by the regulator circuit.

236. Differential amplifier A1Q3, A1Q4 compares the output from transistor 1A1Q1 with the reference established by 4.7 volt zener diode A1VR2. The output at the emitter of transistor 1A1Q1 is developed across the voltage divider consisting of resistors A1R7, A1R8, and A1R9. Assume that the 20 volts dc output of this transistor increases to 22 volts dc. The collector-emitter voltage, being the voltage difference between the collector and emitter of the transistor, increases. This causes the output voltage of A1Q1 to increase, and the output voltage of A1Q2 to increase. Therefore, the change in voltage at the collector of transistor A1Q1 will decrease, and the voltage on the collector of transistor A1Q2 will increase. The collector voltage of driver A1Q2 is the base bias for transistor 1A1Q1. Therefore, the decrease at the collector of driver A1Q2 causes transistor 1A1Q1 to conduct less. This increases the collector-to-emitter resistance to drop the voltage back to 20 volts dc. A similar sequence of events will occur if the 20 volts dc decreases. However, the reversal will occur in all the circuits in order to increase the conduction of transistor 1A1Q1, thereby decreasing the collector-to-emitter resistance to increase the voltage at the emitter of transistor 1A1Q1 to 20 volts dc.

237. Capacitor A1C5 provides filtering for the 20 volts dc output line. Capacitor A1C4 provides collector-to-base feedback for transistor 1A1Q1. Therefore, any ripple on the 20 volts dc output line will be fed back into the regulator circuit, and in turn to transistor 1A1Q1, 180 degrees out of phase with itself. This allows the ripple to be cancelled.
Capacitors C1, C2, and C3 provide high frequency filtering. If the 20 volts dc line becomes shorted, the resulting ground will forward bias diode A40R1. This will shut off dc amplifier A4Q2, which in turn shuts off driver A4Q1 and transistor 1A41A. When the short is removed, the regulator will recover and resume regulating action.

CHASSIS FRONT PANEL ASSEMBLY 1A4 (FIGS 1025, 1026 AND 1027)

Circuit Description

General

238. The front panel and chassis assembly 1A4 contains all the interconnections for the subassemblies, the code switches for intra-tuning (Receiver-Transmitter, Radio RT-662/GRC) and inter-unit tuning (Amplifier, Radio Frequency AM-3349/GRC-06), Noise Blanker sub-assembly 1A1A6, Internal ALC assembly 1A1A5, and all switches and controls for determining and controlling the various modes of operation in either the transmit or receive condition. The Noise Blanker and Internal ALC assemblies have been described previously.

Service Selector Switch (fig 1026)

General

239. The Service Selector Switch 54 is used to select the mode of operation for Radio Set AR/GRC-106.

240. The 27 volts dc applied to pins A and B of POWER connector J24 is applied through FUSE 2 AMP P4, diode OR1, and filter FL1 to contact 1 of switch 54, section 1, front. Diode OR1 is used to ensure correct polarity of the 27 volts dc applied to POWER connector J24. Zener diode VR2 will conduct when the voltage approaches 30 volts dc, increasing the current through FUSE P4 to ensure that it opens. Filter FL1 is a low pass readthrough filter, designed to suppress unwanted rf interference that may be present on the 27-volts dc input line. When the SERVICE SELECTOR switch is set at STANDBY, the 27 volts dc is applied through contacts 1 and 2 of switch 54, section 1, front to pin 3 of connector XA11, module A3. This voltage is then used in frequency standard module 1A5 to energize the oven assembly. When the SERVICE SELECTOR switch is set at STANDBY, the 27 volts dc is applied through contacts 1 and 3 of switch 54, section 1, front, to pin 7 of connector XA11, pin 26 of connector XA5, and to the STANDBY and OVEN ON circuits (XA5-A-3). This voltage is used in the 25-volt dc converter circuit. This voltage is also used in the STANDBY circuit and audio module 1A5 to energize the 25-volt dc converter circuit. When the SERVICE SELECTOR switch is set at STANDBY and OVEN ON circuits as previously explained and through contacts 1 and 4 of switch 54, section 1, front, to the following points:

a. Pin K of AUDIO connectors J18 and J19 for auxiliary use.

b. Pin 8 of connector XA11 to energize the 2-watt amplifier portion of receiver audio module 1A10.

c. Pin 3 of relay K2 and pin R3 of assembly A7.

d. Contact 6 of relay K2, from which it is applied through contact 8 (when motor B1 is de-energized) to pin 2 of relays K3 and K4, pin 4 of relay K1, the collector of transistor Q1, and pin 13 of connector XA11 to energize the 20-volt regulator circuit of dc-to-dc converter and regulator module 1A11.

e. Contact 5 of relay K2, from which motor B1 is energized through contact 2 of relay K2.
FIG 29 - KEYING RELAYS IN RT-662/GRC
241. **When the SERVICE SELECTOR switch is set at CW, -20 volts dc is applied through contacts 5 and 6 of switch S4, section 1, rear, to the BFO control, pin 10 of connector XA7, and pin 13 of connector XA5. The switched 20 volts dc is applied to receiver IF, module 147 to energize the BFO circuit. The switched 20 volts dc is applied to transmitter IF, and AUDIO module 145 to disable the microphone circuits and energize the 2-kc generator circuit.** When the SERVICE SELECTOR switch is set at SSB NSK, or AM, the output from the VOX switch is connected through contacts 10 and 11 of switch S4, section 1, rear to contact 10 of switch S4, section 3, front. When the SERVICE SELECTOR switch is set at CW or FSK, contacts 10 and 11 of switch S4, section 1, rear, are open to disable the VOX switch for CW or FSK operation.

242. When the SERVICE SELECTOR switch is set at STANDBY, the required standby ground for the AM-3349/GRC-106 is applied through contacts 9 and 5 of switch S4, section 2, front, and pin N of PA CONTROL CONNECTOR J30. When the SERVICE SELECTOR switch is set at any operate position (SSB NSK, CW, AM, FSK), the required operate ground for the AM-3349/GRC-106 is applied through contacts 9 and 10 of switch S4, section 2, front and pin P of CONTROL CONNECTOR J30.

243. When the SERVICE SELECTOR switch is set at SSB NSK, ground is applied through contacts 11 and 12 of switch S4, section 2, rear to the VOX switch S4. When the SERVICE SELECTOR switch is set at FSK, ground is applied through contacts 11 and 1 of switch S4, section 2, rear, to pin 5 of connector XA0 and pin 22 of connector XA5. This ground is used to disable the squelch circuit in receiver audio module 140 and to disable the VOX circuit in transmitter IF, and audio module 145. When the SERVICE SELECTOR switch is set at AM, the ground is applied to the VOX switch through contacts 11 and 2 of switch S4, section 2, rear, and to pin 5 of connector XA5, to energize the squelch intervention gate in transmitter IF, and audio module 145. When the SERVICE SELECTOR switch is set at CW, the ground is applied through contacts 11 and 1 to disable the squelch and VOX circuits as was the case during FSK operation, and through contacts 11 and 3 to pin 14 of connector XA5. This ground is used to energize the 2-kc amplifier in transmitter IF, and audio module 145.

244. Switch S4, section 3, front, is used in conjunction with the VOX switch. Switch S4, section 3, rear is used to select the correct tap of voltage divider R11, B5, B6, for applying the necessary AFO control voltage to transmitter IF, and audio module 145.

**Vox Switch S1 (fig 1027)**

245. The VOX Switch, in conjunction with the SERVICE SELECTOR switch, is used to select the method in which the ground will be applied to pin 27 of J1 in the transmitter IF and audio subassembly 145 to place the AM/GRC-106 into the transmit mode of operation. The VOX switch is operating during the SSB and AM modes of operation only. During CW and FSK modes of operation, the VOX switch is bypassed.

**Service Selector Switch Set at SSB NSK**

246. In this position of the selector switch pin 27-J1 (sub assembly 145 fig 1027) is connected to the push to talk switch on the H-33/PT or M-29/U. Ground is applied to pin F of AUDIO connectors J48 or J49 (fig 1026) each time the push to talk switch on the M-29/U or H-33/PT is depressed. This ground is applied to contact 8 of switch S4, section 3, front and it is also applied through contacts 8 and 6 of switch S4, rear, and contacts 10 and 11 of switch S4, section 1, rear, to contact 10 or switch S4, section 3, front. From contact 11 the ground is also applied to pin 29 of connector XA5 to turn off transmit-receive switch 1ASA29, (fig 1015) and turn on transmit-receive switch 1ASA3, placing ground on Transmit/Receive (T/R) line 3. In order to ensure that there is no hang time when the push to talk switch is released, the bias developed by voltage dividers 1ASA2R, 1ASA2R3, 1ASA2R4 is applied through pin 27 of connector XA5, contacts 3 and 4 of switch S4, front, diode DB5, contacts 10 and 11 of switch S4, section 1, rear, contact 10 or switch S4, section 3, front, and to pin 29 of connector XA5. Therefore, inverter 1ASA241 is turned back on as soon as the push-to-talk switch is released, turning off transmit-receive switch 1ASA3 and removing the bias from 1/3 line 3. This ensures that the ZT-662/GRC is placed into receive operation immediately after the push-to-talk switch is released, without any hang time.

247. **Push to Vox:** When the Vox switch is set at PUSH TO Vox, the ground for keying T/R line 3 is produced by the voice input at the AUDIO connectors when the push-to-talk switch on the M-29/U or H-33/PT is depressed. When the push-to-talk switch is depressed, ground is applied to pin F of AUDIO connector J48 or J49. (fig 1026) This ground is applied through contacts 8 and 9 of switch S4, section 3, front, contacts 5 and 3 of switch S4, front to pin 27 of connector XA5. Thus Vox detector 1ASA29 (fig 1015) is operative allowing the voice to key the AM/GRC-106. As long as the handset is held depressed, the hang time function, as explained previously, is present. If the push-to-talk switch is released, the hang time function is bypassed, immediately placing the AM/GRC-106 into receiver operation. The bias
on voltage divider \(1\text{A5A2EQ}3, 1\text{A5A2Eq}4\) is applied through pin 27 of connector X45 to contact 3 of switch S1, front, from which it is applied through diode Q6, contacts 10 and 6 of switch S1, rear, contacts 10 and 11 of switch S4, section 1, rear, contact 10 of switch S4, section 3, front to pin 29 of connector X45. Therefore, transmit-receive switch \(1\text{A5A2Q}1\) is turned on, which turns off transmit-receive switch \(1\text{A5Q}1\) and removes the ground from T/R line 3, thus bypassing the hang time function in a manner similar to the PUSH TO TALK position of switch S4.

248. VOX: When the switch is set at VOX, the ground for keying T/R line 3 is produced by the voice input present at AUDIO connector J18 and J19. Ground is applied via contact 9 of switch S4, section 2, front, from which it is applied through contacts 11 and 12 of switch S4, section 2, rear, and contacts 7 and 3 of switch S1, front, to pin 27 of connector X45. Therefore, the VOX circuit will be operative, permitting the voice to supply the ground to T/R line 3 and key the AN/GRC-106.

249. SERVICE SELECTOR switch set at P/SK: When the SERVICE SELECTOR switch is set at P/SK, the VOX switch is bypassed by opening contacts 8 and 9 of switch S4, section 3, front, and contacts 10 and 11 of switch S4, section 1, rear. The keying information is still applied to pin 9 of AUDIO connector J18 and J19. This information is then applied through contacts 8 and 10 of switch S4, section 3, front, to pin 29 of connector X45. Therefore, transmit-receive switch \(1\text{A5A2EQ}1\) (fig 1045) and transmit-receive switch \(1\text{A5Q}1\) will be turned off and on at the keying rate of the radio teletypewriter terminal equipment.

250. SERVICE SELECTOR switch set at AM: When the SERVICE SELECTOR switch is set at AM, the AN/GRC-106 is keyed in the same manner as SSB NSK for the PUSH TO TALK and VOX positions of the VOX switch. With VOX switch set at PUSH TO VOX, the keyline is applied through contacts 8 and 11 of switch S4, section 3, front, rather than 8 and 9 as is done in SSB NSK.

251. SERVICE SELECTOR switch set at CW: When the SERVICE SELECTOR switch is set at CW, the VOX switch is again disabled as it was in P/SK. However, the keying information is still applied to pin 9 of AUDIO connectors J18 and J19. This keying information is then applied through contacts 8 and 12 of switch S4, section 3, front, to pin 30 of connector X45, keying the VOX circuit.

Intra-Unit Tuning

252. The turret in RF amplifier module \(1\text{A12}\) (fig 1005, 100) which contains Mc strips for the tuned input and output circuits, and the switch in Mc synthesizer module \(1\text{A9}\), which contains crystals, capacitors and HS/LC information, are repositioned every time a change of \(\pm 25\) or more is made in the operating frequency (2 to 29 Mc). When either KS switch \(\text{KS}5\) or \(\text{KS}6\) is rotated, a ground is established on one contact of switch \(\text{KS}9\), front (fig 1025). This ground is mechanically coupled to switch \(\text{KS}9\), rear which in turn applies the ground to pin 7 of motor relay \(\text{K}2\). Since 27 volts dc is applied to pin 3 of relay \(\text{K}2\), the relay will be energized. This action removes the 27 volts dc from pin 12 of connector J1X41, the collector of transistor \(1\text{AAQ}1\), and relay \(\text{K}1\), \(\text{K}3\), and \(\text{K}4\). The removal of the 27 volts from pin 12 of connector J1X41 and transistor \(1\text{AAQ}1\) will in turn prevent a 20-volt dc output from dc-to-dc converter module \(1\text{A11}\). This renders the RF-662/GRC inoperative while tuning is in progress. When relay \(\text{K}2\) is energized, 27 volts dc is applied through contacts 5 and 2 of the Relay to one side of turret motor \(\text{B}1\). The other side of turret motor \(\text{B}1\) is grounded, therefore \(\text{B}1\) will rotate. The motor drives a gear train assembly, which rotates the synchro switch, the turret, and the rotors of switch S2. The rotation will continue until the notch in the switch rotor (in front) reaches the grounded contact. This removes the ground from pin 7 of relay \(\text{K}2\), de-energizing it. When relay \(\text{K}2\) is de-energized, the 27 volt dc is removed from motor \(\text{B}1\) and ground is applied through contacts 4 and 2. With ground on both sides, the motor is dynamically braked. The 27 volt dc is re-applied to all operating circuits when relay \(\text{K}2\) is de-energized.

253. Kelt-Renv No. 3 (T/R Line 3): During receive operation, T/R line 3 is open and grounded during transmit operation. When T/R line 3 is grounded, relays \(\text{K}1\), \(\text{K}3\), \(\text{K}4\), and \(\text{K}5\) are energized. The ground applied to T/R line 3 corresponds to system keying. This ground is applied as outlined in the following chart.
### Service Selector

<table>
<thead>
<tr>
<th>Switch Position</th>
<th>VOX Switch Position</th>
<th>Keyed By</th>
</tr>
</thead>
<tbody>
<tr>
<td>AM or SSB N5K</td>
<td>Push to Vox</td>
<td>Applied voice when the push-to-talk switch is depressed.</td>
</tr>
<tr>
<td>AM or SSB N5K</td>
<td>Vox</td>
<td>Applied voice.</td>
</tr>
<tr>
<td>AM or SSB N5K</td>
<td>Push to Talk</td>
<td>Push-to-talk switch.</td>
</tr>
<tr>
<td>CW</td>
<td>Disabled</td>
<td>CW key.</td>
</tr>
<tr>
<td>PSK</td>
<td>Disabled</td>
<td>Radioteletypewriter terminal equipment key.</td>
</tr>
</tbody>
</table>

a. Relays K3 and K4: Initially, relays K3 and K4 are de-energized (receive operation). Relay K3 on signal from RECEIVER IN connector J16 to RF amplifier module 1A12 through coupling capacitor A661G and contacts A3 and A2. When energized (transmit operation), relay K3 connects the RF output from translator module 1A6 to RF amplifier module 1A12 through contacts A3 and A2. Relay K4 (de-energized) connects the RF output from RF amplifier module 1A12 to translator module 1A6 through contacts A3 and A2. When energized (transmit operation), relay K4 connects the RF output from RF amplifier module 1A12 to RF DRIVE connector J21 through contacts A2 and A1, in parallel with internal ALC assembly 1A14.

b. Relay K5: During receive operation, relay K5 (de-energized), serves no function. When energized (transmit operation), relay K5 grounds the RF input from RECEIVER IN connector J16.

c. Relay K1: Relay K1 generates the Xmt-rev No.1 (T/R line 1) and Xmt-rev No.2 (T/R line 2) information. When relay K1 is de-energized (receive operation), T/R line 2 applies a ground (contacts 8 and 12 of relay K1) to all circuits not required for receiving, and T/R line 1 applies 20 volts dc (contacts 14 and 10 of relay K1) to all circuits required for receiving. When transmitting (relay K1 energized), T/R line 1 applies ground (contacts 13 and 10 of relay K1) to all circuits not required for transmitting, and T/R line 2 applies 20 volts dc (contacts 9 and 12 of relay K1) to all circuits required for transmitting.

### Coding of Inter-Unit Tuning

#### General

254. A second code is generated by switches A185 and A186. S5 is the 10's of megacycles switch and S6 is the unit megacycle switch.

255. The purpose of this second code is to position the tuning turret in the power amplifier (AM-3349/GRC-106). Thirty tuned circuits are positioned according to the frequency selection scheme. The encoding scheme places a pattern or "ground" or "no-ground" on five wires. The turret decoder then seeks the complementary code. When this condition is satisfied, the turret stops. The system is an open-seeking circuit.

256. Since each of the five interconnected lines between the encoder switch and the decoder switch has either a ground or is open, it can be said that it has either one of two states. A convenient way to designate the state of the wire is to use a ZERO (0) to indicate "open" or a ONE (1) to indicate "ground". Using this idea, a table showing the code for each of the 30 positions of the turret can be found in Table 5. Table 5 gives the code for each tuned circuit. This chart is useful in checking the pattern of "grounds" or "no-grounds" on the five wires if a bad encoder switch is suspected. The inter unit coding system is described in more detail in par 277 to 279.

#### Encoder-Decoder, Principles of Operation

257. The digital tuning scheme of the radio set requires the positioning of a turret in the Power Amplifier AM-3349/GRC-106. This turret connects the tuned circuits into the circuitry. To reduce the size of the connecting cable from the receiver-transmitter to the power amplifier, a five wire code system is used.
258. The purpose of the encoder-decoder system is to accurately position the turret which is carrying the tuned circuits. For any one band, a driver stage tuned circuit and an output stage tuned circuit are changed. The encoder places a pattern of "grounds" or "no grounds" on five interconnecting wires. The turret decoder then seeks the complementary pattern at which point it stops rotating. The system is an open-seeking system.

259. Since each of the five interconnecting lines, between encoder switch and decoder switch, has either a ground or is open, it can be said that it has either one of two states. A convenient way to designate the state of the wire is to use a ZERO (0) to indicate "open" and a ONE (1) to indicate "ground". Using this system table 5 can be arranged which shows all of the codes for each tuned circuit. This chart is useful to check the pattern of "ground" or "open" on the five wires if a faulty encoder switch is suspected.

<table>
<thead>
<tr>
<th>Freq (Mo)</th>
<th>Code Line 1</th>
<th>Code Line 2</th>
<th>Code Line 3</th>
<th>Code Line 4</th>
<th>Code Line 5</th>
<th>Turret Position</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.0 - 2.5</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>3.0 - 3.5</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>14 - 15</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>15 - 16</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>4</td>
</tr>
<tr>
<td>24 - 25</td>
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<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>5</td>
</tr>
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<td>25 - 26</td>
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<td>1</td>
<td>1</td>
<td>0</td>
<td>6</td>
</tr>
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</tr>
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<td>0</td>
<td>1</td>
<td>12</td>
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<td>0</td>
<td>0</td>
<td>0</td>
<td>13</td>
</tr>
<tr>
<td>27 - 28</td>
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<td>0</td>
<td>0</td>
<td>0</td>
<td>14</td>
</tr>
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<td>28 - 29</td>
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<td>6 - 7</td>
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<td>0</td>
<td>1</td>
<td>24</td>
</tr>
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<td>7 - 8</td>
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<td>1</td>
<td>1</td>
<td>0</td>
<td>25</td>
</tr>
<tr>
<td>12 - 13</td>
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<td>0</td>
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<td>1</td>
<td>1</td>
<td>26</td>
</tr>
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<td>13 - 14</td>
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<td>1</td>
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</tr>
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<td>10 - 11</td>
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<td>0</td>
<td>1</td>
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<td>11 - 12</td>
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<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>29</td>
</tr>
</tbody>
</table>

1 Represents ground
0 Represents open
260. To use this type of coding and to ensure a start path circuit, a master and image section are used in both the encoder switch and the decoder switch. The image section of the switch uses a code which is the exact opposite, to that of the master section. In this description, the section using the codes in Table 5 are the master section in the encoder switch, and the image in the decoder switch, an example of master-image codes used for some frequencies in the encoder are shown in Table 6 as a system of five contacts making either contact or no-contact with a master disc and an image disc. Fig 30 shows the master and image section for the encoder switch. Note that it is necessary to use two switches to cover codes in three decades. The diagram shows the image and master of the decoder switch which rotates with the turret when driven by the motor and gear system. The five contacts in the encoder switch connect to the corresponding contacts in the decoder switch and to no other points except the contact areas of their respective discs. The complete circuitry uses a relay to start the motor as illustrated in Fig 30.

**Table 6 - Master and Image Codes in the Encoder**

<table>
<thead>
<tr>
<th>MEGACYCLES</th>
<th>MASTER</th>
<th>IMAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.0 - 2.5</td>
<td>01040</td>
<td>10101</td>
</tr>
<tr>
<td>8.0 - 9.0</td>
<td>10101</td>
<td>01010</td>
</tr>
<tr>
<td>10.0 - 11.0</td>
<td>01001</td>
<td>10110</td>
</tr>
<tr>
<td>16.0 - 19.0</td>
<td>00010</td>
<td>11101</td>
</tr>
<tr>
<td>25.0 - 29.0</td>
<td>11100</td>
<td>00011</td>
</tr>
</tbody>
</table>

261. It is obvious that, if the motor is to start and rotate the turret, a path must exist through the two switches. If the MG frequency selection knob is rotated to a new position of the encoder, the motor drives the decoder switch to the complementary code of that in the encoder. This, then, is the situation when the decoder switch has found the "open" in the circuitry and has removed voltage from the motor.

262. To summarize, the encoder sets up a code on five wires representing a turret position. When this happens, the code in the decoder switch is no longer complementary to the code in the encoder. There now exists a path through the two switches. The motor turns until the decoder switch again finds the complementary code and the motor circuit is broken. Complementary means that the code on the master in the encoder is opposite to that on the master in the decoder. Likewise the code on the image in the encoder is opposite to the code on the image decoder.

263. When the encoder-decoder switches have been rotated to select a new code (change of frequency on MP-662/GRC) a single path normally exists through the switch system; at other times multiple paths exist; at still other code settings, a device path will exist which goes back and forth between the two switches. However, as long as the code is different in the two master-image systems, a path will always be present to complete the circuit through to the motor. The motor can then start to rotate the decoder switch until the complementary code is found to stop the motor (and the turret).

264. It should be noted that the codes as shown in Table 5 seem to have no logical order. Table 7 shows the codes again, this time slant lines have been drawn to show that the code order is such as to bring the zeros and the ones into groups. Furthermore, it shows that all the information is contained in the column for code line five. If the five pickup contacts are now arranged in a trailing fashion, the same information can be obtained from one track. This is easily checked out. The code, as read from right to left, for 2.0 - 2.5 Mc is 01010. Read in this order, line 5-4-3-2-1. This is the code as picked up on a contact for each line column. Now read the code opposite the five contacts as arranged in trailing fashion on line 5. The code again reads 01010. Imagine that the column of figures moves upward one position. The five trailing contacts are now reading 10100. Checking the code across for 3.0 - 3.5 Mc (second position) the code is (right to left) 10100.

255. This arrangement is used on the decoding end of the system as the code can be arranged around the edge of a metal switch plate. Refer to Fig 31, where this is illustrated. Since a master and an image disc are required, there are two discs, each with five trailing contacts. The third disc with 30 notches insures that the turret positions itself correctly. The encoding end of the system cannot be arranged this way, since in a digital system two controls are needed. One is needed for the 10's of megacycles and the second for the digits.
### TABLE 7 - INTERUNIT TUNING - ENCODER LOGIC

<table>
<thead>
<tr>
<th>Freq (Mc)</th>
<th>Code Line 1</th>
<th>Code Line 2</th>
<th>Code Line 3</th>
<th>Code Line 4</th>
<th>Code Line 5</th>
<th>Trailing Contacts</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.0 - 2.5</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>←5</td>
</tr>
<tr>
<td>3.0 - 3.5</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>←4</td>
</tr>
<tr>
<td>14 - 15</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>←3</td>
</tr>
<tr>
<td>15 - 16</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>←2</td>
</tr>
<tr>
<td>24 - 25</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>←1</td>
</tr>
<tr>
<td>25 - 26</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>16 - 17</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>17 - 18</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>2.5 - 3.0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>3.5 - 4.0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>18 - 19</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>19 - 20</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>26 - 27</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>27 - 28</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>28 - 29</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>29 - 30</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>30 - 31</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>4 - 5</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>4 - 6</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>5 - 6</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>6 - 7</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>7 - 8</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>12 - 13</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>13 - 14</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>10 - 11</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>11 - 12</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

1 Represents ground  
0 Represents open

It could be done with one control if the one switch had thirty positions.

266. The encoder switch in the receiver-transmitter, RT-652/1RC, uses two switches. The first switch (10's of megacycles) changes the pattern of ground and open for each of the three decades, 0-9, 10-19, and 20-29. Therefore, the first switch has only three positions, 0-1-2. The second switch reads out the digit megacycles and, therefore, rotates through ten positions, 0 through 9.

267. To cover those tuned circuits which are one half megacycle wide (500 kc), it is necessary to have a switch on the 100-KC knob, since this is the only control which can recognize the half megacycle point. In this case, the code on one wire is changed.
TO MOTOR RELAY

TO ENCODER

ALL 3 SECTIONS ROTATE TOGETHER

S1

S2

S3

30 TEETH EVENLY SPACED

FIG. 31 - DECODING SWITCH USED IN AN-3349/GRC 106
A ground is carried on this wire as the knob rotates from 0 through 4. When the knob reaches 5, the ground is removed and this condition holds from 5 through 9. This changes the 5 wire code which initiates the turret change at the half megacycle point.

268. The action of the complete system is such that any megacycle, from 02 through 29, set up on the first two digit switches on the front panel causes the power amplifier turret to rotate and connect the proper tuned circuits into the circuitry. Since some tuned circuits cover only a half megacycle, the third frequency setting knob (100 kc) assists in selecting these tuned circuits.

Circuit Description of the Encoder-Decoder

269. Fig 32 is the circuit of the encoder wiring used in HF 662/696. This diagram also contains information about the two switches which establish the code on the five code lines.

270. Switch 85 front has three positions. Each position determines the pattern of "ground" or "open" which will appear for each decade. For megacycles 2 through 9, this switch will be in the 0 position. It will move to the 1 position for megacycles 10 through 19 and to the 2 position for megacycles 20 through 29. The table on fig 32 supplies information showing which contacts will have a ground or an open condition. A portion of 85 rear is used. Information is also given showing which contacts are connected together for the three positions, 0-1-2.

271. Switch 86 is used to set up the second digit of megacycles. Each code line is switched to a contact on 85 front to pick up a ground or an open condition in order to satisfy the requirements for each individual code. A table for each code line is provided which shows the contact number for each digit, 0 through 9. It should be observed that all switches are set in the 0 digit position. If switch 86 is advanced from 0 to 1, the wiper connected to each code line moves past a contact, coming to rest on the second contact. In other words it skips over a contact each time it advances. Since the contacts on the left side of the switch are assigned to a code line and those on the right side to another code line, it becomes evident that the two switch wipers interchange their roles at a point half way through the rotation angle of the switch. 0 through 4 is covered by one wiper and 5 through 9 by the other wiper.

272. The right-hand side of 86 section 3 front is not used for the five wire coding. The right-hand side of 86 rear, 86 section 1 rear, and 87 rear are used to create a ground pulse, also 87 front is used for switching at half megacycle points and will be described later. The code used for the 2.0 to 2.5 Mc tuning is as follows:

<table>
<thead>
<tr>
<th>Line</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Code</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Switch 85, the 10-Mc switch will be in the 0 position and will display the digit 0 in the panel window.

273. Switch 86, the 1-Mc switch will be in the 2 position and will display the digit 2 in the panel window. The code for each line is traced out in the following manner:

Code line 1 connects to contact 13 of switch 86, section 3 front. Contact 13 is the wiper contact. In the chart for the code line 1, it is noted that the contact for digit 2 (2 megacycles) is 21. Tracing out the wiring from contact 21, the circuit goes to contact 7 of switch 85 front. Checking the chart for switch 85 (0 position), it is found that contact 7 is open and cannot place a ground on line 1. Therefore line 1 has a 0 code marking.

a. In a similar manner, line 2 connects to wiper contact 2 on switch 86, section 2 rear. The contact for digit 2 is 8. Contact 8 connects to contact 9 of switch 85 (0 position). In the chart for switch 85 front, it is shown that contact 9 connects to contact 10 which in turn connects to contact 3 of ground pulse switch 86, section 1 rear. Contact 3 connects to contact 7 and thence to ground. Line 2 therefore has a 1 code marking.

b. In like manner, line 3 can be traced as follows: Line 3 to wiper 15 of 86, section 2 rear. From 15 to contact 21 (2 megacycles) then to contact 12 of 85 front. Contact 12 is open, therefore line 1 has a 0 code marking.

c. Line 4 does not go to 85 front. Since this turret position covers only a half megacycle (2.0 to 2.5 Mc), the circuitry is not normal on line 4. Line 4 connects to wiper contact 2 on switch 86, section 2 front. The circuit goes from contact 2 to contact 8 (2 megacycles) and then to 85 rear, contact 9. Contact 9
connects to contact 8 through the wiper. From contact 8 the circuit is to contact 3 of switch 87 front. Switch 87 is the 100 KC switch and is the only switch which can recognize the upper megacycle point. For the digits 6 through 4 contact 3 connects to contact 10 and thence to ground. Line 4 has a code marking of 1.

d. Line 5 connects to wiper contact 15 of switch 86, section 2 front. 15 connects to 21 (21 megacycles) and 21 connects to contact 5 of 85 front. 6 of 85 connects to 7 and 8 but is not grounded. Code line 5 is marked 0.

274. The tuned circuit switched into use by the above code will be used from 2 megacycles through 2.499 megacycles. At this point a new tuned circuit is required. This new tuned circuit covers 2.5 megacycles through 2.999 megacycles. The code for 2.5 to 2.499 megacycles, as previously indicated, is 0101. The code for 2.5 megacycles through 2.999 megacycles is 0100.

2.000 to 2.499 Mc 0101
2.500 to 2.999 Mc 0100

275. Examination of the two codes above shows that they differ only on line 4. If the ground on line 4 (2.000 to 2.499 megacycles) can be removed, the code for 100 to 2.999 megacycles will be set up and the turret in the power amplifier will rotate and thus set up the new tuned circuit. This is exactly the purpose of switch 87 front on the 100-kc knob. For the digit positions 0-4, contact 3 connects to contact 10 which is grounded. As the wiper turns, contact 3 will be disconnected from contact 10 when the digit position 5 is reached. For positions 5 through 9, 3 will be connected to contact 5. This removes the ground formerly supplied through contact 10. When contact 3 connects to contact 5, line 4 is connected to all the other open lines, namely lines 1, 2, 3 and 5. This is necessary in order to maintain the circuit connections for the system.

276. It should be noted that there is one more pair of tuned circuits that is handled in the above manner. The tuning for 3 to 4 megacycles is split into two tuned circuits. The first tuned circuit covers 3 to 3.499 megacycles and the second tuned circuit covers 3.5 to 3.999 megacycles.

The codes for these two circuits are as follows:

3.000 to 3.499 Mc 0010
3.500 to 3.999 Mc 0010

Inspection of the above codes indicates that line 5 is the line that must have the ground removed.

277. Both of these cases discussed above were in the decade 6 through 9 megacycles. Since this special condition does not occur in the decades 10 to 19 and 20 to 29, switch 85 rear is used to disconnect the 100-kc switch 87 front, whenever these decades are in use. Contact 8 on switch 85 rear is opened and contact 9 is grounded through contact 10. For all other tuning positions, the 100-kc switch is not used and switch 85, front and rear, is used to establish the pattern or "ground" or "open".

278. Since a change of 100 kc or more will require that the operator return the power amplifier, a ground pulse is generated which will automatically put the radio set in the tune position. This, then, requires that the 10-Mc, the 1-Mc, and the 100-Mc knob generate a ground pulse if they are turned one position or more.

279. a. For the 10-Mc knob, switch 85 rear is used. Whenever this switch is moved from one position to another a contact on the wiper will momentarily connect contact 5 to contact 6. The ground at contact 7 or switch 86 section 4 rear can be followed to contact 3 and thence to contact 5 of 85 rear. Contact 6 makes momentary contact on 5. Contact 5 connects to the ground pulse line to pin H of J20. From pin H of J20 the ground pulse is delivered to the power amplifier circuitry.

b. For the 1-Mc knob, switch 86, section 1 rear is used. Each time this switch is moved one position a wiper contact momentarily makes contact with 4. Contact 4 connects to the ground pulse line.

c. When the 100 KC knob is moved one position or more, switch 87 rear is used. The wiper contacts on this switch connect contact 8 to either contact 7 or contact 9 to momentarily produce a ground pulse. Contact 8 is also connected to the ground pulse line.
### S5 Front
- **0 Position**
  - Digit 0
  - Contacts 1-2-12 Open
  - Contacts 3-4-5 Gnd
  - Contacts 6-7-8 Open
  - Contacts 9-10 Gnd

### S5 Rear
- **0 Position**
  - Contacts 8-9 Connected

### 1 Position
- **Digit 1**
  - Contacts 1-2-3 Open
  - Contacts 4-5-6 Gnd
  - Contacts 7-8-9 Open
  - Contacts 10-12 Gnd

### 2 Position
- **Digit 2**
  - Contacts 2-3-4 Open
  - Contacts 5-6-7 Gnd
  - Contacts 9-10 Gnd
  - Contacts 1-8-12 Open

<table>
<thead>
<tr>
<th>Code Line #1</th>
<th>Code Line #3</th>
<th>Code Line #4</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>S6 Section 3 Front</strong></td>
<td><strong>S6 Section 2 Rear</strong></td>
<td><strong>S6 Section 2 Front</strong></td>
</tr>
<tr>
<td>Digit 0 Contact 17</td>
<td>Digit 0 Contact 17</td>
<td>Digit 0 Contact 4</td>
</tr>
<tr>
<td>Digit 1 Contact 19</td>
<td>Digit 1 Contact 19</td>
<td>Digit 1 Contact 6</td>
</tr>
<tr>
<td>Digit 2 Contact 21</td>
<td>Digit 2 Contact 21</td>
<td>Digit 2 Contact 8</td>
</tr>
<tr>
<td>Digit 3 Contact 23</td>
<td>Digit 3 Contact 23</td>
<td>Digit 3 Contact 10</td>
</tr>
<tr>
<td>Digit 4 Contact 1</td>
<td>Digit 4 Contact 1</td>
<td>Digit 4 Contact 12</td>
</tr>
<tr>
<td>Digit 5 Contact 14</td>
<td>Digit 5 Contact 14</td>
<td>Digit 5 Contact 3</td>
</tr>
<tr>
<td>Digit 6 Contact 16</td>
<td>Digit 6 Contact 16</td>
<td>Digit 6 Contact 5</td>
</tr>
<tr>
<td>Digit 7 Contact 18</td>
<td>Digit 7 Contact 18</td>
<td>Digit 7 Contact 7</td>
</tr>
<tr>
<td>Digit 8 Contact 20</td>
<td>Digit 8 Contact 20</td>
<td>Digit 8 Contact 9</td>
</tr>
<tr>
<td>Digit 9 Contact 22</td>
<td>Digit 9 Contact 22</td>
<td>Digit 9 Contact 11</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Code Line #2</th>
<th>Code Line #4</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>S6 Section 2 Rear</strong></td>
<td><strong>S6 Section 2 Front</strong></td>
</tr>
<tr>
<td>Digit 0 Contact 4</td>
<td>Digit 0 Contact 4</td>
</tr>
<tr>
<td>Digit 1 Contact 6</td>
<td>Digit 1 Contact 6</td>
</tr>
<tr>
<td>Digit 2 Contact 8</td>
<td>Digit 2 Contact 8</td>
</tr>
<tr>
<td>Digit 3 Contact 10</td>
<td>Digit 3 Contact 10</td>
</tr>
<tr>
<td>Digit 4 Contact 12</td>
<td>Digit 4 Contact 12</td>
</tr>
<tr>
<td>Digit 5 Contact 3</td>
<td>Digit 5 Contact 3</td>
</tr>
<tr>
<td>Digit 6 Contact 5</td>
<td>Digit 6 Contact 5</td>
</tr>
<tr>
<td>Digit 7 Contact 7</td>
<td>Digit 7 Contact 7</td>
</tr>
<tr>
<td>Digit 8 Contact 9</td>
<td>Digit 8 Contact 9</td>
</tr>
<tr>
<td>Digit 9 Contact 11</td>
<td>Digit 9 Contact 11</td>
</tr>
</tbody>
</table>

*Issue 1, 31 May 67*
Code Line #5

Section 2 Front

git 0 Contact 17
git 1 Contact 19
git 2 Contact 21
git 3 Contact 23
git 4 Contact 1
git 5 Contact 14
git 6 Contact 16
git 7 Contact 18
git 8 Contact 20
git 9 Contact 22

FIG 32 - ENCODER SWITCH MIXING USED IN RT 662/GRC
Circuit Description of the Do-to-Ao Inverter (Fig 1028)

280. The Do-to-Ao inverter produces 6.3 VAC, 128 VAC, and -130 VDC. The 6.3 VAC is the filament voltage for the driver tube. 128 VAC is provided for two blower motors and the -130 VDC is used for bias on the two vacuum tubes in the power amplifier.

281. The do-to-ac inverter assembly utilizes a saturable-core transformer oscillator circuit to develop a square-wave output from the 27-volts dc input. When Receiver-Transmitter, Radio FT-562/GRC SERVICE SELECTOR switch is at STD, BY or any operating mode (AM, CW, WSP, SSB only) and Amplifier, Radio Frequency AM-3545/GRC-100 FMR, circuit breaker is at ON, 27 volts dc is available at pins 3 and 4 of connector P1. This 27 volts dc is applied to pin 4 of transformer T1 and through current-limiting resistor R1 to pin 1 of transformer T1. From pin 1, 27 volts dc is applied through primary winding 1-2 to the collector of switch Q1 and through primary winding 4-5 to the collector of switch Q2. From pin 1, 27 volts dc is applied through feedback winding 1-2 and current-limiting resistor R2 to the base of switch Q1 and through feedback winding 1-6 and current-limiting resistor R3 to the base of switch Q2. These applications are simultaneous, and both transistors will be forward biased. However, due to the inherent differences in components and circuit unbalance, one transistor will start conducting first.

282. Assume switch Q1 starts conducting, the voltage at pin 3 of transformer T1 will begin to decrease. This will induce a voltage across winding 4-5 with pin 4 positive and pin 3 negative. This will create a field through the transformer core with the same polarity. The voltage induced across winding 4-5 by this decrease is of the same polarity as the induced by the collapsing field. Therefore, a new field is developed around the transformer core with the same polarity. Since pin 4 of transformer T1 is referenced to ground through diode CR1, the level at pin 2 will continue to decrease, holding switch Q1 cut off. At this point, the field around the core collapses. This will induce voltages in the primary and feedback windings of opposite polarity to that just described. Therefore, the level at pin 2 will decrease and the level at pin 6 will increase. When the level at pin 2 decreases, switch Q1 is cut off. When the level at pin 6 increases, switch Q2 is forward biased and starts conducting. When switch Q2 starts conducting, the level at pin 5 decreases. The voltage induced across winding 4-5 by this decrease is of the same polarity as that induced by the collapsing field. Therefore, a new field is developed around the transformer core with the same polarity. Since pin 4 of transformer T1 is referenced to ground through diode CR2, the level at pin 2 will continue to decrease, holding switch Q1 cut off, and the level at pin 6 will continue to increase, driving switch Q2 toward saturation. When switch Q2 reaches saturation, the voltage induced across winding 4-5 will stabilize. This condition (Q1, cut off; Q2, saturated) will continue until the core is again saturated. At this time, the field will collapse. Switch Q1 will be driven to saturation and switch Q2 will be cut off. The oscillations caused by this process produce a square-wave output. The frequency of the ac output, which is determined by the saturation time of the transformer core, is approximately 400 c/s. Any transients or spikes produced at the collector of either switch by the instantaneous transfer from cut off to saturation are applied through either diode CR2 or CR3 to the driver diode D1. If these peaks exceed 68 volts, the driver diode D1 will fire, shutting the peaks to ground.

283. There are three outputs from the do-to-ac inverter assembly: 6.3 volts ac, 128 volts ac, and -130 volts dc. The 6.3 volts ac, 400 c/s driver amplifier 2A8V filament supply is developed across winding 7-8 and applied to pins 5 and 6 of connector P1. The voltage developed across winding 9-13 is applied across bridge rectifier CR4, CR5, CR6 and CR7. The -100-volts dc output from the bridge rectifier is applied to pin 13 of connector P1 to be used as the bias supply for power amplifier tubes 2A1AV1 and 2A1AV2. The voltage developed across winding 9-13 is also applied to pins 1 and 2 of pins 1 and 2 of connector P1. From pins 1 and 2, the 128 volts ac 400 c/s, is applied to the internal blower motor on the main frame lernin. Pin 9 of connector P1 is connected to one side of the external blower motor on the case. Winding 9-13 is tapped, and this line is applied to pin 11 of connector P1. Pins 10 and 11 of connector P1 are connected to thermostat 2A681. Thermostat 2A681 is connected to one side of the external blower motor. While the temperature in the case is below 75°C, the voltage between pins 9 and 11 of connector P1 is applied to the external blower motor. If the temperature in the case exceeds 75°C, the 128 volts ac between pins 9 and 10 of connector P1 is applied to the external blower motor, which will increase its speed to provide more air flow. Pins 7 and 9 of connector P1 are jumpered to provide an interlock so that if the blower inverter is disconnected, the ground path to
standby relay 2A5AE1 is broken. Therefore, no power can be applied to the power amplifier tube filament, the DC-to-DC converter, and the protection circuits.

Circuit Description of the Do-to-Do Converter (fig 1028)

284. The DC-to-DC converter produces two outputs. The 500 VDC output is used for the screen grid and plate voltage on the driver stage and for the screen grids of the output stages. The 2400 VDC output supplies the plate circuit of the output stage. This converter uses an extra transformer in the feedback loop. With large load currents it is undesirable to saturate the output transformer. This prevents the formation of spikes in the collector circuits of the switch transistors. The full load collector current wave shape is still a square wave but does not produce any appreciable spikes. Therefore, a saturable core transformer is used at low power in the feedback loop. The efficiency is also greatly improved by this method of operation, since the loss due to heat is less.

285. The 27 volts dc at contact 4 of relay 2AK2 (P/O 2A5A2) is applied through contact 2 to charge capacitor 6A61 while relay 2AK2 is de-energized. When the radio is keyed, the keyline ground is applied to pin N of CONTROL connector J2, through contacts 5 and 1 of relay 3AK3, the relay will energize. When relay 2AK2 is energized, the converter feedback path is completed through contacts 1 and 6 of relay 2AK2 and capacitor 6A61 discharges through contacts 2 and 5 of the relay, the parallel combination of resistor 6A62 and resistor 2AK2, and the base-emitter junction of switch 3A64. There are 27 volts dc applied to the collector of switch 3A64, therefore, when capacitor 6A61 discharges, switch 3A64 is forward biased and conducts. The conduction of switch 3A64 causes current flow through resistor 2AK3 and the base-emitter junction of switch 2AK2. Since there is 27 volts dc applied to the collector of switch 3A64, the base circuit starts a flow of collector current. When switch 2AK2 is conducting, the level at pin 3 of transformer 2AK1 will decrease. This will induce a voltage across winding 2-3, which results in a voltage being induced across winding 4-10 of transformer 2A71. This voltage is applied across pins 4 and 3 of transformer 2A72 through contacts 1 and 6 of relay 2AK2 (energized). The field developed as a result of this voltage induces a voltage across the secondary of transformer 2A72 such that pin 4 is positive and pin 5 is negative. The positive level at pin 4 is applied to the base of switch 2A22, which drives switch 2A22 into saturation. The negative level at pin 5 holds switch 2Q1 cut off. When switch 2A22 reaches saturation, the voltage induced in the various windings stabilizes until the core of transformer 2A72 is saturated. At this time, the field around transformer 2A72 collapses, the polarity at pins 4 and 5 reverse, switch 2A22 is cut off, switch 2Q1 is driven into saturation, and the process is repeated in essentially the same way as described for the do-to-do inverter assembly with one exception. Transformer 2A71 does not saturate. 2A72 in the feedback loop performs this function. This is done to improve efficiency and to prevent the formation of transients across the "off" transistor. The frequency of oscillation of this converter is approximately 1200 c/s.

286. There are three outputs from transformer 2A71. The output across winding 2-10 is the feedback signal applied to transformer 2A72. The output across winding 6-7 is rectified by bridge rectifier 2A92, 2A93, 2A94 and 2A95. The resulting 500 volts dc is applied to plate of conector J1 to be used as the plate and screen grid supply for driver amplifier 2A6V1 and the screen grid supply for power amplifiers 2A1AV1 and 2A1AV2. A representative portion of this voltage is applied to the front panel TEST METER circuit. The signal across winding 11-8 is rectified by bridge rectifier unit 2A96, and the resulting 2400 volts dc is applied to pin 3 of connector J1 to be used as the plate supply for power amplifier tubes 2A1AV1 and 2A1AV2. A representative portion of this voltage is applied to the front panel TEST METER circuit. The power amplifier plate current flows through resistor 2A5R1, and the resultant voltage drop is applied to the front panel TEST METER circuit to provide an indication of power amplifier plate current.

287. When the At/GEO-106 is keyed, the feedback path through contacts 1 and 6 of relay 2AK2 is broken, and the oscillations stop. At this time, 27 volts dc is applied through contacts 4 and 2 of relay 2AK2 to capacitor 6A61. Capacitor 6A61 will recharge to the supply voltage, and when the At/GEO-106 is keyed again, the process described above is repeated.

Over-Current and Under-Voltage Protection Circuit (fig 1028)

General

288. The DC-to-DC converter is provided with an over-current protection circuit which will turn off the converter whenever the power amplifier tubes draw plate current in excess of approximately 500 milliamperes for approximately 40 milliseconds. An under-voltage protection circuit is also provided. This assures that the switch transistors Q1 and Q2 cannot operate below the saturated condition.
Over-Current Protection

289. When the radio set is keyed, the ground keyline is applied through contacts 5 and 1 of relay 53 (de-energized) to pin 3 of relay 282 to start the de-to-de converter. If power amplifier 2A1V1-2A1V2 draws excess plate current, relay 53, which is in the plate current return path, will be energized. When relay 53 is energized, the 20-volt dc output from regulator 5V1 is applied through contacts 2 and 3 of the relay and feed-through capacitor 205 to the RC combination of resistor 207 and capacitor 204. The time constant of the RC combination is such that after approximately 40 milliseconds, the charge on capacitor 204 will exceed 10 volts dc. This will cause zener diode 208 to conduct. When zener diode 208 conducts, current flows through resistor 205. This potential is applied to silicon-controlled rectifier 7Q2 to trigger it. Since the coil of relay 53 is part of the conduction path for SCR 7Q2, when the positive potential is applied to SCR 7Q2 and the SCR conducts, relay 53 is energized. When relay 53 is energized, the ground keyline to relay 282 (above) is broken, which de-energizes relay 282. When relay 282 is de-energized, the feedback path from transformer 272 to transformer 272 is opened, which turns off the de-to-de converter assembly. This condition will continue until the TUNE-OPERATE switch 586 is moved from one position to the other. It also breaks the +27 VDC to silicon-controlled rectifier 7Q2. This turns off 7Q2 thus de-energizing relay 53 and the ground keyline circuit is again completed to relay 282. When switch 586 is operated contacts 6 and 11 are broken to break the 27 VDC line to SCR 7Q2.

Under Voltage Protection (fig 1028)

290. While the de-to-de converter assembly is turned off, there is no feedback voltage at pins 1 and 3 of transformer 272, there is no signal applied to the cathode of zener diode 7V2, and the zener diode 7V201 is held essentially at ground through contacts 6 and 8 of relay 282 and winding 2-3 of transformer 272. When the AM/SSC-106 is keyed, the de-to-de converter assembly is turned on. The feedback signal is detected by diodes 532 and 532, and the resultant output is applied through isolating resistor 531 and feed-through capacitor 530 to the cathode of zener diode 7V201. Under normal operation, the level at the cathode of zener diode 7V201 is of sufficient amplitude to operate zener diode 7V201 (within approximately 50 milliseconds from the time the de-to-de converter is keyed). This will supply enough current through the base-emitter junction of transistor 7Q1 to keep switch 7Q1 in a conducting state. However, since the coil of relay 7Q2 is in the conduction path for switch 7Q1, when switch 7Q1 is saturated, relay 7Q2 is energized. This condition will continue as long as the operation of the de-to-de converter assembly is normal.

291. When the radio set is keyed and the de-to-de converter assembly is turned on, the ground at the junction of resistors 7R1 and 7R2 is removed (contacts 6 and 8 of relay 282 opened). The 20-volt output from regulator 5V1 is then applied to the RC combination of resistors 7R1 and 7R2 and capacitor 7C1. The time constant for the RC combination is such that after 150 ms, the charge on capacitor 7C1 will reach 10 volts. This will cause zener diode 7V201 to conduct. However, as long as relay 53 is energized, there is no conduction path for zener diode 7V201.

292. If the output voltage from the de-to-de converter assembly should decrease, the feedback voltage will also decrease. If the voltage at capacitor 7C1 drops below approximately 10 volts, zener diode 7V201 will stop conducting. Therefore, the base to emitter junction of switch 7Q1 will be reverse biased and stop conducting. Diode 7C1 in the emitter circuit of switch 7Q1 provides reverse biasing to hold switch 7Q1 non-conducting when zener diode 7V201 is not conducting. At this time, relay 7Q2 is de-energized, and the conduction path is provided for zener diode 7V201 through feed-through capacitor 7C1, contacts 4 and 5 of relay 7Q2, feed-through capacitor 7C1, inductor 7L1, and resistor 7R8. This triggers SCR 7Q2 and the de-to-de converter assembly is turned off as described previously. Normal operation can be resumed after the faulty condition is repaired, by operation of the TUNE-OPERATE switch 586.

POWER CONTROL CIRCUITS (FIG 1028)

Initial Voltage Application

293. Twenty-seven-volt dc primary voltage for the AM-3342/GO-106 is applied to pins A and B of FMU POWER connector 557. When FMU POWER circuit breaker 542CR1 is set at ON, the 27 volts dc is applied through polarity diode 542CR1 to pin 4 and contact 3 of standby relay 5A2X1. Relay 5A2X1 is not energized until a ground is applied to pin 1. The ground necessary for energizing relay 5A2X1 is generated by the SERVICE SELECTOR switch on the RF-1062/GRO. (Fig 1028) When the SERVICE SELECTOR switch on the RF-1062/GRO is set at BAND BY or any operate (CW, AM, FM, or SSTN SRC) position, switch 54 section 2, front, connects a
ground through feed-through capacitor A524 and L-section filter A1A121-A1A124 to pin N of PA CONTROL connector A1 29, which is connected to pin N of CONTROL connector A522 through Cable Assembly, Special Purpose, Electrical CX-1009/0. Pin N of CONTROL connector A532 connects the ground through L-section filter A5A1A207-A5A1A217, feed-through capacitor A5A1A14, pin 21 of connectors A5J1 and A1X45, pin 8 of connectors A5J1 and A1X4A1, pin 8 of connectors A5J1 and A5A1P1, pin 7 of connectors A5P1 and A5J1, pin 7 of connector A5A1X and A5J1, pin 4 of connectors A1X2A5 and A5J1, and thermostat A5B3, which will be closed at this time, to pin 1 of relay A5A2X1. If the equipment is over-heated, A5J1 will open, de-energizing relay A5A2X1 and removing the 27 volts dc.

Standby Voltage Distribution

294. When ground is applied to pin 1 of relay A5A2X1, with the 27 volts dc on pin 4, relay A5A2X1 will energize and apply the 27 volts dc through contacts 3 and 2 to the following points: pins 3, 4, and 5 of connector A5J1, contact 4 of relay A5A2X2, voltage regulator A5A5VR1, collector of switch A5A6Q1, contact C6 of TUNE-OPERATE switch S6, and to pin 3 of relay A5A2X2. Also at this time, 27 volts dc is applied from contact 3 of relay A5A2X1 to pin 2 of transformer A5A2X1.

a. From pins 3 and 4 of connector A5J1, the 27 volts dc is applied through pins 3 and 4 of connector A1X2A5, pin 3 of connector A5A6Q1, and A5A6Q2. These two applications start the switching action in the dc-to-ac inverter assembly.

b. From pin 5 of connector A5J1, the 27 volts dc is applied through pin 5 of connector A1X2A5 to the following points: power amplifier A1A1V1-A1A1V2 Filaments, collectors of emitter followers A1A1Q1 and A1A1Q2, pin 3 of connector A1A1X8, and pin 6 of connector A1A1X7.

1. The 27 volts dc is the filament voltage for power amplifier A1A1V1-A1A1V2. It is applied to pin 7 of A1A1V1 and to pin 3 of A1A1V2. Capacitors A1C16 and A1C17 provide filtering.

2. The 27 volts dc is applied to emitter follower A1A1Q1 and A1A1Q2 to be used as operating voltage. These emitter followers are the output circuit for tube level control signal and the TEST NETHER grid drive indication.

3. The 27 volts dc at pin 3 of connector A1A1X8 is applied through pin 3 of connector A5J1 and resistors A5A5R7, A5A5R5, and A5A5R6 to grid circuit of driver amplifier A5V1. This is the grid bias for driver amplifier A5V1, which is regulated by zener diode A5A5VR1 and adjusted by A5A5R6.

c. The 27 volts dc applied to resistor A5A5R2 in the regulator A5A5VR1 circuit, contact C6 of TUNE-OPERATE switch S6, pin 3 of relay A5A2X2, (collector of A5A6Q1 operating voltage for the dc-to-dc converter assembly protection circuits).

Operate Voltage Distribution

295. The 27 volt standby supply is used to develop the 27-volt operate supply and is used in conjunction with it throughout the equipment as described below.

a. The standby 27-volts dc at pin 6 of connector A1A1X7 is applied through pin 6 of connector A1J1 to contacts X1 and A2 of time delay relay A7K1, contact 1 of operate relay A7K5, contact 1 of capacitor motor relay A7K1, pin 7 of zone locking relay A7K6, contact 1 of circuit motor relay A7K2, contact 1 of bandswitch motor relay A7K3. After a 60-second delay, contact A2 of time delay relay A7K4 will close with contact A1, and the 27 volts dc is applied to pin 7 of operate relay A7K5. In any operate position (A1, PSK, OW, SSB PSK), SERVICE-SELECTOR switch (fig 1026) A1S1 section 2, front, on the RF-662/38G apply a ground through contacts 9 and 10, feed-through capacitor A1C123; L-section filter A1A1L2-A1A1L5, pin P of PA CONTROL connector, Cable Assembly, Special Purpose, Electrical CX-1009/0, pin P of CONTROL connector A5J2, L-section filter A5A1O2-A5A1O5, feed-through capacitor A5A1O11, pin 15 of connectors A5J1 and A1X2A5, and pin 10 of connectors A1A1X7 and A1X2A5 to pin 3 of relay A7K5. Therefore, as soon as the time delay is over, relay A7K5 is energized. When relay A7K5 is energized, the standby 27 volts dc at contact 1 is applied through contact 6 to pin 15 of connectors A7J1 and
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ENGINEERING INSTRUCTIONS (AUS)

A1A1X7, contacts 2 and 4 of relay A7X6 and pin 6 of A1A1X7, and pin 11 of connectors A1X05 and A5G1 to pin 7 of relay A5A2X2 and pin 1 of relay A5K1 (Antenna Switching) to be used as the operate 27 volts dc. With 27 volts dc on pin 7 of A5A2X2 at any time ground is applied to pin 3 of relay A7K5, the relay will be energized, breaking the operate 27-volt line during tuning. When turret motor relay A7K1 is energized, the 27 volts dc at contact 1 is applied through contact 6, pin 4 of connectors A1J4 and A1A1X7, and pin 1 of connectors A1X22 and A2J1 to energize turret motor A2J2. When capstain motor relay A7K2 is energized, the 27 volts dc at contact 6, pin 4 of connectors A7J1 and A1A1X7, pin 14 of A1X3 and A3J1, and feed-through capacitor A3C14 to energize capstain coding motor A3M1. When bandswitch motor relay A7K3 is energized, the 27 volts dc at contact 1 is applied through contact 6, pin 3 of connectors A7J1 and A1A1X7, pin 22 of connectors A1X5 and A3J1, and feed-through capacitor A3C22 to energize bandswitch motor A3B2.

b. When the equipment is in standby, 27 volts dc is applied through contacts 4 and 2 of relay A5A2K2 to charge up capacitor A5A6C1. At the same time, 27 volts dc is applied to the collector of switch A5A6A1. As long as the equipment is unkeyed, this condition remains static. When the equipment is in an operating condition, 27 volts dc is applied from pin 11 of connectors A1X05 and A5G1 to pin L1 of relay A5K1 and pin 7 of relay A5A2X2. When the equipment is keyed, ground is applied to pin L2 of relay A5K1, which will be energized to connect RF output line to the antenna in use. This ground is also applied through contacts 5 and 1 of relay A5A3K3 to pin 3 of relay A5A2X2. When relay A5A2X2 is energized, capacitor A5A6C1 will discharge through contacts 5 and 2 to the base of switch A5A6A1. Switch A5A6A1 is driven into saturation, and the pulse is applied to the base of A5A2Q2 in the do-to-do converter assembly. Since 27 volts dc is available from pin 3 of transformer A5A2T1, A5A2X2 will start the do-to-do converter switching action.

c. The operate 27 volts dc applied to dropping resistor A5A5R2 is applied to pin 1 of TEST METER switch A5S2. When TEST METER switch A5S2 is set at PRIM VOLT, the 27 volts dc is applied to TEST METER M4 to provide an indication of the level of the operate 27 volts dc.

LEVEL CONTROL SIGNAL CIRCUITS (Fig 1028)

General

296. The purpose of the level control signal circuits is to maintain the output from the Power Amplifier at a nominal value of 400 watts PEP. The OPERATE level controls the output during normal operation. The TUNE level controls signal functions during tuning at which time a reduced level signal is required.

297. Fig 33 provides, in block form, the method used to secure automatic control of the power amplifier output. This block diagram shows the circuitry contained in the power amplifier and indicates the path of the signal in the control loop. The control loop includes portions of the receiver-transmitter RF-662.

Operate Level Control Signal

298. The output from the AH-3349/GRC-106 is sampled and detected to provide a dc signal to Receiver-Transmitter, Radio RF-662/GRC to control the output from RF-662/GRC. The output from power amplifier 2A1A1W1, 2A1A1W2 is applied through the tune discriminator and the load discriminator to connector 2A1A3P1, from which it is applied through connectors 2A1A3J1, 2A1A3P3, and 2A1A3Q2 to the impedance matching networks in antenna coupler assembly 2A3.

299. The power on the 50-ohm line is sampled across capacitive divider A3G1, A3G2. This sampled voltage is detected by diode A3C1, filtered by capacitor A3C5, and used to drive emitter follower A3Q1. The output from emitter follower A3Q1 is applied through connectors 2A1A3R1-A, 2A1A3R2-A, 2A1A3X-A3, 2A5A2Q3-A3, feed through capacitor A5A10Q3, and pi-section filter to pin 6 of CONTROL connector A5C7 for connection to the RF-662/GRC.

300. When the TUNE-OPERATE switch A5S6 is set to OPERATE, the tune level control signal output is grounded through contacts 7 and C4.

301. The output from emitter follower A1A1Q1 is directly proportional to the peak RF envelope output from the peak RF envelope output from the power amplifier. This control signal is applied to the pi-section to pin 6 of CONTROL connector A5S2, which is connected to pin 6 of PA CONTROL connector A1J20 on the RF-662/GRC through Cable Assembly Special Purpose, Electrical GXX-10095-U. Pin 6 of PA CONTROL connector A1J20 applies the level
control signal through L-section filter 1A12C, 1A13L2 (fig 1026) and feedthrough capacitor A1C25 to FPC control A1R5 and AFC control A1R14. The FPC control A1R5 is used to adjust the peak power control dc voltage level applied from the AK-3559/GRC-106 to FPC dc amplifier A2G41 in transmitter IP, and audio module 1A5. (fig 1014) The AFC control, A1R14, is used to vary the dc voltage level applied to voltage divider A1H4, A1R5 and A1R6. The mode of operation determines the point on the voltage divider that is to be connected to the SERVICE SELECTOR switch. The SERVICE SELECTOR switch connects the dc voltage from the voltage divider to AFC dc amplifier A3Q1 in transmitter IP, and audio module 1A5 through diode A1C7.

Tune Level Control Signal

302. The input to power amplifier 2A1A-V1, 2A1A-V2 is detected and applied to Receiver-Transmitter, Radio RT-662/GRC when the TUNE-OPERATE switch is set at TUNES. This voltage is used in addition to the operate AFC signal, to provide additional control over the RF-662/GRC required for tuning. The input to the grids of power amplifier 2A1A-V1, 2A1A-V2 is applied to a shunt detector circuit. When the signal goes positive, capacitor A1A14C1 will charge nearly the peak value of the applied signal. The negative portion of the signal will be shunted to ground through the low impedance of diode CR1. On the positive portion of the signal, diode CR1 will be reverse biased, causing capacitor C1 to discharge through resistors R10 and R11 and thermistor RT1. The discharge time constant is such that a modulated dc signal is applied to the base of emitter follower Q2. Emitter followers Q1 and Q2 are used to provide a high impedance load for the shunt detector circuit and a low impedance output to the RF-662/GRC. The output from emitter follower Q1 is applied through pin 25 of connectors 2A1A-X5 and 2A5-J1 and connects 8 and Q1 of TUNE-OPERATE switch 2A5J6 (TUNE and position) to pin B of CONTROL connector 2A5J2 for application to the RF-662/GRC.

303. Thermistor HT1 provides temperature compensation for the drive to emitter follower Q2. Capacitor C2 is an RF bypass. Resistor 2A1A1-W7 provides a dc return for the tune AFC circuit.

304. The output from emitter follower A1A1A14-V1 is applied through pin 25 of connectors 2A1A-X5 and 2A5-J1, contacts 8 and C1 of TUNE-OPERATE switch A1-R6 (when set at TUNES), feedthrough capacitors A1A12C3, A1A12C, to pin B of CONTROL connector A1J2. CONNECTOR connector A1J2 is connected through Cable Assembly Special Purpose, Electrical CX-1000U to PA CONTROL connector A1C0 on the RT-662/GRC. The dc signal is applied through L-section filter 1A1C3G1-1A13L3, (fig 1026) diode A1C8B. Tune level control A1R13 is used to adjust the level of the tune level control signal to AFC dc amplifier A3Q1 in transmitter IP, and audio module 1A5. (fig 1014)

BLOCK DIAGRAM OF RF AMPLIFIER, AM-3559/GRC-106 (fig 33)

Main Signal Flows

305. The RF output from Receiver-Transmitter, Radio RT-662/GRC is connected to RF DRIVE connector A5J3. RF DRIVE connector A5J3 connects this RF signal to the input bridge circuit. This input bridge circuit provides the necessary isolation between the RT-662/GRC and the feedback loop in Amplifier, Radio Frequency AM-3559/GRC-106. Output signals from the input bridge circuit are connected to driver amplifier A1V7, where they are raised in level and applied to power amplifier A1A1-V1-A1A1-V2. One of thirty tuned transformers (mounted on the motor-driven turret assembly) is connected into the output circuit of driver amplifier A5V. The tuned transformer is automatically programmed into the circuit according to the operating frequency selected at the RT-662/GRC. These tuned transformers ensure optimum load impedance for driver tube A5V, providing low distortion and maximum voltage transfer.

Power amplifier A1A1-V1-A1A1-V2 consists of two electron tubes connected in parallel that raise the RF signal level to 1000 watts PEP. The output signals from power amplifier A1A1-V1-A1A1-V2 are connected through tune discriminator A1A1 and load discriminator A1A2 to the antenna coupler circuits. Feedback is provided between power amplifier A1A1-V1-A1A1-V2 and driver amplifier A5V to ensure linear operation. One of the tuned transformers (mounted on the motor-driven turret assembly) is connected into the output programmed into the circuit according to the frequency selected at the RT-662/GRC. These tuned transformers ensure optimum load impedance on the power amplifier tubes providing low distortion and maximum power output to the antenna coupler. The antenna coupler consists of the normally-tuned antenna tuning and antenna loading circuits, and the automatically programmed antenna switching circuits. When the TUNE-OPERATE switch is set to OPERATE, the power output from the antenna coupler is applied through delay ASK and switch A5S5 to either WHIP connector A5S6 or 50 QM LINE connector A5S5.

Tuning

306. The phase and load discriminator circuits are each essentially a toroidal trans-
former, through which the output signals from power amplifier A1A1V1 - A1A1V2 are passed to the antenna coupler circuits. The discriminator A1A1 senses any phase difference between the transmitted voltage and current waveforms and displays a relative indication proportional to the difference on ANT. TUNE meter A5M2. Load discriminator A1A2 senses any difference in magnitude between the transmitted voltage and current waveforms and displays a relative indication, proportional to this difference, on ANT. LOAD meter A5M3. The antenna tuning and antenna loading circuits are varied by the ANT. LOAD and ANT. TUNE controls, respectively. When the TUNE-OPERATE switch is set at TUNE, the ANT. TUNE and ANT. LOAD controls are adjusted for zero indications (center scale) on their respective meters, A5M2 and A5M3. When the ANT. TUNE meter gives a center zero indication, there is no phase difference between the transmitted voltage and current waveforms. When the ANT. LOAD meter gives a center zero indication, the voltage and current waveforms are in proper ratio for a 50-ohm line impedance. The antenna and the AM-3349/GFC-106 will be correctly matched in this condition for a 50-ohm resistive line impedance. A counter is mechanically coupled to the ANT. LOAD and ANT. TUNE controls to provide a reference indication, which is recorded on the LOGGING CHART for future tuning to the same operating frequency.

Level Control Signal Generation

307. Two level control signals are generated in the AM-3349/GFC-106: operate and tune. The output from power amplifier A1A1V1 - A1A1V2 is envelope-detected by diode A1A3CR and applied to emitter follower A1A3Q1. The modulated dc output from emitter follower A1A3Q1 is applied to pin F of CONTROL connector A5J2. This signal is then applied to the voltage divider network in the RT-662/GRC, where it is processed and used for controlling the system gain. The input to power amplifier A1A1V1 - A1A1V2 is also envelope-detected by detector A1A1A10B4, A1A1A10B5, and applied to emitter followers A1A1A1Q1 and A1A1A1Q2. The emitter followers provide a high shunt impedance for the detector load. The modulated dc output from the emitter followers is applied to pin E of CONTROL connector A5J2 through TUNE-OPERATE switch A5S5, when it is set at TUNE. This signal is then coupled to the RT-662/GRC. The tune level control signal provides the additional control in the system gain, which is required when tuning the system.

Power Supply

308. Any time that the SERVICE SELECTOR switch on the RT-662/GRC is set at STANDBY or any operating position, a ground is applied from pin X of CONTROL connector A5J2 to the coil of relay A5A2X1. When PRIM PWR circuit breaker A5A2C1 is set ON, 27 volts dc is also applied from PRIM POWER connector A5J2 to relay A5A2X1. This energizes relay A5A2X1, and this, in turn, applies the 27 volts dc to the dc-to-dc converter assembly and to the dc-to-ac inverter assembly. These two assemblies produce all voltages used in the AM-3349/GFC-106 except the 27 volts dc. Under-voltage and over-current protection for the dc-to-dc converter assembly is also provided.

Parameter Monitoring

309. TEST METER A5M1 is provided to monitor various voltages and parameters of the AM-3349/GFC-106 to determine whether or not the equipment is functioning properly. TEST METER

M1 provides indications of the parameters selected by TEST METER switch S1.

Receive Function

310. During receive operation, any RF signal received by the antenna is applied to either WHIP connector 2A5J5 or 50 OHM LINE connector 2A5J5, depending on the antenna being used. The RF signal is applied through switch 2A5S5, and antenna switching relay 2A5K1, to RTVR ANT connector 2A5J4. RTVR ANT connector 2A5J4 is connected to RECEIVER IN connector 1A5: 6 on Receiver-Transmitter, radio RT-662/GRC.

DRIVER AND POWER AMPLIFIER STAGES (Fig 1023)

General

311. The driver and power amplifier stages amplify the low level from the transmitter section of Receiver-Transmitter RT-662/GRC to a 400-watt FEP level in the SSEG and AM modes. In the CW and PEP modes the level is 200-watts average power.

Driver Amplifier

312. Driver amplifier 2A5V1 amplifies the low level output from the RT-662/GRC to a level suitable for driving power amplifier 2A1A1V1, 2A1A1V2. The output from the RT-662/GRC
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ANTENNA TUNING ELEMENTS
ANTENNA COUPLER A3
ANTENNA LOADING ELEMENTS

RF DETECTOR CRI
P/O A4A3

EMITTER FOLLOWER Q1
P/O A4A3

ANALOG SWITCHING

ANT. LOAD
COUNTER

TRANSMIT
50 OHM LINE
ASJ6
ASJ5

RECEIVE
 Whip
ASJ4

LEVEL CONTROL SIGNALS TO THE ATTENUATOR IN TRANSMITTER IF AND AUDIO MODULE 145

P/O A5J2-F
P/O A5J2-E

TEST METER

PRIM. VOLT
LOW VOLT.
HIGH VOLT.
DRIVER CUR.
GRID DRIVE
PA CUR.
POWER OUT

NOTES:
1. PREFIX ALL REFERENCE DESIGNATIONS ON THIS DIAGRAM WITH UNIT NUMBER 2.
2. ( ) INDICATES FRONT PANEL MARKING

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is applied to RF DRIVE connector 2A5J3 on the front panel. From here, it is routed through connectors 2A5J1-A1, 2A1X6-A1, 2A1X6A-A1, J1-A1, and P1 to connector A1J1. From connector A1J1, the RF input signal is applied to an input bridge (fig 34). The input bridge algebraically sums the RF input with an inverse feedback signal that is proportional to the output from power amplifier 2A1A1V1, 2A1A1V2. The inverse feedback maintains the gain characteristics of the AM-3349/3RG-106 relatively constant over the entire range of transmitted frequencies. It also increases the linearity, thereby reducing the intermodulation distortion.

![Diagram](image)

**FIG 34 – DRIVER INPUT BRIDGE**

3.13. The RF input is coupled by capacitor A1C1 to the primary of transformer A1T1, and coupled by transformer action to the secondary of transformer A1T1. Resistor A1R4 provides the proper termination for the RF input signal. The primary of transformer A1T1 is tuned by capacitor A1C1 and the secondary of transformer A1T1 is tuned by capacitor A1C2, the inter-electrode capacity Cgk, and the stray capacity of the transformer. Both the primary and secondary windings of transformer A1T1 are tuned to the geometric center (8 Mc) of the pass-band. This provides a broadband tuned input for operating frequencies between 2 and 30 Mc and minimizes the VSWR on the input line.

3.14. The feedback signal from the plates of power amplifier 2A1A1V1, 2A1A1V2 is applied to connector J1-A1, from which it is applied to the junction of capacitors A1C3 and C2. Normally, the feedback is 180° out of phase with the RF input. The feedback signal is divided by the capacitive divider arms of the bridge: A1C3, A1C2 and A3C2, Cgk. When the bridge is balanced, a very small portion of the feedback signal appears across the secondary of transformer A1T1. However, the reactance of capacitor A1C2 causes the RF input signal at the secondary of transformer A1T1 to appear between the grid of driver amplifier V1 and ground. This RF input signal is algebraically summed with the feedback signal. The resultant signal (the net difference) is coupled by capacitor A1C5 to the grid of driver amplifier V1. Capacitor A1C5 to the grid of driver amplifier V1. Capacitor C2 is adjusted for best bridge balance at the worst conditions of Cgk (30 Mc). Since the signal applied to driver amplifier V1 is the difference between two relatively large signals, it is evident that, given a constant RF input, a small change in feedback will produce a large change in the signal applied to the grid of driver amplifier V1. It is also evident that this change will, in effect, minimize the original change in the feedback signal as a result of the system gain. The feedback signal is directly related to the input by the gain factor of the AM-3349/3RG-106. Therefore, moderate changes in the regulated supply voltages resulting from temperature variations, or changes in tube or component characteristics that would normally have great effect on the overall gain and sensitivity, will be minimized.

3.15. The output from the input bridge is raised in level by driver amplifier V1 and is developed across one of thirty interstage tuned circuits which form a part of turret assembly 2A2. These tuned circuits are mounted on a motor driven-turret and are automatically programmed into the circuit according to the operating frequency. The output from the tuned circuit is applied to connectors J1-A2 and J1-A3 for application to power amplifier 2A1A1V1,
2A14AV2. Capacitor C6 is adjusted to compensate for the input capacitance of power amplifier 2A14AV1, 2A14AV2 and the output capacitance of driver amplifier V1. This prevents mistuning to ensure optimum power transfer.

316. The 500-volt dc output from the dc-to-dc converter assembly is regulated to 200 volts dc by zener diode 2A14VR3. This regulated 200 volts dc and the 27-volt dc primary power are used to develop the operating voltages for driver amplifier V1. The 27 volts dc, applied to pin 1 of connector J1, is regulated to 15 volts dc by zener diode A1VR1 and applied across resistors A1R5 and A1R6. A portion of this voltage is applied through isolating resistor A1R2 to the grid of driver amplifier V1 as a fixed bias. Driver amplifier V1 also develops a self-bias across resistors A1R3 and A1R4. This combination of biasing results in a cathode dc load line (on the transfer characteristics) that has a very shallow slope with respect to using either the self-biasing method or fixed bias method alone. Therefore, changes in tube characteristics will have only a minimum effect on the operating point of driver amplifier V1. Capacitors A1C6, A1C7, and A1C8 are RF bypass capacitors, used to reduce intermodulation distortion when voice transmissions are being made. The 200 volt dc present at pin 7 connector J1 is used as the plate supply for driver amplifier V1 and is regulated to 164 volts dc by zener diodes VR1 and VR2 for use as the screen supply for driver amplifier V1.

**Power Amplifier Stage**

317. Power amplifier A1V1, A1V2 amplifies the output from driver amplifier 2A8V1 to a level of approximately 400 Watts PEP, for application to the impedance matching networks in antenna coupler assembly 2A3. The output from driver amplifier 2A8V1 is coupled by the interstage tuned transformer (2A2A16 through 2A2A30) to the neutralization bridge (fig 35). The neutralization bridge is used to compensate for the feed-back between the output and input of power amplifier A1V1, A1V2 through the inter-electrode capacitance. One leg of the bridge is composed of the two inter-electrode capacitances Cg2 and Cgk. The other leg of the bridge is composed of capacitors A1C3, A1C4, and A1C24. Capacitor A1C4 is adjusted so that the voltage developed across each leg of the bridge is equal in magnitude to:

\[
\frac{1}{A_{1C24}} = \frac{1}{C_gk}
\]

**Fig 35 - PA Neutralization Bridge**
CN is equal to A105 times A104 divided by A103 plus A104. Therefore, since the voltage in the two legs are in phase with each other, the feedback will be canceled and the input to the grids of power amplifier A1V1, A1V2 will be the output from the driver amplifier 2ASV1. Resistor A1R6 provides the correct termination for the RF input pilot. The amount of feedback to driver amplifier 2ASV1 is determined by capacitor A102.

316. The output from the neutralization bridge is coupled by capacitors A105, A108, A106 and A109 to the control grids of power amplifier A1V1, A1V2. Power amplifier A1V1, A1V2 consists of two electron tubes connected in parallel to raise the level of the output from driver amplifier 2ASV1 to a level of 400 Volts. This RF output from power amplifier A1V1, A1V2 is developed across one of the tuned transformers mounted on the power amplifier front panel assembly 2AS2. The transformer in the circuit depends on the frequency of the operating channel. The automatic tuning system automatically switches the correct transformer into the circuit. The required capacitors for the tuning the primary and secondary of the transformer used is mounted on the assembly 2AS3. Capacitor ZASV2 is adjusted so that at 50 kHz, capacitor ZASV2 will exactly equal 90 uF. Capacitor A1C22 is adjusted to compensate for the output capacity or power amplifier A1V1, A1V2. The output from power amplifier A1V1, A1V2 is applied through connectors 2A941B, 2AI19E, 2A1L1, and discriminator assembly 2A1L to the antenna coupler.

319. The 2400 volts dc output from the dc-to-dc converter assembly 2AS5A2 is applied through the primary of the transformer switched into the output circuit of power amplifier A1V1, A1V2 to the plates of power amplifier A1V1, A1V2. The screen voltage for power amplifier A1V1, A1V2 is developed from the 500-volts dc output from the dc-to-dc converter assembly. This 500 volts dc is regulated to 400 volts dc by zener diodes A1V1R and A1V2R. The 500 volts dc is also regulated to 200 volts dc by zener diode A1V2R2. This 200 volts dc is used as the required plate and screen supply for driver amplifier 2ASV1. The bias for power amplifier A1V1, A1V2 is developed from the -110 volts dc output from the 2AS5A1. This -110 volts dc is regulated to -95 volts dc by zener diodes A1A1A1R2 and A1A1A1V3. Potentiometer A1A1A1E5 is used to adjust the amount of bias applied to tube A1V2 and potentiometer A1A1A1E6 is used to adjust the bias applied to tube A1V1. The arrangement of zener diodes A1A1A1R2 and A1A1A1V3 and potentiometers A1A1A1R2 and A1A1A1R6 is such that the bias to the two tubes can be varied from -75 to -20 volts dc. The two separate adjustments are used to ensure that both tubes are at the same operating point and share the load during operation.

**KEYING CIRCUITS**

**Keying Function Initiation**

320. When the RT-662/GRC is keyed, a ground is placed on the keyline. This turns on transmit-receive switch A5A41, (Fig 1015) which turns on transmit-receive switch A5A41 in transmitter IP. and audio module 'A5. With transmit-receive switch A5A41 conducting, T/R line 3 is grounded. This ground is applied through pin 32 of connectors A5A41 and A1X5, feed-through capacitor A1C29, and L-section filter A1A1L6-A1A1O6 to pin P of PA CONTROL connector A1J20. PA CONTROL connector A1J20 is connected to CONTROL connector A5J2 on the AM-3349/GRC-106 front panel. From pin P of CONTROL connector A5J2, the ground is applied through pin 1 of relay 5A3K3 to pin 3 of relay A5A2E2. With the RT-662/GRC SERVICE SELECTOR switch set at any operate position (SS9, HSK, A1, C1, or PSS), the operate 27 volts dc is applied to pin 1 of relay A5K1 and pin 3 of A5A2E2. Relay A5K1 will be energized and connect the RF line to the antenna in use and disconnect RCVR ANT connector A5J4. Relay A5A2E2 is energized and turns on the dc-to-dc converter assembly and completes the feedback path for the assembly.

**Tune-Looking Interlock**

321. If a frequency change is made at the RT-662/GRC, the detents of switches A187, (Fig 1026) rear, A86, section 1, rear, (Fig 1025) or A185, rear, (Fig 1025) connect a momentary ground from contact 7 to 8, contact 7 to 4, or contact 5 to 4, respectively. The momentary ground is applied through feed-through capacitor A1C30 and L-section filter A1A3L1-A1A3O4 to pin H of PA CONTROL connector A1J20. Pin H of PA CONTROL Connector A1J20 is connected to pin H of CONTROL connector A5J2 on the AM-3349/GRC-106. Pin H of CONTROL connector A5J2 is applied to L-section filter A1A3C5-A1A3G6, feed-through capacitor A1C12, pin 20 of connectors A5J1 and A1X5, pins 6 and 29 of connectors A1X23 and A5J1, and pin 1 of connectors A1A1X7 and A7F to pin 3 of tune looking relay A7K5, which energizes and locks itself through contacts 1 and 6. The ground on contact 2 of operator relay A7K5 is applied through contact 5, pin 7 of connectors A7J1 and A1A1X7, pin 13 of connectors A7J1 and A1A1X7, pin 15 of connectors A1X5 and A5J1, contacts 6 and 1 of TUNE-
OPERATE switch A586, pin 23 of connectors A591 and A1058, and pin 12 of connectors A104X7 and A701 to connect 1 of tune locking relay A756. When tune locking relay A756 energizes, the connection between contacts 2 and 4 is broken. This breaks the 27-volt operate line, de-energizes relays ASK1 and ASK2. Tune locking relay A756 will not de-energize until TUNE-OPEKATE switch S6 is set at TUNE, breaking the self-locking ground path. This informs the operator that he must check his tuning and readjust the ANT TUNE and ANT LOAD controls on the AM-3349/GRC-106 before reoperating the unit.

Tune Information

322. When the TUNE-OPEKATE switch is set at TUNE, the ground at contact 2 of operate relay A753 is applied through contact 5, pin 7 of connector A701 and A104X7, pin 13 of connectors A104X6 and A591, contacts S1 and 2 of TUNE-OPEKATE switch A586, and diode ASK5, causing relays ASK1, and ASK2 to be energized if the tuning cycle is complete and all over-current or under-voltage conditions exist. This ground is also connected through feedthrough capacitor A107 and L-section filter A104X1 to pin M of CONTROL connector A592. CONTROL connector A592 is connected to PA CONTROL connector A5210 on the EE-662/GRC. Pin 12 of PA CONTROL connector A5210 applies this ground through L-section filter A104C-A104F, and A104X7. Pin 10 of connector A104X5 (fig 104A) mates with pin 10 of connector J1 of transmitter IF, and audio module 1A5. Pin 13 of connector A104X7 (fig 106A, fig 100A) mates with pin 13 of connector J1 on receiver IF module 1A7. This ground is used in transmitter IF, and audio module 1A5 for carrier re-insertion and changing the ACO level. It is used in receiver IF module 1A7 for turning off the balanced modulator.

TEST METER M1 FOR PARAMETER MONITORING

General

323. Switch A582 and test meter A584 provide a monitoring function to assure that the correct voltages and currents are present in the power amplifier.

Primary Voltage

324. When the SERVICE SELECTOR switch on Receiver-Transmitter, Radio IF-662/GRC is set at any operate position (SERB NSK, AM, CW, FSK) and the AM-3349/GRC-106 PRIM. PWR. switch (A58B) is set at ON, the 27-volts dc primary power is applied to contact 4 of relay A751 from PRIM. POWER connector J7. Also at this time, ground is applied to pin 1 of relay A2K1 from pin M of CONTROL connector J2. Therefore, relay A2K1 energizes, and the 27 volts dc at contact 2 is applied through pin 5 of connectors J1 and 2A10X5 and pin 6 of connectors 2A10X6 and J1, and 2A10X7 to contacts X1 and X2 of time delay relay 2A10X8. After 60 seconds, time delay relay 2A10X8 applies the 27 volts dc through contacts X2 and X1 to pin 7 of operate relay 2A10X5, energizes, due to the ground on pin 3 from pin P of CONTROL connector J2. At this time, the 27 volts dc is applied from contact X2 of time delay relay 2A10X6, through contacts 1 and 6 of operate relay 2A10X6, pin 15 of connectors 2A10X1 and 2A10X7, pin 28 of connectors 2A10X6 and J1, and resistor ASK1 to connect 1 of TEST METER switch S2-B. Therefore, when the TEST METER switch S2 is set at PRIM VOLT, TEST METER M1 and resistor ASK2 are connected across the 27-volts dc supply through contacts 1 and 10 of sections A and B of switch S2. Resistor ASK1 is the metering resistor for TEST METER M1 when measuring the 27-volts dc primary power. See fig 36.

Low Voltage Power Supply

325. The 500-volts dc output from dc-to-de converter assembly (F/O 2A5) developed across voltage divider ASK1, ASK2, ASK3, ASK4, and a proportional amount is connected to meter M1 through contacts 2 and 10 of TEST METER switch S2, Sections A and B. Resistor ASK1 is the metering resistor for TEST METER M1 when measuring the 500-volts dc output. See fig 37.

High Voltage Power Supply

326. The bleeder circuit for the 2400-volts dc output from dc-to-de converter assembly A2 consists of resistors A2R3 sections A to D which are connected between the output (positive side of diode bridge A2CR6) and the return (negative side of diode bridge A2CR6). When TEST METER switch S2 is set at HIGH VOLT, the high voltage output is sampled across resistor A2R3, and this proportional amount is connected to TEST METER M1 through contacts 3 and 10 of TEST METER switch, sections A and B. Resistor A2R3 is the metering resistor for TEST METER M1 when measuring the 2400-volts dc output. See fig 38.
Driver Plate Current

327. When TEST METER switch S2 is set at DRIVER CUR, TEST METER switch S2 connects TEST METER M1 between the cathode of driver amplifier 2A5V1 and ground, through resistor 2A5A1R9, pin 4 of connectors 2A5V1 and 2A5V2, pin 27 of connectors 2A5A5 and J1, and contacts 4 and 10 of sections A and B of TEST METER switch S2. The meter then provides an indication of the amount of self bias developed across resistors 2A5A1R3 and 2A5A1R4, or, the amount of plate current. Resistor 2A5A1R8 is the metering resistor for TEST METER M1 when measuring the plate current of driver tube 2A5V1. See fig 35.

Grid Drive

328. When TEST METER switch S2 is set at GRID DRIVE, TEST METER M1 is connected to the tube ALC output from emitter-follower 2A1A1V1 through pin 25 of connectors 2A1A1X5 and J1, resistor 2A1A1R8 and contacts 5 and 10 of TEST METER switch S2. This output is directly proportional to the grid drive applied to power amplifier 2A1A1V1, 2A1A1V2. Resistor 2A1A1R8 is the metering resistor for TEST METER M1 when measuring the drive to the grids of power amplifier 2A1A1V1, 2A1A1V2. See fig 40.

Power Amplifier Plate Current

329. The return path for power amplifier 2A1A1V1, 2A1A1V2 plate current is through resistor 2A1A1R7 and the soil of the over-current sensing relay 2A1A1X1 to the negative side of diode bridge 2A1A1R6. When TEST METER switch S2 is set at PA CUR, TEST METER M1 is connected across resistor 2A1A1R7. The voltage drop across resistor 2A1A1R7 is applied through resistor 2A1A1R6 and contacts 6 and 10 of TEST METER switch S2, sections A and B. Resistor 2A1A1R6 is the metering resistor of TEST METER M1 when measuring the plate current of power amplifier 2A1A1V1, 2A1A1V2. When setting the quiescent operating point for power amplifier 2A1A1V1, 2A1A1V2 PA idle current switch 2A1A1R6 is depressed. This parallel resistor 2A1A1R6 with resistor 2A1A1R7 to change the sensitivity of TEST METER M1. The circuitry is shown in fig 41. Switch 2A1A1R8 is adjustable when the chassis is withdrawn from the case. The only time this metering circuit is used is when tubes are changed in the power output stage. With no excitation one tube at a time is put into the amplifier. The bias is then set to center scale for each tube, so as to maintain balance in both tubes.

Power Output

330. The output from the operate ALC circuit is sampled across resistors 2A1A1R3 and 2A1A1R5. When TEST METER switch S2 is set at POWER CUR, the sampled output from voltage divider 2A1A1R3, 2A1A1R5 is connected through pin 10 of connectors 2A1A2 and F1, pin 12 of connectors 2A1A5 and J1, and across TEST METER M1 through contacts 7 and 10 of TEST METER switch S2. This voltage is directly proportional to the power output from the AM-3349/86-10S. See fig 42.

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**Fig 35 - Primary Voltage Metering (Position 1)**

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Fig 37 - 500V Line Metering (Position 2)
FIG 38 - 2400 VOLT METERING (POSITION 3)
FIG 39 - DRIVER PLATE CURRENT METERING (POSITION 4)
FIG 40 - GRID DRIVE METERING (POSITION 5)
TO NEGATIVE TERMINAL OF 2400V BRIDGE RECTIFIER

ASR1 3.9 Ω

ASR3 21.5KΩ

ASR4 1910Ω

AS51 P.A. IDLE CURRENT

S2A

M

S2B

FIG 41 - PA PLATE CURRENT METERING (POSITION 5)
FIG 42 - PA POWER OUTPUT METERING (POSITION 7)
CIRCUIT DESCRIPTION AND OPERATION OF THE ANTENNA COUPLER (Fig 45 and 1026)

General

331. The antenna coupler assembly is a semi-automatic impedance matching network consisting of manually and automatically programmed parts. The function of this network is to match the impedance of the system antenna to the 50 ohm output impedance of the power amplifier at the desired operating frequency. Bandswitch 2A381 is automatically programmed to rough tune the AM-3549/GRC-106 so that it is within the operating range of the manually variable circuit, consisting of inductance 2A384 and capacitor 2A385. After antenna coupler 2A3 is programmed, ANT LOAD control 2A3L1 is adjusted so that the power amplifier looks into an impedance of 50 ohms. Capacitor 2A3C86 is adjusted so that the phase angle of the impedance is zero. Therefore, after tuning, the power amplifier works into the desired resistive load of 50 ohms. Fig 45 illustrates the impedance matching networks according to the operating frequency. The RF power output is applied through relay 2A3B1 and switch 2A3B3 to WHIP connector 2A535 or 50 OHM LINE connector 2A535, depending on whether a whip or doublet antenna is used. The power output is connected to the antenna from the appropriate connector.

332. When the interunit tuning cycle is completed switches 2A3B1 and 2A3B5 will be positioned according to the LC frequency setting for which the units are to be tuned. These switches provide coding information for programming the antenna coupler assembly for the frequency band in use. The chart in table 8 provides a listing of the thirty tuning positions of these switches and their corresponding LC passbands. The function of whip coding switch 2A2B4 is to generate the coding information to position capacitor 2A3C7 and bandswitch 2A3B1 when a whip antenna is being used. The function of 50-ohm line coding switch 2A3B3 is to generate the coding information to position capacitor 2A3C7 and bandswitch 2A3B1 when a doublet antenna (50-ohm line) is being used. As shown, the unit is tuned for position 1 (2.0 to 2.5 Mc). Assume that the operating frequency is changed (at Receiver-Transmitter, Radio RC-662/GRC) to 26.000 Mc. The interunit tuning will be accomplished and we will set switches 2A3B1 and 2A3B5 at 13. These switches will then function to program the antenna coupler assembly for this new frequency. The programming provides the configuration according to the operating frequency as shown on fig 45. The following paragraphs provide a detailed description of the programming necessary to obtain the configuration for the operating frequency for various types of antennas.

Whip Antenna Programming

333. When using a 15-foot whip antenna, whip coding switch 2A2B4 will program band-switch 2A3B1 and capacitor 2A3C7 as follows.

a. Bandswitch A3B1 positioning: When switch 2A3B5 connects WHIP connector 2A3J6 into the circuit, it mechanically positions microswitch 2A3A1. A ground from micro-switch 2A3A1 is applied through pin 17 of connectors 2A3J4 and 2A3J5 and pin 35 of connectors 2A3A2 and 2A3J4 to the common contact 13 (corresponding to position 13) of switch 2A2B4 to pin 9 of connector 2A2A4, which mates with pin 9 of connector 2A2A2. A ground path is then established through pin 3 of connectors 2A1X3 and 2A3H, via pin 10 to pin 4 of switch 2A3B to bandswitch motor relay K3, capacitor 2A3C2, pin 22 of connectors 2A3H and 2A3J1, and pin 3 of connectors 2A1X7 and 2A1Y1 to pin 3 of bandswitch motor relay AK3. Since 27 volts dc is applied to pin 7 of bandswitch motor relay AK3, bandswitch motor relay AK3 will energize and apply 27 volts dc to contacts 1 and 6 of relay AK3, pin 2 of connectors 2A1X1 and 2A1X7, pin 23 of connectors 2A1X3 and 2A3H, and feedthrough capacitor 2A3C2 to motor 2A3B2. Since the other side of motor 2A3B2 is grounded, it will rotate, turning RF bandwidth coding switch 2A3B2 and the set of switch 2A3H until the notch of the wiper of switch 2A3B2 aligns with contact 10. This will then break the ground path to pin 3 of bandswitch motor relay AK3, causing it to de-energize. Ground will then be connected (in place of 27 volts dc) to motor 2A3B2 through contacts 8 and 6 of bandwidth motor relay AK3. Motor 2A3B2 is then dynamically braked. With the antenna connected to WHIP connector 2A3J6, the RF bandwidth coding will vary dependent upon frequency.

b. Capacitor 2A3C27 positioning: Assuming that the interunit tuning has placed switch 2A2B4 at position 13 as above, there will be no ground path. Using another example, such as a position 12 (19.000 Mc) a ground path will be produced as follows: ground is connected from the common contact of switch 2A2B4 through contact 12 of switch 2A2B4 to pin 20 of connector 2A2J1, which mates with pin 20 of connector 2A2A2. The ground is then connected through pin 13 of connectors 2A1X3 and 2A3H, feedthrough capacitor 2A3J3 and contact 9 of switch 2A3H to contact 20 of switch 2A3H. Contact 20 of switch 2A3H connects the ground through feedthrough capacitor 2A3J2.
FIG 43 - IMPEDANCE MATCHING NETWORKS AT VARIOUS FREQUENCIES (AE COUPLER)
pin 12 of connectors A381 and A1X4, and pin 9 of connectors A1A1X7 and A7J1 to pin 3 of capacitor motor relay A7K2. Since 27 volts dc is connected to pin 7, capacitor motor relay A7K2 will energize and apply 27 volts dc through contacts 1 and 6 of relay A7K2, pin 1 of connectors A3J1 and A1A1X7, pin 14 to motor A3B1. Since the other side of motor A3B1 is grounded, it energizes and rotates switch A383 and capacitor A3C27. Capacitor A3C27 is only in the circuit, however, when bandswitch A381 is in position 6. When the wiper notch of switch A383 is aligned with contact 9, the ground path is broken and capacitor motor relay A7K2 de-energizes. Motor A3B1 is then dynamically braked by a ground (instead of 27 volts dc) connected from contact 6 of capacitor motor relay A7K2 through contact 5, pin 1 of connectors A3J1 and A1A1X4, pin 14 of connectors A1A3 and A3J1 and readthrough capacitor A3C14.

Doublet Antenna Positioning

334. When using a doublet antenna, switch A382 will program bandswitch A381, and 50-ohm line switch A285 will program capacitor A3C27 as follows.

a. Bandswitch A381 positioning. When the antenna is connected to 50 OHM LINE connector A3J5, the ground path to switch A285 from switch A381 is broken. A new ground path is then applied from switch A381 through pin 18 of connectors A3J1 and A1A1X5, pin 37 of connectors A1A4 and A2J1, diode A2A3C1R1, pin 27 of connectors A3J2 and A1A1X2, pin 1 of connectors A1A3 and A3J1 and readthrough capacitor A3C1 to contact 14 of switch A382. The motor is energized as previously stated and turns switch A382 until the wiper notch is aligned with contact 14, breaking the ground path. This setting of bandswitch A381 is then used for all frequencies.

b. Capacitor A3C27 positioning. Assuming that the interunit tuning has positioned switch A285 to position 13 and that switch A381 is connected to 50 OHM LINE connector A3J5, the ground path is as follows: a ground is connected from the common contact of switch A285 through contact 13, pin 30 of connectors A3J1 and A1A1X2, pin 10 of connectors A1A3 and A3J1, and readthrough capacitor A3C10 to contact 7 of switch A383. Contact 20 of switch A383 then connects ground to pin 3 of capacitor motor relay A7K2, which energizes and in turn energizes motor A3B1. Motor A3B1 rotates switch A383 and capacitor A3C27 until the wiper notch of switch A383 is aligned with contact 7, causing the ground path to be broken. Capacitor motor relay A7K2 then de-energizes and motor A3B1 is dynamically braked.

Programmed Configurations

335. The bandswitching accomplished in the above description results in the setting of bandswitch A381 and capacitor A3C27. Bandswitch A381 selects either a tap on inductor A3L2, the straight through position (position 4), or capacitor A3C27, depending on the frequency and the antenna used. The tap is used to apply a short across inductor A3L2 at the various frequencies where it is not used. The settings of A3J1, A3L1 and A3C25 result in the coarse tuning of the antenna to the AM-3349/GRC-106 for the desired operating frequencies. The AM-3349/GRC-106 is then fine tuned using the ANT, TUNE and ANT LOAD controls.

TUNE AND LOAD DISCRIMINATORS (Fig 1028)

336. TUNE DISCRIMINATOR: When the power amplifier is correctly tuned (50 ohm resistive load), the RF output voltage and current are in phase. When the output is reactive, tune discriminator 2A4M1 detects the resulting phase difference between the RF voltage and current and produces a DC voltage proportional to the phase difference. This voltage is applied to meter 2A5M2 which is located on the front panel. This meter provides a relative indication of the magnitude of phase difference for tuning.

337. LOAD DISCRIMINATOR: When the power amplifier is correctly loaded (50 ohm impedance), the RF output and current are of the correct magnitude to produce an output of 400 watts PEP. If the load for the power amplifier is greater or less than 50 ohms, the RF output voltage and current will no longer be of the correct magnitude to produce this 400 watt PEP output. This difference is detected by the load discriminator, which produces a DC output proportional to the difference. The DC voltage is applied to antenna Load Meter 2A5M3 on the front panel. This meter provides a relative indication of loading.

Discriminator Operation (Fig 44)

338. The RF output from power amplifier 2A4A1V1-2A4A1V2 is applied to connector 2A1P1, from which it is applied through connectors 2A4J1 and 2A4P1 to connector J1. This cable...
<table>
<thead>
<tr>
<th>POSITION</th>
<th>FREQUENCY Mo/s</th>
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<tr>
<td>1</td>
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<tr>
<td>2</td>
<td>3-3.5</td>
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<td>11-12</td>
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passes through toroidal transformer T1. Since toroidal transformer T1 is center-tapped, the RF output current will induce a voltage in each half of the winding. These voltages, designated E1 and E2, will be of equal magnitude, 90° out of phase with the RF output current, and 180° out of phase with each other. TUN meter output voltage is sampled across a capacitance voltage divider consisting of capacitors C2 and C1. This voltage, which is vectorially in phase with the RF output voltage, is applied to the center tap of toroidal transformer T1. The vectorial summation of the sampled voltage (E0) and induced voltage E1 is detected by diode CR1, producing a dc voltage E1 at the cathode of diode CR1. Similarly, the vectorial summation of E1 and E2 is detected by diode CR2, producing a dc voltage E2 at the cathode of diode CR2. Voltage E1 is applied through pin 1 of connectors 2AS5 and 2AF2, pin 28 of connectors 2AX10 and 2AP1, and resistor 2AS5R8 to one side of ANT. TUN meter 2AS5M2. Voltage E2 is applied through pin 7 of connectors 2AI2 and 2AI2 and pin 29 of connectors 2AX10 and 2AP1 to the other side of ANT. TUN meter 2AS5M2.

3.9. If the impedance of the RF output line is resistive, the RF output voltage and current will be in phase. Therefore, the two vectorial summations will result in E1' and E2' being equal, Fig 44, and there will be no difference in voltage across ANT. TUN meter 2AS5M2. The meter will then indicate center scale. 0° phase difference between the RF output voltage and current. If the impedance of the RF output line is inductive, the RF output current will lag the RF output voltage by some angle 8. Therefore, as shown in Fig 44, E1' will be greater than E2', causing ANT TUN meter 2AS5M2 to deflect to the left of center.

The degree of deflection will be proportional to the phase difference between the RF output current and voltage. If the impedance of the RF output line is capacitive, the RF output current will lead the RF output voltage by some angle 8. Therefore, as shown in Fig 44, E1' will be less than E2', causing ANT TUN meter 2AS5M2 to deflect to the right of center. The degree of deflection will be proportional to the phase difference between the RF output current and voltage. The phase angle is corrected by varying the value of capacitor 2AS26, when TUN-METER switch 2AS5 is set at TUNE. When TUN-METER switch 2AS5 is set at TUNE, E1' is applied through contacts C2 and B of switch 2AS5. This path changes the sensitivity of meter 2AS5M2 by bypassing resistor 2AS5R8 for diodes CR1 and CR2 through transformer A171.

3.10. Inductor L1 provides a dc return for diodes CR1 and CR2 through transformer A171. The values of these components are such that they are not frequency sensitive within the operating passband of the AM-3349/GRG-106. Capacitors C2 and C3 are RF bypasses. Resistors R1 and R2 provide a dc path for CR1 and CR2, respectively. Resistor R3 is an equalizing resistor to make the dc output from the phase discriminator the same as the output from the load discriminator. Capacitor 2AS5 bypasses any RF present in the meter voltage around meter 2AS5M2.

---

**Fig 44 - Vector Diagram of Discriminator Operation**

*a. ZL = RESISTIVE
IRF OUT IN PHASE
WITH RF IN
E1 = E2'*

*b. ZL = INDUCTIVE
IRF OUT LAGS RF OUT
E1' > E1
E2' > E2*

*c. ZL = CAPACITIVE
IRF OUT LEADS RF OUT
E1' < E1
E2' < E2*

RF OUT = RF OUTPUT VOLTAGE
IRF OUT = RF OUTPUT CURRENT
ERF OUT = RF OUTPUT IMPEDANCE
ERF = SAMPLED PORTION OF RF OUT
E1' = VOLTAGE AT CATHODE OF DIODE CR1
E2' = VOLTAGE AT CATHODE OF DIODE CR2
341. The RF output from power amplifier 2AM1V1, 2AM1V2 is applied through tune discriminator 2AH4 to connector 2AH4J4. From this point, the power output is connected through connector P4 and the load discriminator to connector J1. The current flow in this line induces a voltage in toroidal transformer T1. This induced voltage is detected by diode CR2, producing a dc voltage which is applied through pin 2 of connectors 2AH4J2 and 2AM2P2, pin 30 of connectors 2AMX5 and 2ASJ1, to one side of ANT LOAD meter 2AS5M3. The RF output voltage is sampled by capacitive divider C1, C2 and detected by diode CR1 to produce a dc voltage which is applied through pin 8 of connectors 2AH2J2 and 2AM2P2, pin 31 of connectors 2AMX5 and 2ASJ1, and resistor 2AS5R7 to the other side of ANT LOAD meter 2AS5M3. The impedance of the RF output line equals 50 ohms, capacitor C1 is adjusted so that the voltage at pin 8 of connector 2AH2J2 is equal in magnitude to the voltage at pin 2 of connector 2AH4J2. If the load impedance differs from the desired 50 ohms, the voltages at pins 8 and 2 of connector 2AH2J2 will differ. The amount of difference will be proportional to the degree of deviation from 50 ohms. These two voltages will cause ANT LOAD meter 2AS5M3 to deflect either right or left from center scale, indicating that the load must be decreased or increased to reach the 50 ohm balance point. The load is varied by varying the value of inductor 2AM1L, when TUNE-OPERATE switch 2AS96 is set at TUNE. When TUNE-OPERATE switch 2AS96 is set at OPERATE, the voltage at pin 31 of connector 2AH2J2 is applied through contacts C3 and 5 of switch 2AS5Q6. This new path changes the sensitivity of ANT LOAD meter 2AS5M3 by bypassing resistor 2AS5R7. Resistor R1 provides a dc return for diode CR1. Resistor R3 is a swamping resistor for toroidal transformer T1 to minimize the effects of frequency variations. Capacitors C3 and C4 are RF bypasses. Resistors R2 and R4 provide a dc path for diodes CR1 and CR2, respectively. Capacitor 2AS5Q6 bypasses any RF present in the voltage applied to meter 2AS5M3.
FIG 46 - LEVEL CONTROL INTERUNIT CIRCUITRY
ELECTRICAL AND MECHANICAL
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FIG 48 - RADIO SET AN/GRC-106 PRIMARY
106 PRIMARY POWER DISTRIBUTION - INTERUNIT CIRCUIT
<table>
<thead>
<tr>
<th>Fig</th>
<th>Description</th>
<th>Page</th>
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<tr>
<td>1001</td>
<td>Frequency Standard 1A3 (Part 1)</td>
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<td>1002</td>
<td>Frequency Standard 1A3 (Part 2)</td>
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<tr>
<td>1003</td>
<td>RF Amplifier (exploded view of turret in ET-662)</td>
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<tr>
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<td>RF Amplifier (100 Kc - 10 Kc turret in ET-662)</td>
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<td>Receiver Audio 1A10</td>
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<td>Internal Auto level control 1A5</td>
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<td>DC to DC Converter 1A11</td>
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<td>Circuit Diagram ET-662 Chassis (Part 3)</td>
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<td>Circuit Diagram Power Amplifier AM-5349/G3-106</td>
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<td>1029</td>
<td>Power Amplifier AM-5349/G3 - Turret Assembly Details</td>
<td>1029</td>
</tr>
</tbody>
</table>
ELECTRICAL AND MECHANICAL ENGINEERING INSTRUCTIONS (AUST)

FIG 1001 - FREQUENCY STAND
NOTES:
1. PARTIAL REF DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH IA3
2. UNLESS OTHERWISE SPECIFIED, ALL RESISTOR VALUES ARE IN OHMS ±2%, 1/4W
   ALL CAPACITOR VALUES ARE IN MICROMICROFARADS
3. RESISTIVE WIRE IS USED FOR R4 & R2
   APPROX RESISTANCE IS SHOWN
4. _ _ _ INDICATES EQUIPMENT MARKING

P1, J2, P2, E1

- 20VDC FROM A2, E2

- 20VDC TO PART OF J1

A2

OVEN CONTROL CIRCUIT

Oven Assembly A1

Q4

Q3 2N335

Q1 2N485

POWER AMPL

SEE NOTE 3

R1 30

R2 40

S1 NC

S2 NC

C4 33UF

R5 3900

C6 1UF

CR2 IN3666

CR3 IN3666

RII 2700

RIZ 4700

I OC

IT & DRIVER

V1 I+ IN755A

+20VDC

P3, J3, P3

E2

PART OF JA

PART OF JA2 & E2

P2, J9, P1

E3

PART OF JA1

P1, J2, P2

E1

+20VDC

+20VDC

R4 470

R7 2000

TEMP ADJ

I OC
Fig 1002 - Frequency Standard 1A3 (Part 2)
 ELECTRICAL AND MECHANICAL
ENGINEERING INSTRUCTIONS (AUST)

Issue 1, 31 Mar 67
FIG 1003 - RF AMPLIFIER TURRET IN RT-662/GRC
SW OF 100 KC - 10 KC TURRET IN RF AMPLIFIER RT-662/GRC
Fig 1006 - RF Amplifier 1A1
ELECTRICAL AND MECHANICAL
ENGINEERING INSTRUCTIONS (AUST)

LOW FREQUENCY MIXERS

NOTES
1. PAR' FOR
2. UNLI
3. 

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FIG 1007
NOTES:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN:
   FOR COMPLETE DESIGNATION PREFIX WITH 1A8

2. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTOR VALUES ARE IN OHMS ± 5%, 1/4W
   ALL CAPACITOR VALUES ARE IN MICROFARADS

3. □ INDICATES EQUIPMENT MARKING

A1007 - TRANSLATOR 1A8 (PART 1)
FIG 1008 - TRANSLATOR 1A8 (PART 2)
NOTES:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN.
   FOR COMPLETE DESIGNATION PREFIX WITH 1A7
2. UNLESS OTHERWISE SPECIFIED:
   a. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%
   b. ALL CAPACITOR VALUES ARE IN MICROFARADS
   c. ALL INDUCTANCE VALUES ARE IN MICROHENRIES
3. ___ INDICATES EQUIPMENT MARKING

RECEIVER IF-1A7 (PART 1)
NOTES:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH 1A10
2. UNLESS OTHERWISE SPECIFIED:
   a. ALL RESISTORS ARE IN OHMS, 5%
   b. ALL RESISTORS ARE 1/4W
   c. ALL CAPACITOR VALUES ARE IN MICROFARADS.
3. □ INDICATES EQUIPMENT MARKING
NOTES

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN:
   FOR COMPLETE DESIGNATION PREFIX WITH 1A1AG

2. UNLESS OTHERWISE SPECIFIED:
   a. ALL RESISTOR VALUES ARE IN OHMS, ±5%, 1/4W
   b. ALL CAPACITORS VALUES ARE IN MICROFARADS

Fig 1012 - Noise Blanker
NOTES

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN:
   FOR COMPLETE DESIGNATION PREFIX WITH IAIA6

2. UNLESS OTHERWISE SPECIFIED:
   a. ALL RESISTOR VALUES ARE IN OHMS, ±5%, 1/4W
   b. ALL CAPACITORS VALUES ARE IN MICROFARADS
ELECTRICAL AND MECHANICAL
ENGINEERING INSTRUCTIONS (AUST)

NOTES:
1. PARTIAL REFERENCE DESIGNATIONS ARE
   SHOWN: FOR COMPLETE DESIGNATION PREFIX
   WITH IAIA5.
2. UNLESS OTHERWISE SPECIFIED:
   a. ALL RESISTOR VALUES ARE IN OHMS
   b. ALL RESISTORS ARE 1/4W 5%
   c. ALL CAPACITOR VALUES ARE IN MICROFARADS

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NOTES:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH 1A5
2. UNLESS OTHERWISE SPECIFIED:
   a. ALL RESISTOR VALUES ARE IN OHM 1/4W, 1%.
   b. ALL CAPACITOR VALUES ARE IN MICROFARADS
3. [INDICATES EQUIPMENT MARKING]

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<th>A SERIAL</th>
<th>3-59</th>
<th>1+2, 60 UP</th>
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<td>A3 R12</td>
<td>4300</td>
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<td>A3 C1</td>
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<tr>
<td>C1</td>
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PART OF J1
4 AUTO LEVEL CONT METER

AM CARRIER SWITCH

TRANSMITTER IF AND AUDIO 1A5 (PART 1)
NOTES:
1. PARTIAL REFERENCE DESIGNATION, DESIGNATION, PREFIX WITH IA6
2. UNLESS OTHERWISE SPECIFIED, ALL RESISTOR VALUES ARE IN OHMS, ALL CAPACITOR VALUES ARE IN MFD.
3. —— INDICATES VERNIER "ON" SI
4. □ INDICATES EQUIPMENT MAINTAINABILITY

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FIG 1016 - FREQUENCY DIVIDE
TIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE SIGNATION, PREFIX WITH IAG.
LESS OTHERWISE SPECIFIED:
R RESISTOR VALUES ARE IN OHMS, .05% 1/4W.
C CAPACITOR VALUES ARE IN MICROFARADS
- INDICATES VERNIER 'ON' SIGNAL PATH
□ INDICATES EQUIPMENT MARKING

- FREQUENCY DIVIDER 1A6 (PART 1)

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<td>R6</td>
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PART OF 10KC DIVIDER A2
ELECTRICAL AND MECHANICAL
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[Diagram of a bi-stable multivibrator circuit with labels for components such as L1, R1, C1, Q1, Q2, R3, R4, R5, R6, C2, C3, etc., and a note indicating this is part of a 10KC divider A2.]

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FIG 1017 - FREQUENCY
Fig 1018 - MC SYNTHESIZER 1A7 (PART 1)
ELECTRICAL AND MECHANICAL ENGINEERING INSTRUCTIONS (AUST)

Fig 1020 - 100

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FIG 1021 - 100 KC SYNTHESIZER 1A2 (PART 2)
CHART B

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**Fig 1023 - 10 KC and 1 KC SYNTHESIZER 1A4 (PART 2)**
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Notes:
1. Partial ref designations are shown for complete designation prefix with 1A11.
2. Unless otherwise specified:
   All resistors are in ohms, 1/4W, ±5%
   All capacitors are in microfarads
3. Items shown on this Dwg. for ref only
   See figure 19 for complete function
4. ______ indicates equipment marking

4 - DC to DC Converter 1A11
CIRCUIT DIAGRAM RT-662/GMC CHASSIS (PART 2)
NOTES

1. PARTIAL DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER P
2. UNLESS OTHERWISE SPECIFIED
   a. ALL RESISTOR VALUES ARE IN OHMS
   b. ALL CAPACITOR VALUES ARE IN MICROFARADS
   c. VALUES ARE IN MICROHENrys
   d. ALL ECCENTRIC CAPACITORS ARE .001
   e. CURRENTS ARE SHOWN AS VIEWS FROM THE END END IN THE EXTREME COUNTER-CLOCKWISE
      POSITION
3. P
develops PART OF
4. NO PART OF THIS DOCUMENT MAY BE REPRODUCED OR TRANSMITTED IN ANY FORM OR BY ANY MEANS WITHOUT THE WRITTEN PERMISSION OF THE ORIGINAL OWNER OF THIS DOCUMENT
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