THE PLESSEY COMPANY LIMITED
PLESSEY AVIONICS & COMMUNICATIONS

SERVICE MANUAL

FOR

PR2250 SERIES HF RECEIVERS

Publication No 1234

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PLESSEY AVIONICS & COMMUNICATIONS
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PR2250 SERIES HF COMMUNICATIONS RECEIVERS

SERVICE MANUAL

CONTENTS LIST

WARNINGS

MOS CIRCUIT DEVICES

1. THIS EQUIPMENT CONTAINS MOS INTEGRATED CIRCUITS. THESE CAN EASILY BE DAMAGED BY VOLTAGES GENERATED BY ELECTROSTATIC CHARGES. PROTECTION IS ESSENTIAL DURING ALL STAGES OF HANDLING (INCLUDING TRANSPORT AND STORAGE) UNTIL THE ITEM IS FINALLY INSTALLED ON A PRINTED-CIRCUIT PANEL.

2. THE FOLLOWING RULES ARE RECOMMENDED WHEN HANDLING MOS COMPONENTS:

   (1) PACKING — PACK IN A CONDUCTIVE PACKAGE WITH ALL LEADS SHORTED TOGETHER.

   (2) CLOTHING — PERSONNEL HANDLING MOS DEVICES SHOULD WEAR COTTON OUTER CLOTHING. THEY SHOULD NOT WEAR OUTER CLOTHING OF MAN-MADE FIBRES SUCH AS NYLON.

   (3) EQUIPMENT — ALL WORKBENCH EQUIPMENT SHOULD BE EARTHED TO ONE POINT. IDEALLY, THE TOP OF THE BENCH SHOULD BE OF EARTHED CONDUCTIVE MATERIAL.

   (4) SOLDERING — USE A TEMPERATURE-CONTROLLED IRON SET TO A TEMPERATURE NO HIGHER THAN 315°C (600°F).

A.C. SUPPLY

THE A.C. POWER SUPPLY CABLE HAS THREE CORES, COLOURED BROWN, BLUE AND GREEN/YELLOW. THESE COLOURS ARE THE CURRENT BRITISH STANDARD, INDICATING:

LINE (U.S. 'PHASE')	:	BROWN
NEUTRAL (U.S. 'COMMON')	:	BLUE
EARTH (U.S. 'GROUND')	:	GREEN/YELLOW

THE SYSTEM IS INTENDED FOR USE WITH A SUPPLY WHERE THE NEUTRAL IS EARTHED AT THE GENERATING STATION. SINGLE-POLE ON-OFF SWITCHES ARE ALWAYS CONNECTED IN THE BROWN (LINE) CORE. THE GREEN/YELLOW CORE SHOULD BE CONNECTED TO EARTH VIA A CABLE OF RESISTANCE LESS THAN 0.5 OHMS: THIS IS A POWER-SUPPLY SAFETY EARTH AND WILL NOT NECESSARILY ACT AS AN R.F. SIGNAL EARTH.

NO RECEIVER OF THE PR2250 SERIES IS FITTED WITH AN A.C. POWER ON-OFF SWITCH. A RECEIVER IS THEREFORE POWERED WHENEVER A.C. POWER IS PRESENT AT PL1 OF MODULE 8A. RECEIVERS SHOULD BE CONNECTED TO THE A.C. SUPPLY VIA AN EXTERNAL ON-OFF SWITCH COMPLYING WITH THE CURRENT LOCAL REGULATIONS APPLICABLE TO THE CUSTOMER'S INSTALLATION.

DO NOT WITHDRAW A RACK-MOUNTED RECEIVER WITHOUT FIRST BREAKING THE EXTERNAL A.C. POWER SWITCH AND REMOVING PL1 FROM MODULE 8A.

A 70V D.C. POTENTIAL IS FED FROM MODULE 8A TO MODULE 9. ALL A.C. POWER SUPPLY VOLTAGES ARE CONTAINED WITHIN MODULE 8A. NO OTHER DANGEROUS VOLTAGES ARE EMPLOYED.

TECHNICAL SUMMARY

Frequency Range:

10kHz to 29.99999MHz continuous coverage in 10Hz steps. Synthesiser allows tuning down to zero.

Modes of Reception:

CW(A1), AM(A2,A3), USB(A3A,A3H,A3J), LSB(A3A, A3H,A3J), ISB(A3B), FSK(F1) with external demodulator.

Frequency Stability:

Temperature:	1×10^{-7}	from 0°C to 50°C (32°F to 122°F)
Time:	2×10^{-8}	max. per 24 hours.
	1×10^{-6}	max. per year.

Bandwidths:
(PR2250A, B, E & F have all first 5: PR2250C, and D omit the 8kHz and 100Hz filters)

Filter	3dB points	6dB points	60dB points
8kHz	-	fo ± 4kHz	fo ± 10kHz
6kHz	fo ± 3kHz	-	fo ± 6kHz
1.2kHz	fo ± 600Hz	-	fo ± 1.8kHz
300Hz	fo ± 150Hz	-	fo ± 1.2kHz
100Hz	fo ± 50Hz	-	fo ± 300Hz
USB	(fo + 3kHz	-	fo + 3.9kHz
	(fo + 250Hz	-	fo - 650Hz
LSB	(fo - 250Hz	-	fo + 650Hz
	(fo - 3kHz	-	fo - 3.9kHz

Sensitivity:

Mode	$\frac{S+N}{N}$	Input	Bandwidth
SSB	15dB	1uV e.m.f.	3kHz
AM	10dB	3uV e.m.f. (30% mod.)	8kHz

Sensitivity drops below 100kHz;
SSB 3dB $\frac{S+N}{N}$ at 20kHz is typical.

Tuning speed:

Typically 10mS (20mS max.) for any frequency change.

Tuning:

(1) Continuous tuning from 10kHz to 29.99999MHz in 10Hz steps by synthesiser operated from optical encoder.

(2) Control rate selectable at either 1kHz or 20kHz per control knob revolution.

(3) Frequency setting to any point by digital key-pad.

(4) Frequency readout by digital LED display.

Tuning Accuracy:

Minimum frequency change is 10Hz.

A.G.C.:

Less than 4dB change in output level for 120dB change in input level from A.G.C. threshold of 1uV e.m.f.

A.G.C. Time-constant:

Attack time-constant fixed, between 5 and 10mS. Decay time-constant is operator selectable from 10 sec., 2 sec., and 0.2 sec (nominal).

B.F.O:	(1) Variable over ± 8kHz in CW mode. (2) Fixed in F mode, providing an offset frequency preset in 100Hz steps by internal links.
R.F. Input:	50 ohms. Can accept up to 5V r.m.s. continuous or 30V r.m.s. for up to 15 minutes without damage.
I.F. Output:	100kHz, 100mV into 50 ohms. Two isolated outputs are available.
Audio Outputs:	(1) 1 watt internal loudspeaker. (2) Two headphone jack sockets, 600 ohm, 20mW level. (3) 2 watt 4/8 ohm external speaker line. (4) Two line outputs, 600 ohm, 10mW level (When working in ISB mode, one is USB and the other is LSB).
Audio frequency response:	Less than 2% distortion, with hum modulation at least 50dB down.
Meter Indications:	(1) AF:- Audio output level (2) RF:- Input level on dBuV (3) LO(2):- 2nd LO drive (4) LO(1):- 1st LO drive (5) ZERO BEAT (6) DC Supplies:- 'coloured band' meter indications of output levels from P.S.U.
Spurious Responses:	(1) External:- greater than 80dB rejection. (2) Internal:- less than 0.3uV e.m.f. equivalent.
Blocking:	With the receiver tuned to any frequency between 100kHz and 30MHz and a wanted signal of 1mV, the level of an unwanted signal at least 20kHz removed which will reduce the output by 3dB greater than 1V e.m.f.
Cross-modulation:	Better than -20dB for interfering signals at least 20kHz removed and of greater than 0.5V e.m.f.
Inter-modulation products:	(1) In Band:- Line output better than 35dB down; IF output better than 60dB down. (2) Out of Band:- Interfering signals of 32mV e.m.f. (90dBuV) at least 20kHz removed produce intermodulation products of less than 1uV e.m.f. at the tuned frequency.

Desensitisation:	With an unwanted signal at least 20kHz removed and of 30mV e.m.f., no more than 1uV e.m.f. of noise is produced in a 3kHz bandwidth.
Synthesiser frequency purity:	Incidental FM is less than 1Hz r.m.s.
Re-radiation:	Less than 15uV at 1st L.O. frequency into an antenna load of 50 ohms.
Power Requirements:	105 to 130V or 200 to 250V, 45 to 450Hz, single-phase. Power consumption 65VA approx.
Environment:	(1) Operation:- 20°C to 55°C (-4°F to 131°F), 95% R.H.
	(2) Storage:- -40°C to +70°C (40°F to 158°F), 95% R.H.
Dimensions and Weight:	Width:- 440 mm (17 3/8 ins) Height:- 178 mm (7 ins) Depth:- 460 mm (18 1/8 ins) Weight:- 20kg (44lb)

AMENDMENT RECORD SHEET

To record the incorporation of an amendment list in this publications, sign against the appropriate A.L. No. and insert the date of incorporation.

A.L. No.	AMENDED BY	DATE
1	On reprint.	May 80
2		July 80

A.L. No.	AMENDED BY	DATE

MODIFICATION RECORD

1. Each of the items listed below bears a Modification Record Label which can be used to indicate the build standard of the item. Incorporation of a modification to an item is recorded by crossing out the appropriate number (strike-off number) on its Modification Record Label.

2. The modifications listed below are all incorporated in the contents of this manual.

MODULE	MODIFICATION STRIKE-OFF
1	1
1A	0
2	0
3	0
3A	0
4	0 (Oman). 1
5	0
6	0
7A	0
8A	0
9	0
10A	0
10B	0
11	0
12	0
Interface	0
Case Assy.	0

CHAPTER 1

GENERAL DESCRIPTION

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ILLUSTRATIONS

1. INTRODUCTION

1.1 Each of the PR2250 series of double-superhet communications receivers provides continuous coverage of the frequency range 10kHz to 30MHz, and allows for the reception of AM, CW, SSB, ISB, and FSK signals. The synthesiser BFO can be internally set in 100Hz steps to accommodate frequency offsets up to 8kHz.

1.2 A conventional tuning control provides continuous fast or slow frequency control without any need for band-changing. In addition, a keypad provides for instant frequency access as required. Instant recall of up to sixteen frequencies, together with their respective mode, bandwidth, and a.g.c. settings, is also provided.

1.3 The series comprises three basic versions; PR2250 receivers are operator-controlled, PR2251 receivers are 'slave' equipments intended for use in such applications as diversity reception, and PR2252 receivers are for use under remote control only. Variants of these three versions are identified by a letter suffix to the type number, and are produced by combinations of alternative RF Amplifier filters and IF bandwidth filters. Table 1 defines the full series at the date of publication.

TABLE 1 : PR2250 SERIES

Rx TYPE	FRONT-PANEL CONTROLS	REMOTELY CONTROLLABLE	RF AMP FILTERS	IF BAND-WIDTH FILTERS	
PR2250 (A	FULL OPERATOR FRONT-PANEL CONTROL	NO	SELECTABLE SUB-OCTAVE FILTERS FIXED LOW-PASS FILTER	FIVE	
PR2250 (B		YES			
PR2250 (C		NO		THREE	
PR2250 (D		YES			
PR2250 (E		NO		FIVE	
PR2250 (F		YES			
PR2251 (A	FEW CONTROLS ONLY	'SLAVE' Rx	SELECTABLE FIXED LOW-PASS FILTER	FIVE	NO INTERNAL LOCAL OSC. OR FREQ. STANDARD FITTED IN PR2251
PR2251 (B				THREE	
PR2251 (C				FIVE	
PR2252 (A	FEW CONTROLS ONLY	YES	SELECTABLE FIXED LOW-PASS FILTER	FIVE	
PR2252 (B				THREE	
PR2252 (C				FIVE	

1.4 The PR2250 series receivers are 7 ins (178 mm) high, 19 ins (483 mm) wide, and 18 ins (458 mm) deep from front to back. They may be used free-standing or rack-mounted. Weight is 48.5 lb (22 kg). They operate from a 100-125V or 200-250V single-phase a.c. power source of 45-450Hz, and consume approximately 65VA. A 50 ohm antenna is required. Headphone, line, and internal speaker audio outputs are produced by PR2250 models.

1.5 The receivers are made up from plug-in modules mounted in a case. The front panel and its associated control circuit panel also form a removeable module. All modules form functional entities, and all can be changed without workshop facilities. All modules can be removed and replaced without using tools.

2. BASIC TECHNICAL DESCRIPTION (Fig.1)

2.1 The received signal from the antenna is filtered in Module 1; according to the particular variant, this is carried out by either a fixed low-pass filter or by one band-pass filter selected from a band of nine. Selection is automatic, linked to the receiver tuning control.

2.2 After filtering, the received signal is applied via a wide-band a.g.c.-controlled amplifier to the first mixer (in Module 2). The 1st local Oscillator input to this mixer is provided by a synthesiser in Module 9, which produces a variable-frequency output of stability equal to the crystal frequency standard in Module 7A. PR2251 receivers do not have Modules 7A and 9: their local oscillator inputs are provided by the associated PR2250 'master' receiver. Frequency control is exercised via the logic in Module 10, either from the front-panel tuning controls or from (in some models) a remote position by digital commands.

2.3 The 65MHz 1st IF output from Module 2 is amplified and applied to the second mixer (in Module 3). The 2nd local oscillator frequency is fixed at 63.6MHz, and is also supplied by the synthesiser in Module 9. In a PR2251 receiver, it is supplied by the associated PR2250 'master' receiver. The 1.4MHz 2nd IF output is selected by one of a band of five (three in some models) crystal filters which, under front-panel (or remote) control, determine reception bandwidth.

2.4 The filtered 2nd IF signal is amplified by an a.g.c.-controlled circuit in Module 4, and applied to the detector circuits. The signal detectors are contained in Module 5, while the a.g.c. detector is contained in Module 4. The decay time constant of the a.g.c. is operator-variable.

2.5 The signal detectors consist of an envelope detector (used in AM mode) and two product detectors (use in F, CW, and SSB modes). The appropriate detector is selected by the operator's 'MODE' control. The product detectors are fed with an input from the BFO in Module 6; this input can either be:

(a) Locked to the crystal frequency standard in Module 7.

(b) Varied over ± 8kHz by the front-panel 'BFO' control.

(c) Locked to an incoming pilot carrier.

For 'F' mode (fixed offset), the BFO fixed offset value is preset by switches in Module 6. The offset can be changed to suit individual operational requirements.

2.6 The detected output signal is applied to circuits in Module 5 which produce the following outputs:

(a) Two audio 'line' outputs.

(b) A 100kHz 'IF' output.

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PR2250 (D)		YES			
PR2250 (E)		NO		FIVE	
PR2250 (F)		YES			
PR2251 (A)	FEW CONTROLS ONLY	'SLAVE' Rx	SELECTABLE FIXED LOW-PASS FILTER	FIVE	NO INTERNAL LOCAL OSC. OR FREQ. STANDARD FITTED IN PR2251
PR2251 (B)				THREE	
PR2251 (C)				FIVE	
PR2252 (A)	FEW CONTROLS ONLY	YES	SELECTABLE FIXED LOW-PASS FILTER	FIVE	
PR2252 (B)				THREE	
PR2252 (C)				FIVE	

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2.6 The detected output signal is applied to circuits in Module 5 which produce the following outputs:

(a) Two audio 'line' outputs.

(b) A 100kHz 'IF' output.

(c) A front-panel headphone output.

(d) A build in speaker output.

2.7 Function control is completely digital on all models and is exercised by the circuits in (according to model) Module 10, 10A, or 10B. Audio Gain, BFO, and RF-IF Gain are analogue control. Front-panel tuning is carried out by setting the frequency in on a keypad, and then tuning 'around' by means of a normal 'feel' manual tuning control driving an optical encoder. Frequency read-out is by 7 segment LED display indicating to 10Hz.

2.8 A maximum of sixteen settings of frequency, bandwidth, mode, and a.g.c. decay time-constant can be stored in the memory circuits of Module 11 or 12 (according to model) for use at any time. Models employing Module 12 can be remotely controlled by digital commands: models employing Module 11 cannot be remotely controlled.

2.9 Slave receivers (PR2251) do not contain either Module 11 or Module 12, nor do they contain Synthesisers (Module 9) or frequency standards (Module 7).

2.10 All PR2250 series receivers are housed in identical frames. Seven modules plug in from the front, and three from the back. The front panel (Module 10) is hinged to the front of the frame.

2.11 The front panel is in two parts. The panel itself is hinged to the frame. The associated printed-circuit panel is hinged to the back of the front panel so that, when the front panel is open, the p.c. panel can swing downward to permit access to the rear of the front panel and the track side of the p.c. panel.

2.12 Connections between Module 10 and the remainder of the receiver are made by (according to model) a maximum of three flat flexible cables. One plugs into Module 11 or 12 (according to model) while the others plug into connectors on the frame.

3. OPERATION

Operating instructions are contained in the Operator's handbook which is supplied with the receiver.

CHAPTER 1

INITIAL CHECKS AND INSTALLATION

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INITIAL CHECKS AND INSTALLATION

1. RECEIVING CHECK

On receipt check the equipment for any physical damage which may have occurred in transit. Release the two quick-release fasteners at the left-hand side of the front-panel, and swing the panel open. Release the catch at the left-hand side of the module-retaining plate, and swing the plate open. Check that all modules are firmly in place, and that all inter-module plugs and sockets are correctly mated. A list of the co-axial connections is given in Tables 1-1 and 1-2 of this chapter. Check at the back of the receiver that Module 8A (Power Supply Unit) and, if fitted, Module 7 (Frequency Standard) are securely in place. Open the door at the rear and check that, if fitted, Module 9 (Synthesiser) is securely in place. Close and secure the rear door, the module-retaining plate, and the front-panel.

2. ELECTRICAL CONNECTIONS

2.1 Power Supply

2.1.1 A 2m (6ft. 6ins.) length of 3-core power cable is supplied with the receiver, having at one end a moulded free socket which connects to the receiver. The three cores are coloured brown, blue, and green/ yellow. This colouring is the British Standard, indicating:

Earth (ground)	:	green/yellow
Live (phase)	:	brown
Neutral (common)	:	blue

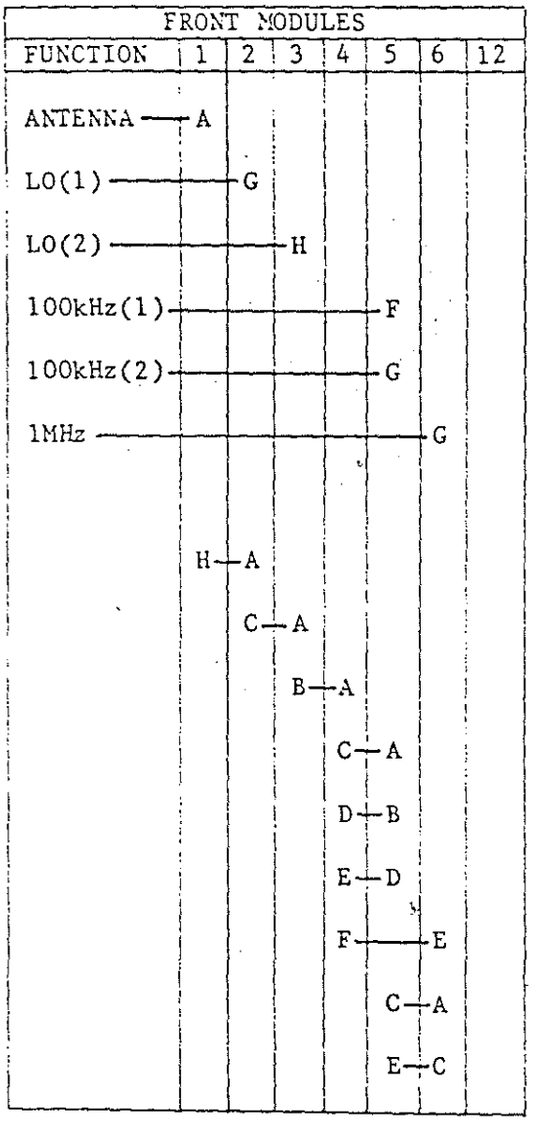
These connections are valid in all places which use an a.c. distribution system with one side (neutral) connected to earth at the generating station. Elsewhere, the brown and blue lines have no separate significance and form the two a.c. supply lines. The green/yellow line must always be connected to earth via as low a resistance as possible to form the power supply safety earth connection: note that this will not necessarily form an r.f. earth.

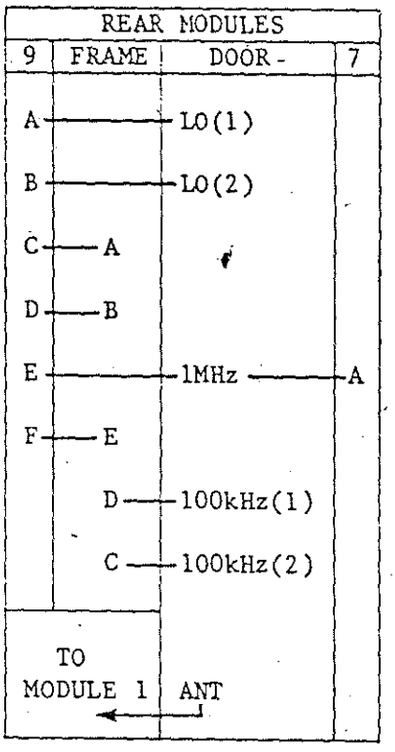
2.1.2 The receiver can be operated from a 45 to 450Hz a.c. supply between either 100V and 125V or between 200V and 250V. Receivers are usually shipped from the factory set for 240V. Before applying power, set the power selector plug on Module 8A (at the back of the case) to the voltage of the local a.c. supply and check that power fuse FS1 (near the power selector plug) is correctly rated for the local supply. Fuse types and ratings are:

FS1	:	1A 'slow-blow' for 200-250V a.c. supply
		2A 'slow-blow' for 100-125V a.c. supply
FS2	:	3A)
FS3	:	3A) Ratings do not change with
FS4	:	1.6A 'slow-blow') a.c. supply voltage.
FS5	:	100mA 'slow-blow')

Finally, connect the power cable between the receiver and the a.c. supply.

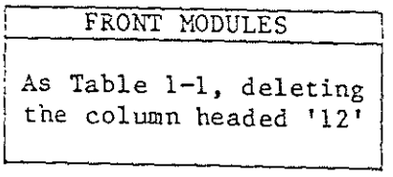
TABLE 1 : PR2250 AND PR2252 INTERMODULE CO-AXIAL CONNECTORS

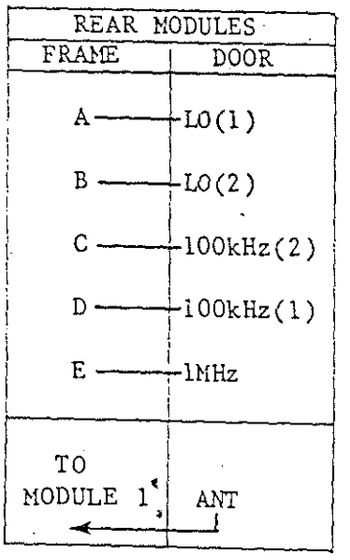




NOTE: Sockets are lettered A to H downward in relation to physical position; e.g. the two sockets on Module 1 are A and H.

TABLE 2 : PR2251 INTERMODULE CO-AXIAL CONNECTORS





2.2 Antenna (Aerial)

Connect a receiving antenna of 50 ohms impedance to the co-axial socket marked AERIAL at the back of the receiver.

2.3 '1MHz STANDARD' Link

Check that the co-axial link on the back of the receiver between socket A on Module 7 and the 1MHz STD socket is in place on PR2250 and PR2252 models. On PR2251 models, the 1MHz STD input is supplied from either the master receiver or from an external standard source.

2.4 LO(1) and LO(2) Output Sockets

On PR2251 models these are connected to the corresponding sockets on the master PR2250 or PR2252 receiver to provide local oscillator inputs. When unused, these sockets must always be terminated by 50 ohm terminating plugs: failure to do so will increase the re-radiation from the receiver and will cause spurious signal response.

2.5 '100kHz IF' Output

If the installation requires 100kHz outputs from the receiver, these are taken from the two '100kHz IF' co-axial sockets.

2.6 Remote Control

2.6.1 Remote control of a PR2250 or a PR2252 receiver is exercised via Module 12 by means of a serial digital data input to RS232C standard. The receiver address (which forms part of the serial data input) is also hard-wired at the CONTROL socket. A data output is provided for check purposes. An external negative supply is necessary if input or output logic levels below 0V are employed.

2.6.2 The standard input and output logic levels employed $\pm$6V; -6V = logic '1' and +6V = logic '0'. The levels are adjustable by means of switches inside Module 12, and can be set to any required levels up to $\pm$12V provided that logic '0' is always greater than +3V and logic '0' is always 0V or negative. The acceptable input data rate is selectable by switches inside Module 12: it can be set to 600, 1200, 2400, or 4800 bauds.

2.6.3 The standard serial data format employed is 12-bit asynchronous ASCII code, in which each 12-bit word consists of 1 start bit, 8 data bits, 1 parity bit, and two stop bits. Odd, even, or no parity can be selected by switches inside Module 12.

2.6.4 Provision can be made, by re-programming the PROM in Module 12, for other serial data formats.

2.6.5 All receivers which are remotely controlled from one point are connected to a parallel data bus. Each has its individual address hard-wired into the plug which mates with its CONTROL socket, and will only react to a data stream containing its own address. The addresses, therefore, are specific to particular receiver bays in which any individual receiver of the correct type can be installed.

2.6.6 Connections to the 50-way Cannon CONTROL socket at the back of the receiver are:

Data from modem	pin 23
Data out to modem	pin 22
Common	pin 17
External negative supply	pin 24
Address (Binary weight 1)	pin 27
Address (Binary weight 2)	pin 28
Address (Binary weight 4)	pin 29
Address (Binary weight 8)	pin 30
Address (Binary weight 16)	pin 31
Address (Binary weight 32)	pin 32

The voltage of the external negative supply shall be equal to the negative voltage of the logic '1' level: if logic '1' = 0V, connect pin 24 to 0V. An address line left open-circuit produces a logic '1' level; an address line connected to 0V produces a logic '0' level.

2.7 Master-Slave Operation

Where a PR2250 or PR2252 receiver is used as a master to a PR2251 slave receiver, the following external connections are made:

(1) Parallel the CONTROL sockets on the two receivers.

(2) Parallel the LO(1) and LO(2) sockets on the two receivers.

(3) Connect the 1MHz STD socket on the PR2251 to SKB of Module 7 on the PR2250 or PR2252.

2.8 Terminal Strip Connections

2.8.1 All connections on the terminal strip at the back of the receiver are made by 4BA pan-head machine-screws (3.6 mm (0.142 ins.) diameter, 38.5 TPI). Terminal tags having a 3.7 mm (or No.26 drill) hole or fork spacing should be employed.

2.8.2 A.G.C.

The A.G.C. terminal is used where external monitoring of the a.g.c. voltage is required.

2.8.3 A.G.C. SLOW

The A.G.C. SLOW output is a slow time-constant a.g.c. voltage which is used where it is required to slave the a.g.c. control of one receiver to another. Details can be found in Chapter 4 of Section 4, 'Module 4 Circuit Description'.

2.8.4 Muting

The MUTE terminal is used where it is necessary to mute the receiver on command from a remote installation. An earth connection to the MUTE terminal mutes the receiver.

2.8.4 External Speaker

An external speaker output of 2 watts maximum is available to feed a load of between 4 and 8 ohms connected between EXT LS and GND.

2.8.6 Phones

An external headphone output of 20 milliwatts maximum is available to feed a load of 200 ohms connected between PHONE and GROUND.

2.8.7 600 ohm Line Outputs

Two floating line outputs of 10 milliwatts maximum into 600 ohms are available, one from LINE O/P 1 and one from LINE O/P 2. Each output has independent level adjustment, situated on the front panel of Module 5.

CHAPTER 2

PERFORMANCE CHECKS

CONTENTS

1. FUNCTIONAL TESTS

1.1 Introduction

The tests described in this chapter are in two parts. The first covers a complete receiver, and rapidly checks that no major fault exists. The second also covers the complete receiver, and provides a detailed performance check. The required test equipment is listed in terms of performance rather than in terms of manufacturers, to cater for what is easily available in different countries.

1.2 Test Equipment

The following test equipment is required to carry out the tests from paragraph 2 onward. The tests in paragraph 1.3 do not required any test equipment.

(1) Two RF Signal generators, each producing a synthesised output over the range from 1000kHz to 30MHz, capable of being set to output levels between 1uV and 1V. CW and AM outputs are required, the AM output to be modulated 30% at 1kHz. The two generators are only required together for the 'intermodulation product' and 'reconstituted carrier' checks.

(2) A Distortion factor meter of 600 ohm input impedance. This is only used as a distortion-factor meter for a few 'SINAD' measurements (see para.2.5.2): it is used at other times as an output meter. If a distortion-factor meter is not available, the majority of the tests can be carried out by using an Output Meter of 600 ohm input impedance which is calibrated in dBm.

(3) An RF Millivoltmeter capable of giving readings from 1 to 100mV over the frequency range 1000kHz to 30MHz.

(4) Two buffer-isolator amplifiers for use with the two signal generators when they are used together. These items are available as optional test equipment, Plessey part number 630/.

(5) A 50 ohm hybrid transformer capable of handling signals from 100kHz to 40MHz.

(6) A variable attenuator capable of variation in 1dB steps from 0dB to 100dB, and of 50 ohms impedance.

1.3 Preliminary Functional Test (no test equipment required)

1.3.1 Carry out the following procedure to check that the receiver is functioning and that no major faults exist. The tests are written for a standard PR2250 receiver (which has full front panel controls) but can be adapted to cover non-standard versions or a PR2251 slave receiver or a PR2252 remote control receiver. For a PR2251, carry out the control operations on the associated PR2250 master receiver and check the results obtained on the PR2251 slave. For a PR2252 carry out the control operations at the remote control point, and check the results obtained on the receiver.

(1) Set POWER to ON and CONTROL to LOCAL. Check that d.c. supplies and LO1 and LO2 meter readings are in the red band.

(2) Connect an antenna to the receiver. For these tests, a short length of wire should be adequate.

(3) Using the keypad, enter the frequency of your local AM broadcast station.

(4) Select AM mode, and check that 6kHz bandwidth is automatically selected.

(5) Select a.g.c. SHORT. Turn the RF-IF GAIN control fully clockwise. Turn the AUDIO GAIN half-way to maximum.

(6) Switch speaker to ON. The broadcast station should now be heard. Adjust AUDIO GAIN over its range, and check for satisfactory operation. Plug in a headset, and check that both sockets produce an audio output.

(7) Select in turn each bandwidth. Check that all are functioning. Little or nothing will be heard on 0.3 and 0.1 bandwidths.

(8) Select CW, and check that 300Hz bandwidth and XTAL are automatically selected. Vary the VARIABLE BFO control and check that the audio tone varies accordingly. Select AF on the meter switch, and adjust the VARIABLE BFO control for the null reading corresponding to no audio tone. Leave the VARIABLE BFO control in this position.

(9) Select USB and check that no bandwidth is automatically selected. Check, by depressing each bandwidth button in turn, that no bandwidth can be selected. The LEDs should illuminate only while the buttons are depressed. Check that an audio output is still present.

(10) Switch the monitor meter to ZERO BEAT and check that a beat indication is present. Select in turn SLOW and FAST tuning rates and set the tuning switch to OPERATE. Check the operation of the VARIABLE TUNING control. Set the tuning switch to INHIBIT and check that the VARIABLE TUNING control is now inoperative.

(11) Select ISB, then select in turn LSB and USB on the ISB AUDIO switch. Check that an audio output is present on both settings.

(12) Tune 50Hz (50 cycles only) off the broadcast station frequency. Select RECON.CAR. and check that the audio is then corrected in frequency. Return the tuning to the original setting.

(13) Select F, and check that 1.2kHz bandwidth and XTAL are automatically selected. Check that a 2.5kHz (or the offset which has been set up) audio tone is present.

(14) Set the power switch to STANDBY and then back again to ON. Check that the control settings have not changed.

(15) Note the displayed memory channel number, depress and release increment INCR button, channel number shall be increased by 1 count, repeat until all 16 have been displayed sequentially. Depress INCR button and hold depressed, the memory channel number shall increase by 1 count at a rate of between 0.5 and 1 sec. per increment.

(16) Depress CLEAR, enter in new frequency 17777.77 (ENTER), store in Channel 15 by selecting 15 on Channel Switch, depressing 'Channel

Select' (note that LED above illuminates) and then 'Store' (check that LED extinguished). Depress CLEAR, enter in frequency 28888.88, store in Channel 14. Select Channel 15, depress 'Channel Select', 'Recall' and settings 17777.77 'F', etc., should be selected. Select Channel 14, depress 'Channel Select', 'Recall' and settings 28888.88, 'F', etc., should be selected. Enter in new frequency 23456.89 (ENTER), Mode AM and store in Channel 15, by selecting 15 on channel switch.

(17) Set in on the keypad the frequency of the local AM broadcast station. Select AM and a.g.c. SHORT. Check for monitor meter readings on AF and RF switch positions.

(18) Select REMOTE and check that all front-panel controls are inoperative. Select LOCAL.

(19) Select a.g.c. LONG. Set the meter switch to RF and, while watching the meter, remove the antenna. Check that the meter reading falls slowly, taking about 10 seconds to pass through 40 divisions. Re-connect the antenna.

(20) Select a.g.c. MED, and check as in step (19). The meter reading should fall 40 divisions in about 2 seconds. Re-connect the antenna.

(21) Select a.g.c. SHORT, and check as in step (19). The meter reading should fall rapidly. Re-connect the antenna.

(22) Select a.g.c. OFF. With the meter switch set to RF check that the meter reading increases as the RF-IF GAIN control is turned anti-clockwise. When the control is fully anti-clockwise, the reading should be full-scale.

(23) Set in '00000. ENTER' on the frequency keypad. Set the VARIABLE TUNE switch to OPERATE, and select SLOW. Swing the manual tuning knob to tune either side of the set reading. Check that the display reading jumps from 0000000 to 2999999.

1.3.2 An 'interrupted mains'soak test may now be performed. Tuned to the local broadcast station, the receiver is connected for 24 hours to an a.c.power supply which cycles ON for one minute then OFF for 6 minutes. At the end of this test, the receiver should pass the tests of paragraph 1.3.1.

1.3.3 If the receiver checks out correctly on these tests, the detailed testing and setting up given in the following paragraphs may be carried out. If it does not check out correctly, locate and repair the fault before attempting further tests.

2. PERFORMANCE CHECKS AND ADJUSTMENTS

2.1 BFO

Set in a frequency of 00000. Set the meter switch to AF, and adjust the VARIABLE BFO control for the sharp null in the audible beat note. If the null does not occur with the white line on the knob coincident with the white line on the front-panel, fit Module 6 on the extender card of the Servicing Kit. Having done so, set the BFO control with the line on the

knob coincident with the line on the panel and adjust C57 in Module 6 for a null in the beat note. Check that the adjustment remains correct after the adjusting tool is removed from C57.

2.2 Gain, AGC, 100kHz IF and Mode Balance

2.2.1 For these four procedures connect the RF Signal Generator output to the antenna input socket of the receiver. Connect the Distortion-factor meter* to the LINE O/P1 terminals of the rear tag-strip. Ensure that the input impedance (if variable) of the Distortion-factor meter is 600 ohms. Set the receiver to 15500kHz, USB, AGC OFF. Set the signal generator output frequency to 15501kHz at a level of 1uV.

*In any test which does not specifically call for 'SINAD' measurements, a 600 ohm input-impedance output meter calibrated in dBm may be used in place of the Distortion-factor meter. The Distortion-factor meter is called up through the tests only to make then a 'one set-up' series.

2.2.2 Overall Gain

With the equipment set up as in paragraph 2.2.1 open the front-panel and set Module 4 on the extender card. Connect the RF Millivoltmeter in parallel with a 50 ohm load to SKD on Module 4. Adjust R8 in Module 4 to give a 9mV reading on the Millivoltmeter.

2.2.3 A.G.C. Threshold

With the equipment set up as in paragraph 2.2.1 select a.g.c. SHORT and increase the RF Signal Generator output level by 10dB. With the RF Millivoltmeter connected as in paragraph 2.2.2, adjust R112 in Module 4 to give a 10mV reading on the Millivoltmeter. Repeat the procedure on AM, adjusting C15 to achieve 9mV at SKC on Module 4. Replace Module 4 in its normal position and disconnect the Millivoltmeter.

2.2.4 100kHz IF

With the equipment set up as in paragraph 2.2.1, connect the RF Millivoltmeter in parallel with a 50 ohm load to either of the 100kHz IF O/P sockets on the rear panel. Set the Signal Generator output level as in paragraph 2.2.3. Check that a Millivoltmeter reading of 100 $\pm$ 25mV is obtained. If the reading is outside these limits, set Module 5 on the extender card and adjust R42 to produce a correct reading.

2.2.5 Mode Balance

With the equipment set up as in paragraph 2.2.1, set the signal generator output level to 1mV, amplitude modulated 30% by a 1kHz tone and carry out the following six steps:

(1) Adjust R68 on Module 5 front-panel to produce a Distortion-factor meter reading of 0 $\pm$ 0.2dBm.

(2) Select USB mode and ISB AUDIO. Set the meter switch to AF and check that a reading of 30 $\pm$ 5 is obtained.

(3) Connect the Distortion-factor meter across the LINE O/P No.2 terminals of the receiver. Adjust R69 on Module 5 front-panel to give a reading on the Distortion-factor meter of 0 $\pm$ 0.2dBm.

(4) Select LSB and ISB AUDIO. Set the meter switch to AF and check that a reading of 30 ± 5 is obtained.

(5) Select USB and XTAL. Set the Signal Generator to 15501kHz CW. Check that the Distortion-factor meter reads 0 ± 0.5dBm and adjust R22 on Module 5 if necessary to obtain this reading.

(6) Select LSB and XTAL. Set the Signal Generator to 15499kHz. Check that the Distortion-factor meter reads 0 ± 0.5dBm and adjust R24 in Module 5 if necessary to obtain this reading.

2.2.6 A 72-hour 'soak' test may now be performed with the a.c. power continuously applied. After this period the receiver should pass the tests in paragraph 1.3.1.

2.3 Sensitivity and Distortion

2.3.1 Set the receiver to 15500kHz, AM, 6kHz, and a.g.c. SHORT. Set the RF signal generator to 15500kHz, at a 3uV output level 30% AM modulated at 1kHz. In the following tests 'SINAD' measurements are taken with the Distortion-factor meter. A 'SINAD' measurement is a measurement of:-

$$\frac{\text{signal + noise + distortion}}{\text{noise + distortion}}$$

2.3.2 AM

Connect the signal generator to the receiver antenna input, and connect the Distortion-factor meter to the LINE O/P No.1 terminals of the rear tag-strip. Ensure that the input impedance (if variable) of the Distortion-factor meter is set to 600 ohms. Check that the 'SINAD' reading shown on the Distortion-factor meter is not less than 10dB. Set receiver bandwidth to 8kHz, Module 3 only, and check that the meter reading is not less than 9dB.

2.3.3 Increase the signal generator output level to 10mV and repeat the tests given in 2.3.2 with bandwidth set to 6kHz. Check that the 'SINAD' reading is not less than 34dB, assuming that the signal generator in use produces an AM signal which is free from distortion.

2.3.4 Set the signal generator to produce a CW output, and repeat the test given in 2.3.3. Check that the 'SINAD' reading is not less than 45dB.

2.3.5 SSB and Dynamic Range

Connect up the receiver, Signal Generator and Distortion-factor meter as in paragraph 2.3.2. Set the receiver to 15499kHz, USB, a.g.c. SHORT, and XTAL. Set the signal generator output to 15500kHz CW at a level of 1uV.

2.3.6 Check that the 'SINAD' reading on the Distortion-factor meter is not less than 15dB. Increase the signal generator output level to 1V, and check that the 'SINAD' reading is not less than 34dB. Check that the audio line output level reading on the Distortion-factor meter is not more than +4dBm.

2.3.7 Set the receiver to LSB, and tune to 15501kHz. Set the signal generator output level to 30uV. Check that the 'SINAD' reading is not less than 34dB. Reduce the signal generator output level to 1uV, and check that the 'SINAD' reading is not less than 15dB.

2.3.8 CW and BFO Range

Connect up the receiver, signal generator, and Distortion-factor meter as in paragraph 2.3.2. Set the receiver to 15500kHz, CW, 300Hz, and a.g.c. SHORT.

2.3.9 Adjust the VARIABLE BFO control to produce a 1kHz audio tone: this can be measured either by connecting a frequency counter to the receiver audio output or by 'notching out' the response on the Distortion-factor meter. Check that the 'SINAD' reading is not less than 18dB. If the receiver contains Module 3 (as opposed to 3A), select 100Hz bandwidth and check that the 'SINAD' reading is then not less than 26dB.

2.3.10 Set the VARIABLE BFO control fully clockwise. Measure the audio tone frequency by either of the methods suggested in paragraph 2.3.9. Check that the frequency is not less than 8kHz. Repeat the test with the control set fully anti-clockwise: the same frequency should be obtained. Return the VARIABLE BFO control to a position giving an approximate 1kHz tone.

2.3.11 Loudspeaker Amplifier Distortion

Connect the signal generator to the antenna input of the receiver, and connect the Distortion-factor meter across the EXT L/S and GND terminals of the receiver. Set the receiver to 10499kHz, USB, XTAL, and a.g.c. SHORT.

2.3.12 Set the signal generator frequency to 10500kHz CW and the output level to 1mV. Adjust the receiver AUDIO GAIN control to produce a reading of 2.8V on the Distortion-factor meter.

2.3.13 Switch the receiver internal speaker on, and measure 'SINAD'. Check that the reading is not less than 30dB.

2.4 Selectivity

2.4.1 Connect up the receiver, signal generator, and Distortion-factor meter as in paragraph 2.3.2. Set the receiver to 10500kHz, CW, and a.g.c. OFF. Set the signal generator frequency to 10500kHz, and the output level to 1mV CW.

2.4.2 Adjust the receiver VARIABLE BFO control to produce an audio tone of approximately 1kHz. Adjust the RF-IF GAIN control to produce a 0dBm reading on the Distortion-factor meter. Select each receiver bandwidth in turn, and check that the Distortion-factor meter reading does not vary by more than 4dB in any case.

2.5 RF Meter AGC Readings

2.5.1 These tests check that the correct a.g.c. decay times are being selected. They do not in themselves give an accurate measurement of the a.g.c. decay times. If required, a stop-watch check can be used to establish decay times to a degree of accuracy which is sufficient for maintenance purposes.

2.5.2 Connect the signal generator to the receiver antenna input. Set the receiver to 5301kHz, LSB, and a.g.c. LONG. Set the signal generator to 5300kHz, producing a CW output of 10uV level.

2.5.3 Set the receiver meter switch to RF and note the meter reading. Increase the signal generator output level to 1mV and again note the meter reading.

2.5.4 Switch off the signal generator output and check that the receiver meter needle takes approximately 10 seconds to fall to the first reading noted in paragraph 2.5.3.

2.5.5 Select a.g.c. MED and switch on the signal generator output. Repeat the test of paragraph 2.5.4. The meter needle should fall in approximately 2 seconds.

2.5.6 Repeat the test in paragraph 2.5.5 with the receiver set to a.g.c. SHORT. The meter needle should fall very quickly (nominally 1/5 sec.).

2.6 RF-IF GAIN Control

With the receiver and signal generator set up as in paragraph 2.5.2, select a.g.c. OFF and turn the RF-IF GAIN control fully anti-clockwise. Increase the signal generator output level to 1V and check that a reading of not more than 0dBm is obtained on a Distortion-factor meter connected across the LINE O/P No.1 terminals of the receiver.

2.7 ISB

2.7.1 Connect up the receiver, signal generator, and Distortion-factor meter as in paragraph 2.3.2. Set the receiver to 3700kHz, ISB, XTAL, and a.g.c. SHORT. Set the signal generator to 3701kHz CW at a level of 1mV.

2.7.2 Switch on the internal speaker and check that a 1kHz tone can be heard when the ISB AUDIO switch is set to USB. Check that the tone disappears when the switch is set to LSB. Check that the Distortion-factor meter reads approximately 0dB.

2.7.3 Shift the signal generator output frequency to 3699kHz and check that the tone is again audible and that the Distortion-factor meter reading has fallen to not less than -50dB.

2.7.4 Shift the Distortion-factor meter to the LINE O/P No.2 terminals of the receiver. Check that the reading is approximately 0dB. Shift the signal generator frequency back to 3701kHz and check that the reading falls to not less than -50dB.

2.8 Mode F

Connect up the receiver, signal generator, and Distortion-factor meter as in paragraph 2.7.1. Set the signal generator frequency to 3700kHz and check that a constant output tone of 2.5kHz is produced: this can be measured either by connecting a frequency counter to the receiver audio output or by 'notching out' the response on the Distortion-factor meter.

2.9 De-sensitisation

2.9.1 Connect up the receiver, signal generator, and Distortion-factor meter as in paragraph 2.3.2. Set the receiver to 2400kHz, USB, XTAL, and a.g.c. OFF. Set the signal generator to 2401kHz CW with an output level of 1uV. Note the Distortion-factor meter reading, which should be approximately 0dBm.

2.9.2 Shift the signal generator frequency to 2421kHz and increase its output level until the Distortion-factor meter reading is the same as that obtained in paragraph 2.9.1. Check that the signal generator output level is not less than 32mV.

2.9.3 Repeat the test in paragraph 2.9.2 with the signal generator set to 2381kHz. The same result should be obtained.

2.9.4 Repeat the test in paragraphs 2.9.1 to 2.9.3 with the receiver tuned to 27500kHz and the signal generator set in turn to 27501kHz for paragraph 2.9.1, 27521kHz for paragraph 2.9.2, and 27481kHz for paragraph 2.9.3.

2.9.5 Note that the tests in paragraphs 2.9.1 to 2.9.4 may not give true results if the sideband noise of the signal generator is of the same order as that of the receiver. If a receiver fails this test first repeat the tests using a signal generator known to produce a low level of sideband noise, such as the Marconi TF144.

2.10 Intermodulation

2.10.1 Connect both signal generators via HF blocking amplifiers to the hybrid. Connect the output from the hybrid via the variable attenuator to the input of the RF Millivoltmeter in parallel with a 50 ohm load.

Third Order Intermodulation

2.10.2 Identify the two signal generators as 'A' and 'B'. Set signal generator 'A' to 17300kHz. Set signal generator 'B' to 17340kHz. Set the attenuator to 0dBm and, one at a time, adjust each signal generator to produce a 50mV reading on the Millivoltmeter.

2.10.3 Set the attenuator to 100dB and connect its output to the antenna input of the receiver. Switch off signal generator 'B'.

2.10.4 Set the receiver to 17300kHz, CW, 300Hz, XTAL, and a.g.c. OFF. Set the VARIABLE BFO control to produce a tone of approximately 1kHz.

2.10.5 Connect the distortion factor meter to the LINE O/P No.1 terminals of the receiver, and note the audio output level reading.

2.10.6 Shift signal generator 'A' frequency to 17320kHz, and switch on the output of signal generator 'B'.

2.10.7 Switch out attenuation until the output reading is the same as that obtained in paragraph 2.10.5. The number of dB attenuation which has been switched out is the level in dBuV of the unwanted signals producing a third-order intermodulation product equivalent to 1uV (specification is 'not less than 90dBuV').

2.10.8 Repeat the tests in paragraphs 2.10.6 and 2.10.7 with signal generator 'A' set to 17280kHz and signal generator 'B' set to 17260kHz.

2.10.9 If the levels are unacceptable, R10 in Module 2 can be adjusted for the lowest possible output level in paragraph 2.10.7. If R10 has to be adjusted, great care must be taken; there is more than one point at which a dip in the response is obtained. The first dip clockwise from the fully anticlockwise setting must be used.

Second Order Intermodulation

2.10.10 Repeat the tests in paragraphs 2.10.6 and 2.10.7 with signal generator 'A' set to 14050kHz and signal generator 'B' set to 3250kHz. If the receiver is fitted with Module 1A, specification is 'not less than 57dBuV' in place of 'not less than 90dBuV'.

2.11 Reconstituted Carrier

2.11.1 Set up the receiver and test equipment as in paragraph 2.10.1. Set the receiver to 1750kHz, LSB, XTAL, and a.g.c. MED: set the receiver meter switch to ZERO BEAT.

2.11.2 Set signal generator 'A' to 1750kHz and set signal generator 'B' to 1749kHz. Set the attenuator to 40dB. With both signal generator outputs on, a 1kHz tone should be heard in the phones or on the speaker.

Note the swing rate of the receiver meter indication and note it as an indication of a 1kHz tone.

2.11.3 Set the receiver manual tuning to SLOW, and tune 50Hz above 1750kHz with the MANUAL TUNING control. Note the change in audio tone with tuning variation.

2.11.4 Select RECON.CAR. and check that the audio tone changes back to 1kHz. This can be checked in two ways; firstly by the slight drop in tone frequency and secondly by the variation in receiver meter needle swing rate.

2.11.5 Repeat the tests in paragraphs 2.11.2 to 2.11.4 with the output of signal generator 'A' reduced by 40dB.

2.11.6 The presence of signal generator 'B' producing 1749kHz tests the ability of the receiver to hold to the tuned (1750kHz) signal in the presence of an adjacent unwanted signal. The test would in fact be valid if carried out with signal generator 'A' only, but would not then prove the receiver's ability to hold in the presence of an unwanted signal.

2.12 Memory

2.12.1 Store sixteen different sets of front-panel settings in the memory, one in each channel. Recall them in turn, and check that all are correct. For convenience, a list of sixteen sets are given below.

TABLE 1 : FRONT-PANEL SETTINGS

CHANNEL	FREQ.	MODE	B/W	AGC	RE.IN.CARR
0	1000	AM	8	LONG	-
1	15500	AM	6	OFF	RECON CAR
2	15500	AM	6	SHORT	RECON CAR
3	15499	USB	-	SHORT	XTAL
4	15501	LSB	-	SHORT	XTAL

continued ...

TABLE 1 continued ...

CHANNEL	FREQ.	MODE	B/W	AGC	RE.IN.CARR
5	15500	CW	300	SHORT	XTAL
6	10499	USB	-	SHORT	XTAL
7	5301	LSB	-	LONG	XTAL
8	5301	LSB	-	MED	XTAL
9	3700	ISB	-	SHORT	XTAL
10	3700	F	1.2	SHORT	XTAL
11	27500	USB	-	SHORT	XTAL
12	17300	CW	300	OFF	XTAL
13	1750	LSB	-	MED	RECON CAR
14	1750.05	LSB	-	MED	RECON CAR
15	12345.67	AM	6	SHORT	-

2.12.2 Set the receiver to any one of the suggested settings given in paragraph 2.12.1. Remove the a.c. power supply from the receiver, and reconnect it after a few minutes. Check that the applied settings reappear.

CHAPTER 3

FAULT-FINDING

CONTENTS

TABLES

ILLUSTRATIONS

FAULT-FINDING

1. INTRODUCTION

The information given in this chapter will aid diagnosis of the majority of faults, especially where the maintainer is unfamiliar with the equipment from the diagnostic point of view. The receiver has a predicted Mean Time Between Failures of 5500 hours. No diagnostic aid can cover every possibility: the information given in this chapter has been chosen to cover the most likely situations, and to locate faults to module and interconnection level. Once a fault has been located to module level reference should be made to the appropriate Section 4 chapter, wherein will be found full test data and test equipment requirements for that module. A Servicing Kit is available as Plessey Part No.630/1/32955.

2. TEST EQUIPMENT

Almost all diagnosis to the levels of the charts in this chapter can be carried out with the aid of:

(1) A 20,000 ohm per volt multimeter.

(2) A 50 ohm input RF Voltmeter.

(3) An oscilloscope capable of displaying signals up to 30MHz.

(4) A signal generator covering 100kHz to 30MHz, capable of producing both AM and CW outputs at levels between 1uV and 1V rms.

Experience in a particular situation and the requirements of a particular repair policy may suggest other useful items.

3. REPAIR TECHNIQUES

3.1 The receiver uses a large number of CMOS integrated-circuit devices and therefore suitable precautions must be taken to avoid damaging them by electro-static charges. These precautions are laid down on page (vi) of this manual: read them before attempting any repair work.

3.2 Generally, normal workshop methods are applicable. However, to avoid damage to printed-circuit panels (especially the flexible type) the use of de-soldering braid ('solder-wick') to de-solder joints is essential. Do not try to pull component leads through a pool of molten solder. We recommended removing faulty components by the following method:

(1) Cut the lead wires close to the component, and discard the component.

(2) De-solder the attachment points of the pieces of lead which remain in the printed-circuit panel.

(3) Remove the pieces of lead without using force: they should pull out easily.

3.3 Apart from the rear tag-strip terminals and the meter terminals, all screw threads are of the ISO metric series. The rear tag-strip threads are 4BA (3.6 mm (0.142 ins) diameter, 38.5 TPI). The meter terminal threads are 8-32UNC, and are fitted with 1/4 ins AF nuts. In a number of places (especially on Module 10) nuts can only be reached with a tubular

box spanner (wrench) or a miniature socket set. AF sizes required are 4 mm, 5.5 mm, 6 mm, and 1/4 ins. The 5.5 mm size is not always easily available, and 7/32 ins AF can be used in its place. Similarly, a 4BA spanner can be used in place of 1/4 ins AF.

4. VOLTAGE AND SIGNAL LEVELS

4.1 Most analogue voltage and signal levels inside modules can be found in the test data given in the chapters of Section 4. The performance checks of Section 5, Chapter 2 also provide a source of test data. In the digital portions of the circuits logic '1' is nominally +12V and logic '0' is nominally 0V, except in the external data lines to and from Module 12: these lines can be of various levels according to the installation and the settings of Module 12 internal switching, and they use a low = '1', high = '0' convention. Refer to Section 4, Chapter 12 and Section 5, Chapter 1 for details.

4.2 Inside the receiver, the integrated circuits employed produce a '0' output level which is within 50mV of 0V, and a '1' output level which is within 50mV of their supply voltage. They will interpret as '0' an input level below +3V, and will interpret as '1' an input level above +7V.

4.3 Unlike TTL devices, CMOS integrated circuits do not require closely regulated power supply voltages. In this equipment they are mainly run from a +12V supply, but work equally well on +9V. The voltage tolerances on the d.c. outputs of the receiver power supply unit (Module 8) will be found in Section 4, Chapter 8.

4.4 Voltage and signal levels quoted for analogue circuitry should not be taken as exact, as they inevitably vary a small amount between individual receivers due to component tolerances. This is especially true when following a signal through from the antenna input to the detectors, as the effects of various gain tolerances can be significant. Table 3-1 defines 'key' analogue levels in such a way as to permit the maintainer to allow for these tolerances. Each level is measured by removing an inter-module co-axial connector and inserting a 50 ohm impedance RF Voltmeter. The receiver tuning is to be set to 15500kHz.

5. FAULT-FINDING CHARTS

5.1 Procedures for dealing with eight estimated fault conditions are given in Figures 1 to 8. Each figure is in the form or a 'flow diagram' which should be followed through as a diagnostic procedure. Each starts from a fault condition which in all probability would have been reported by the operator.

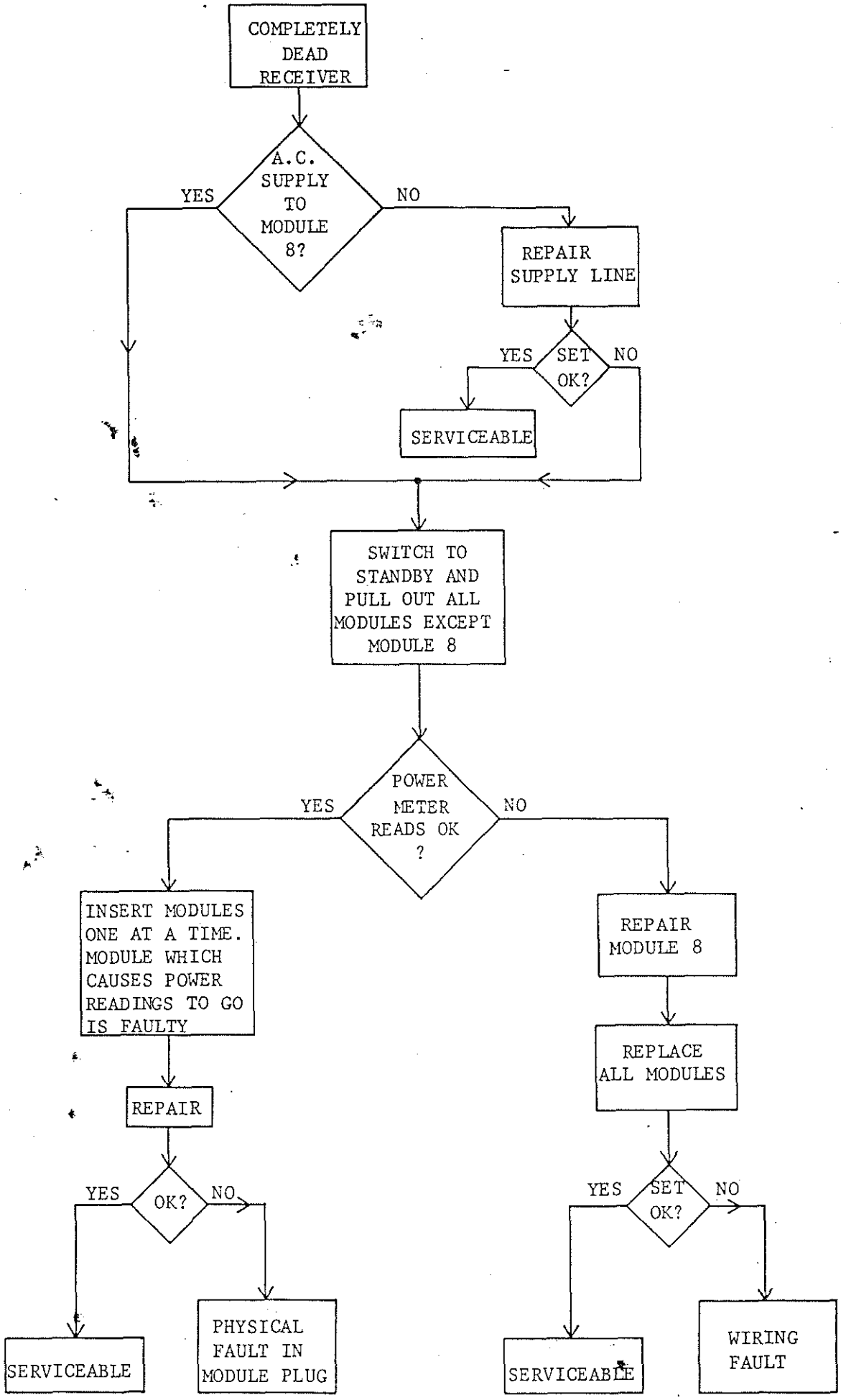
5.2 Each chart takes diagnosis to 'module and interconnections' level. If a repair policy of module replacement only is in force, the charts should be used on the basis of checking modules by substitution, and repairing by replacing modules. If a repair policy of maintaining down to component level is in force, then fault diagnosis inside a suspect module should be carried out with the aid of the appropriate chapter of Section 4. Each chapter in Section 4 covers one module, and contains detailed test data and a list of test equipment required.

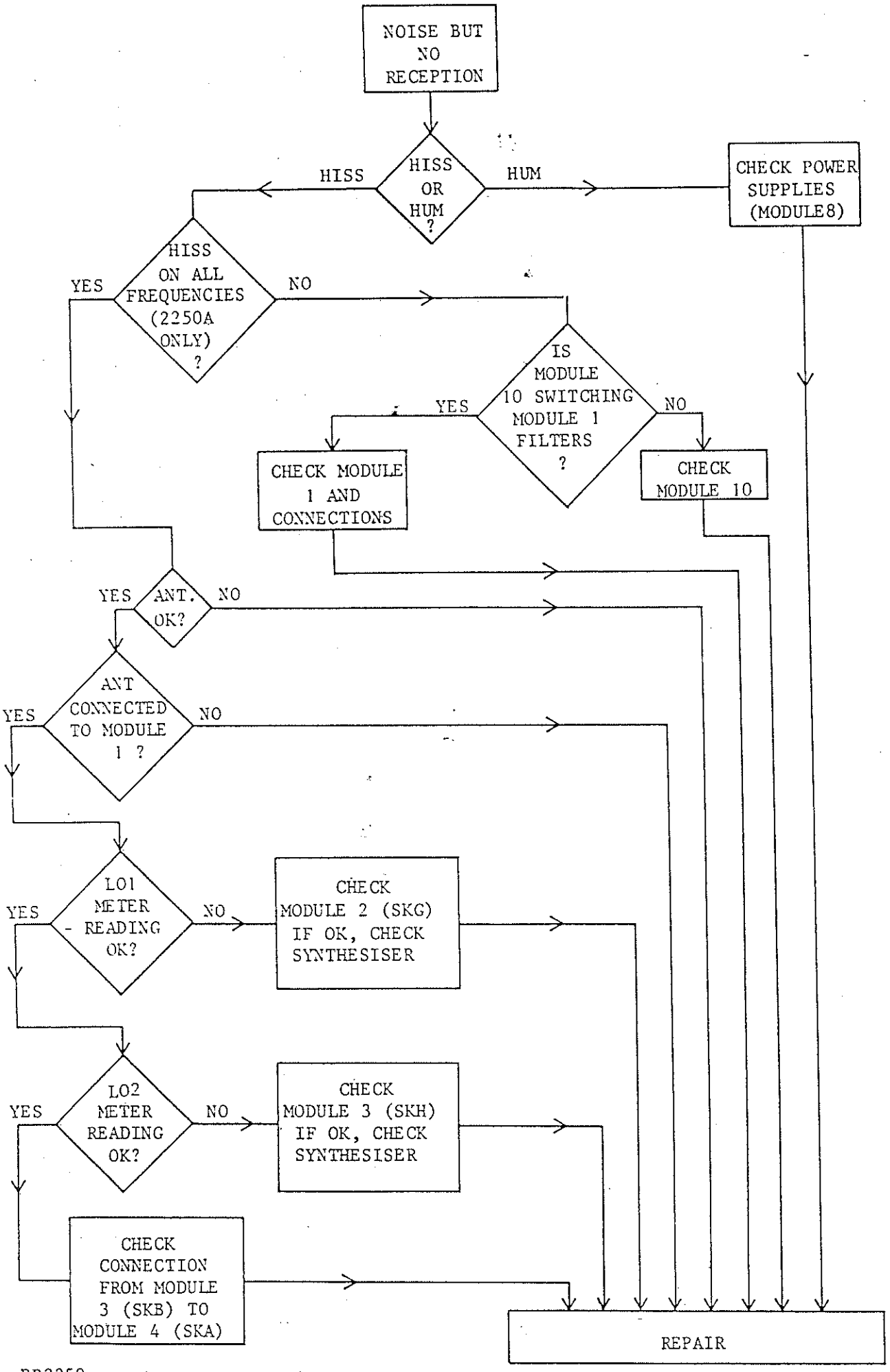
TABLE 1 : KEY ANALOGUE LEVELS

MODULE	MODE	INPUT(S) SIGNAL	INPUT(S) SOCKET	OUTPUT(S) SIGNAL	OUTPUT(S) SOCKET
1	ALL	15500kHz AM, 30% mod, 1mV rms, 50 ohm from Sig. Gen.	AERIAL	1500kHz, -3dB w.r.t. input sig., 50 ohm	SLJ
2	ALL	LO(1); from Module 9 SKA, 49500kHz, 8dBm ±3, 50 ohm. Signal; from Module 1 SKH (unchanged).	SKG SKA	65000kHz, +4dB +0 -2 w.r.t. Module 1 output, 50 ohm	SKC
3	ALL	LO(2); from Module 9 SKB 63600kHz, 8dBm ±3, 50 ohm. Signal; from Module 2 SKC (unchanged).	SKH	1400kHz, +10dB ±2 w.r.t.Module 2 output 1000 ohm (Measured with 50 ohm meter)	SKB
4	USB, F, ISB, CW & 0.1 B/W AM, ISB LSB, ISB CW not 0.1 B/W	) Signal; from) Module 3 SKB) (unchanged:) measured with) a 50 ohm meter)	SKA	1400kHz, 15mV r.m.s. ±2dB, 50 ohm. 1400kHz, 10mV r.m.s. ±2dB, 50 ohm. 1400kHz, 10mV r.m.s. ±2dB, 50 ohm. 1400kHz, 20mV r.m.s. ±2dB, 50 ohm.	SKF SKC SKE SKF
5	AM, ISB USB, ISB (U), CW, F not 0.1 LSB, ISB (L) ALL ALL ALL ALL	Signal; from Module 4 SKC (unchanged). Signal; from Module 4 (unchanged). Signal; from Module 4 SKE (unchanged). 1.4MHz LO; from Module 6 SKA (unchanged). (50 ohm meter). 1.5MHz LO; from Module 6 SKC (unchanged). (50 ohm meter).	SKA SKB SKD SKC SKE	'100kHz IF' outputs. 200mV r.m.s. ±5mV, 50 ohm, or as set up. Variable level audio to speaker and phones.	SKF

TABLE 1 continued ...

MODULE	MODE	INPUT(S)		OUTPUT(S)	
		SIGNAL	SOCKET	SIGNAL	SOCKET
6	SSB	Signal; from Module 4 SKF (unchanged). Ref; from Module 7 SKA (unchanged).	SKE SKG	1400kHz (nominal) 10mV r.m.s, 1000 ohm (measured with 50 ohm meter).	SKA & SKC
7	ALL	-	-	1000kHz, 290mV, r.m.s. 50 ohm.	SKA
9	ALL	-	-	49500kHz, 8dBm ±3, 50 ohm (LO1). 63600kHz, 8dBm ±3, 50 ohm (LO2).	SKA SKB


COMPLETELY DEAD RECEIVER
A.C. SUPPLY TO MODULE 8?
YES
NO
REPAIR SUPPLY LINE
YES
SET OK?
NO
SERVICEABLE
SWITCH TO STANDBY AND PULL OUT ALL MODULES EXCEPT MODULE 8
POWER METER READS OK ?
YES
NO
INSERT MODULES ONE AT A TIME. MODULE WHICH CAUSES POWER READINGS TO GO IS FAULTY
REPAIR
YES
OK?
NO
SERVICEABLE
PHYSICAL FAULT IN MODULE PLUG
REPAIR MODULE 8
REPLACE ALL MODULES
YES
SET OK?
NO
SERVICEABLE
WIRING FAULT


NOISE BUT NO RECEPTION
HISS OR HUM ?
HISS
HUM
CHECK POWER SUPPLIES (MODULE8)
HISS ON ALL FREQUENCIES (2250A ONLY) ?
YES
NO
IS MODULE 10 SWITCHING MODULE 1 FILTERS ?
YES
NO
CHECK MODULE 1 AND CONNECTIONS
CHECK MODULE 10
ANT. OK?
YES
NO
ANT CONNECTED TO MODULE 1 ?
YES
NO
LO1 METER - READING OK?
YES
NO
CHECK MODULE 2 (SKG) IF OK, CHECK SYNTHESISER
LO2 METER READING OK?
YES
NO
CHECK MODULE 3 (SKH) IF OK, CHECK SYNTHESISER
CHECK CONNECTION FROM MODULE 3 (SKB) TO MODULE 4 (SKA)
REPAIR

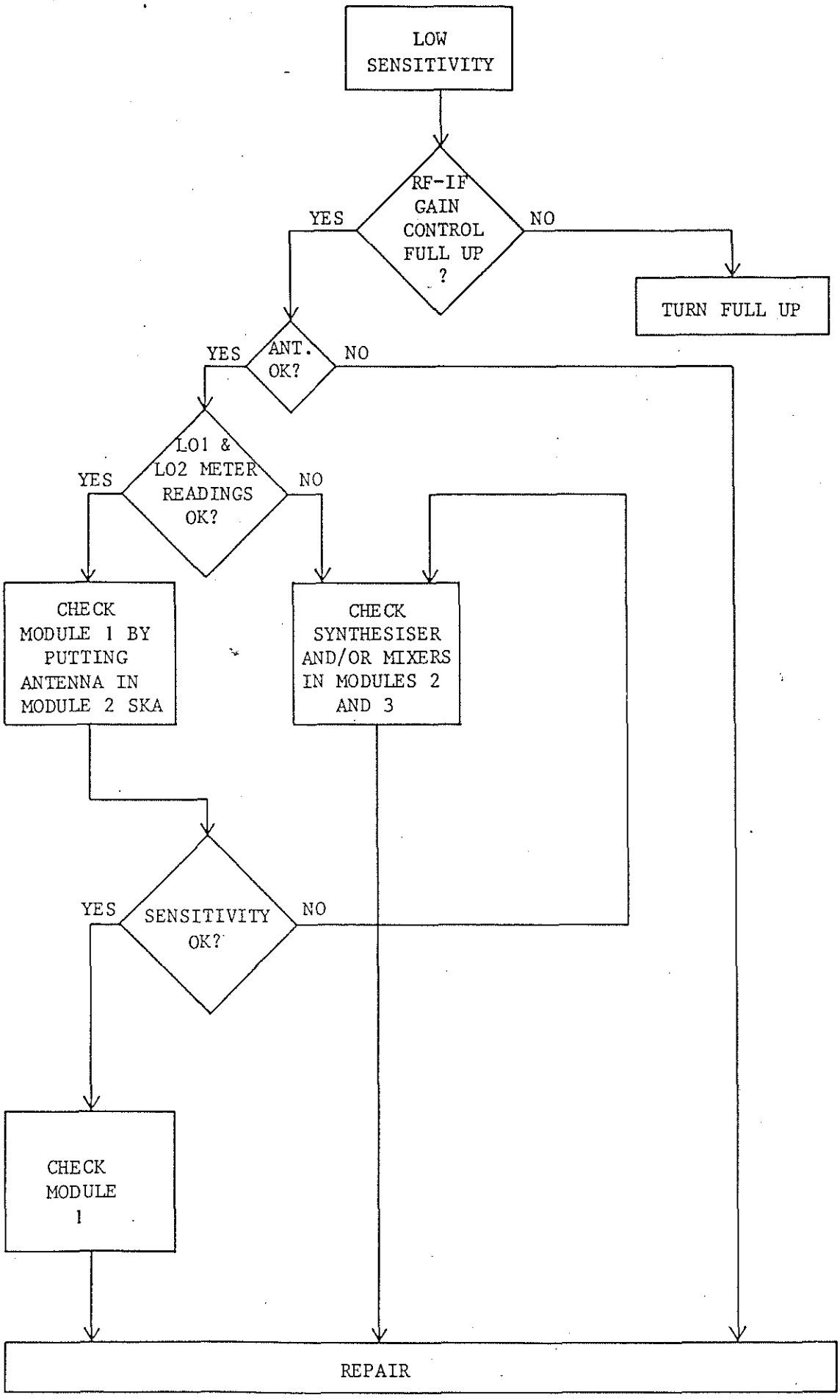


Fig. 3 LOW SENSITIVITY

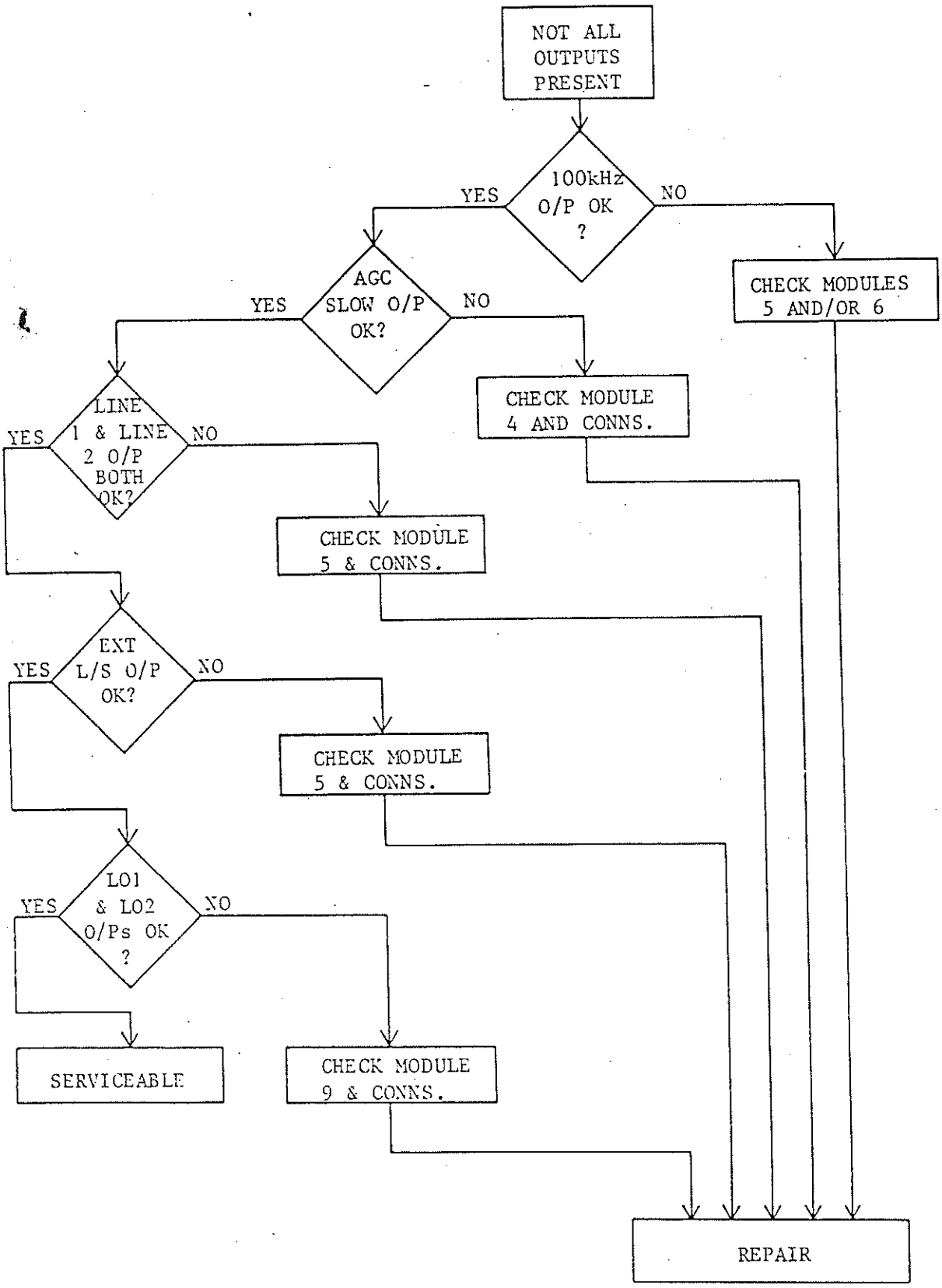


Fig. 4 MISSING RECEIVER OUTPUTS

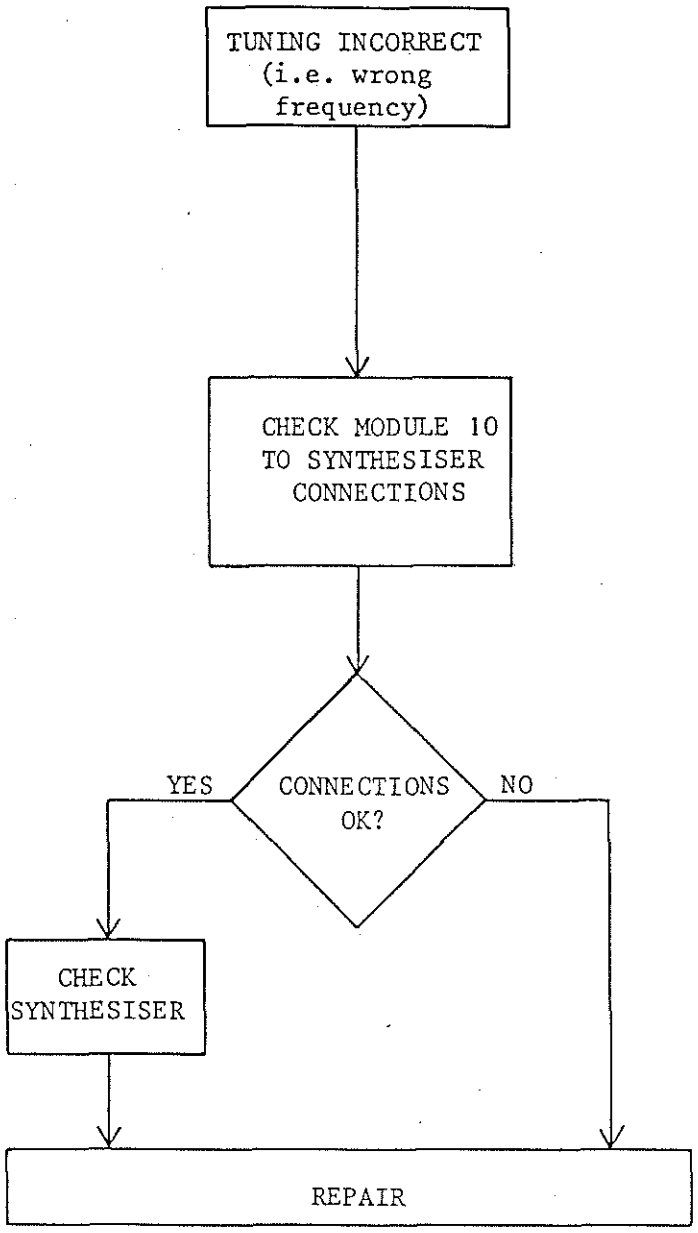


Fig. 5 INCORRECT FREQUENCY

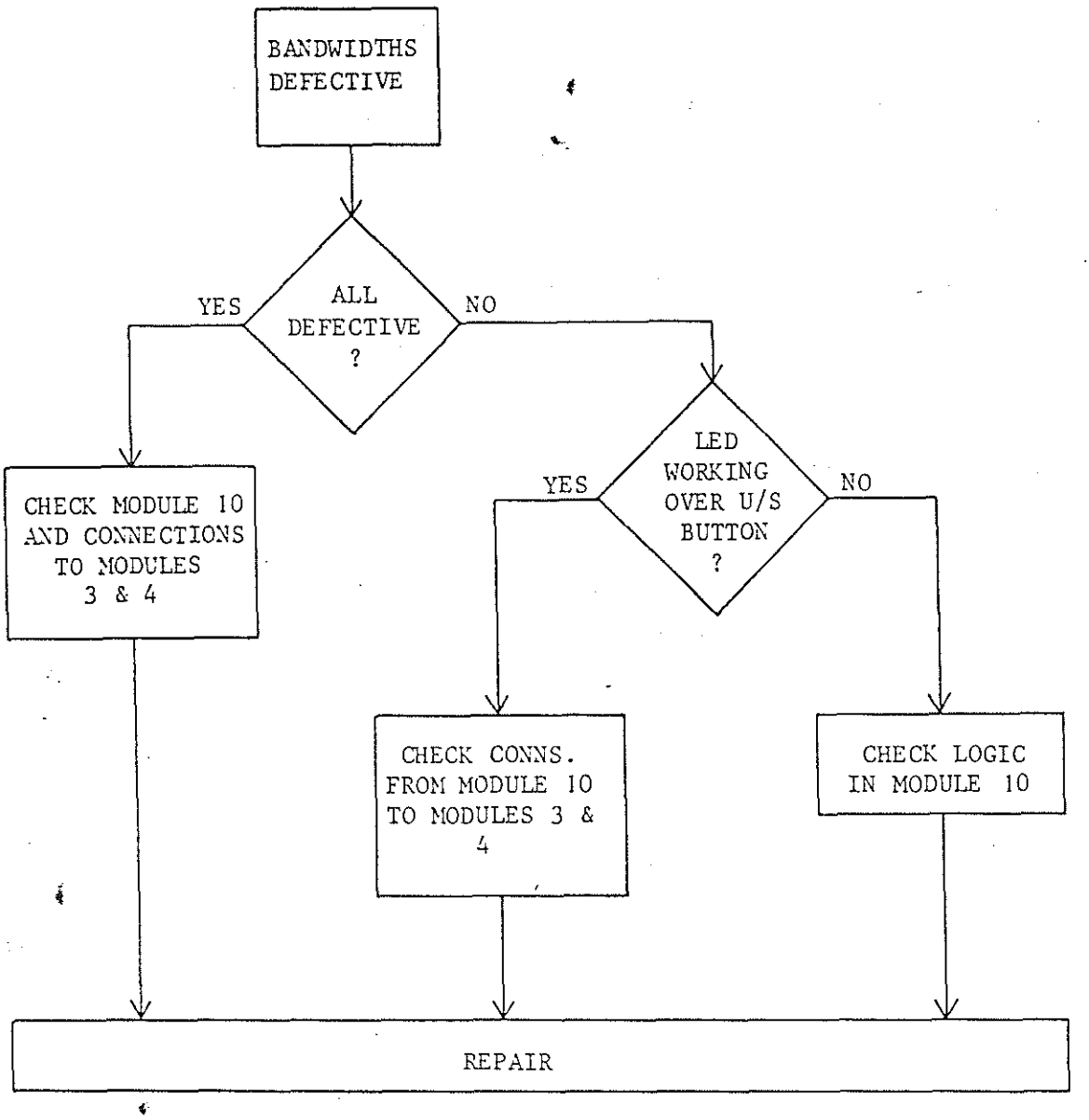


Fig. 6 DEFECTIVE BANDWIDTHS

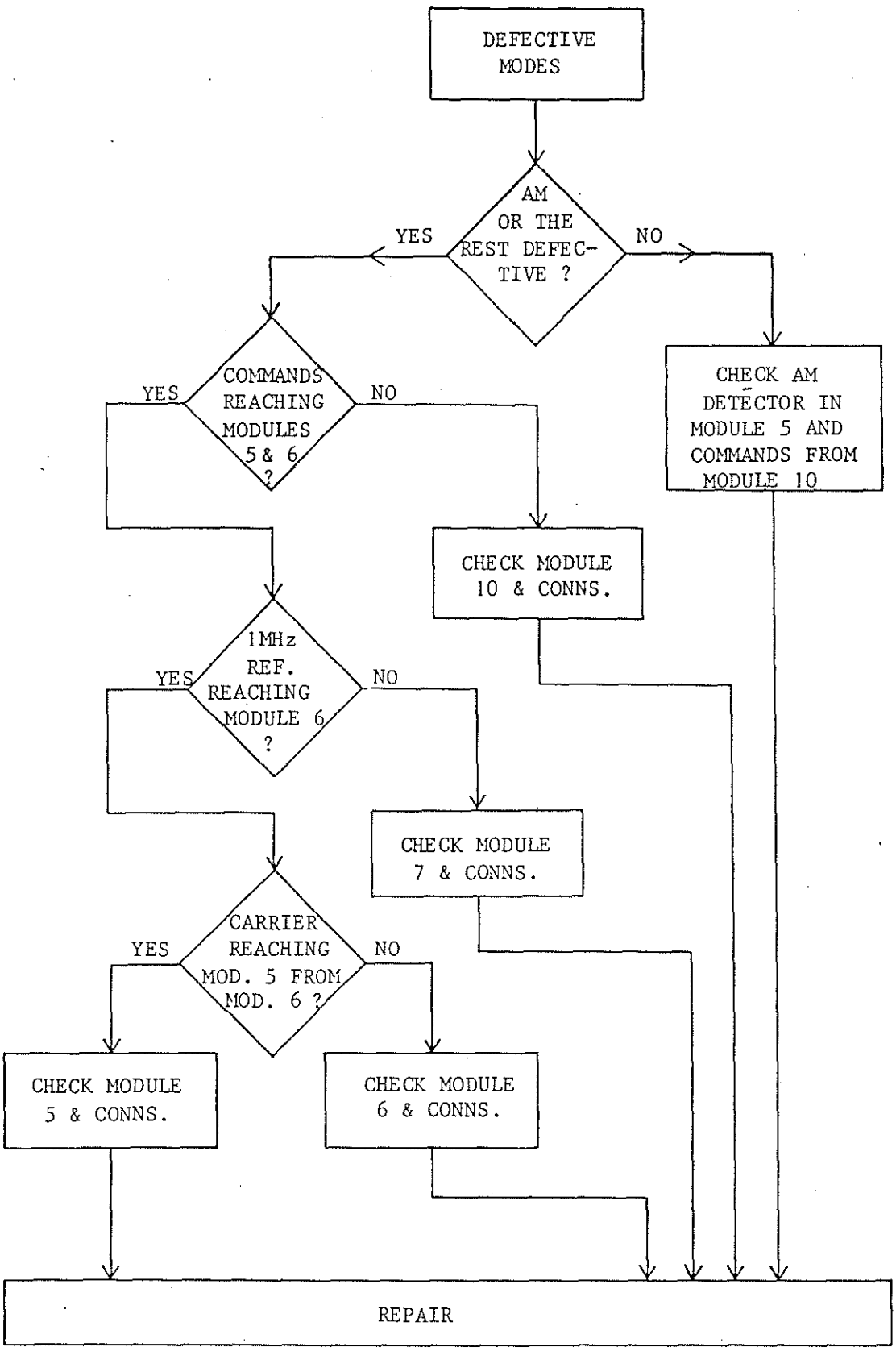


Fig. 7 DEFECTIVE MODES

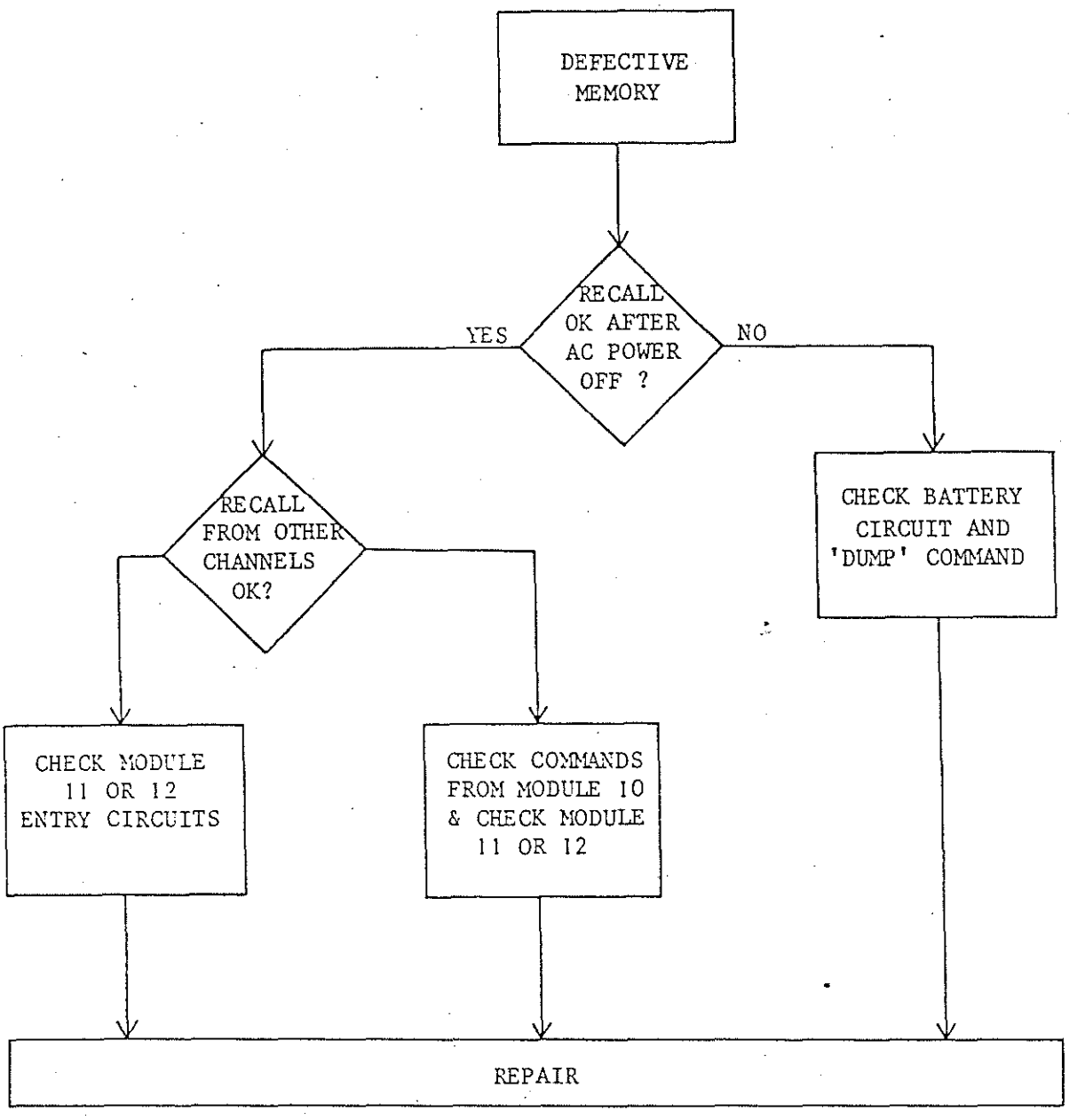
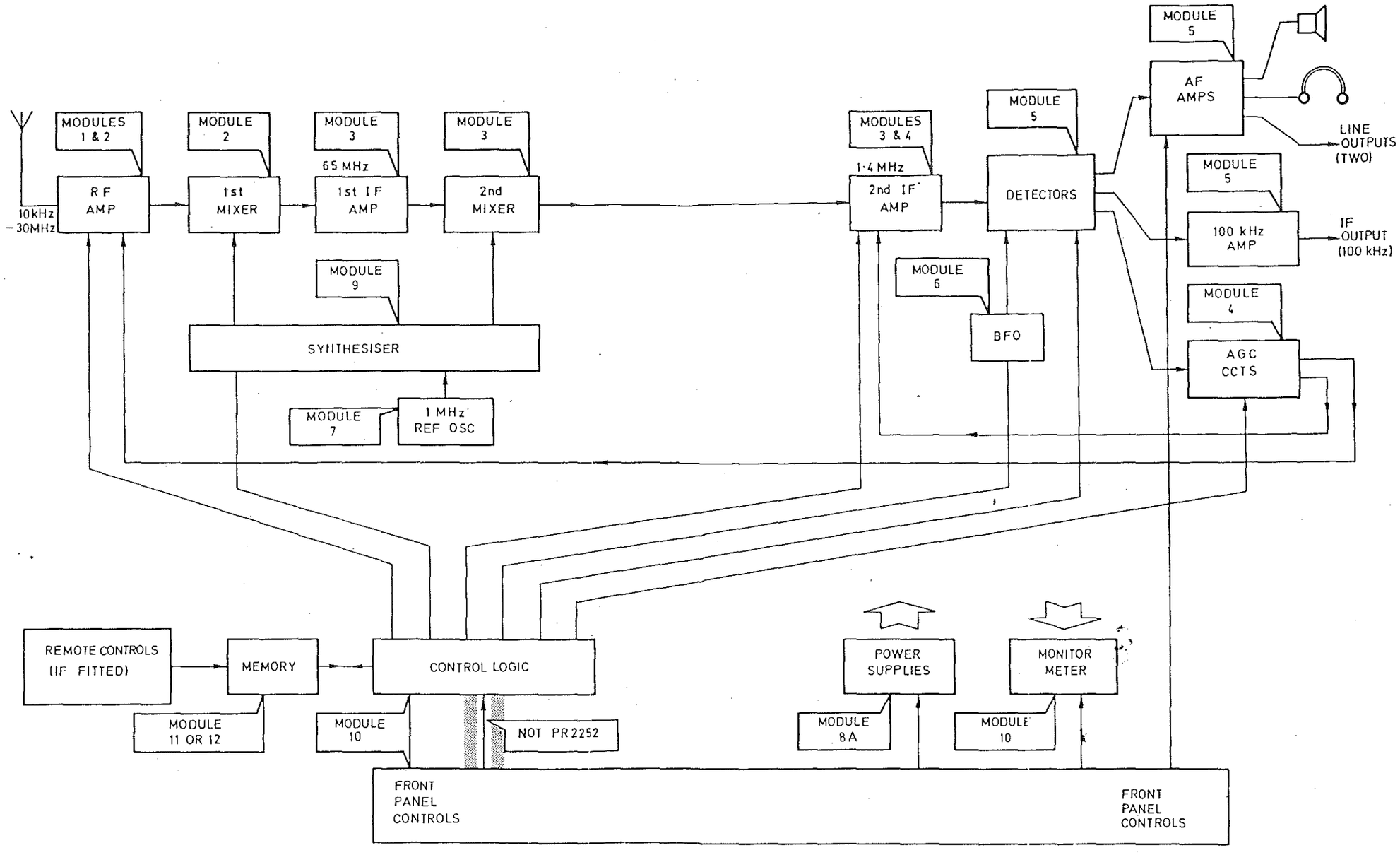
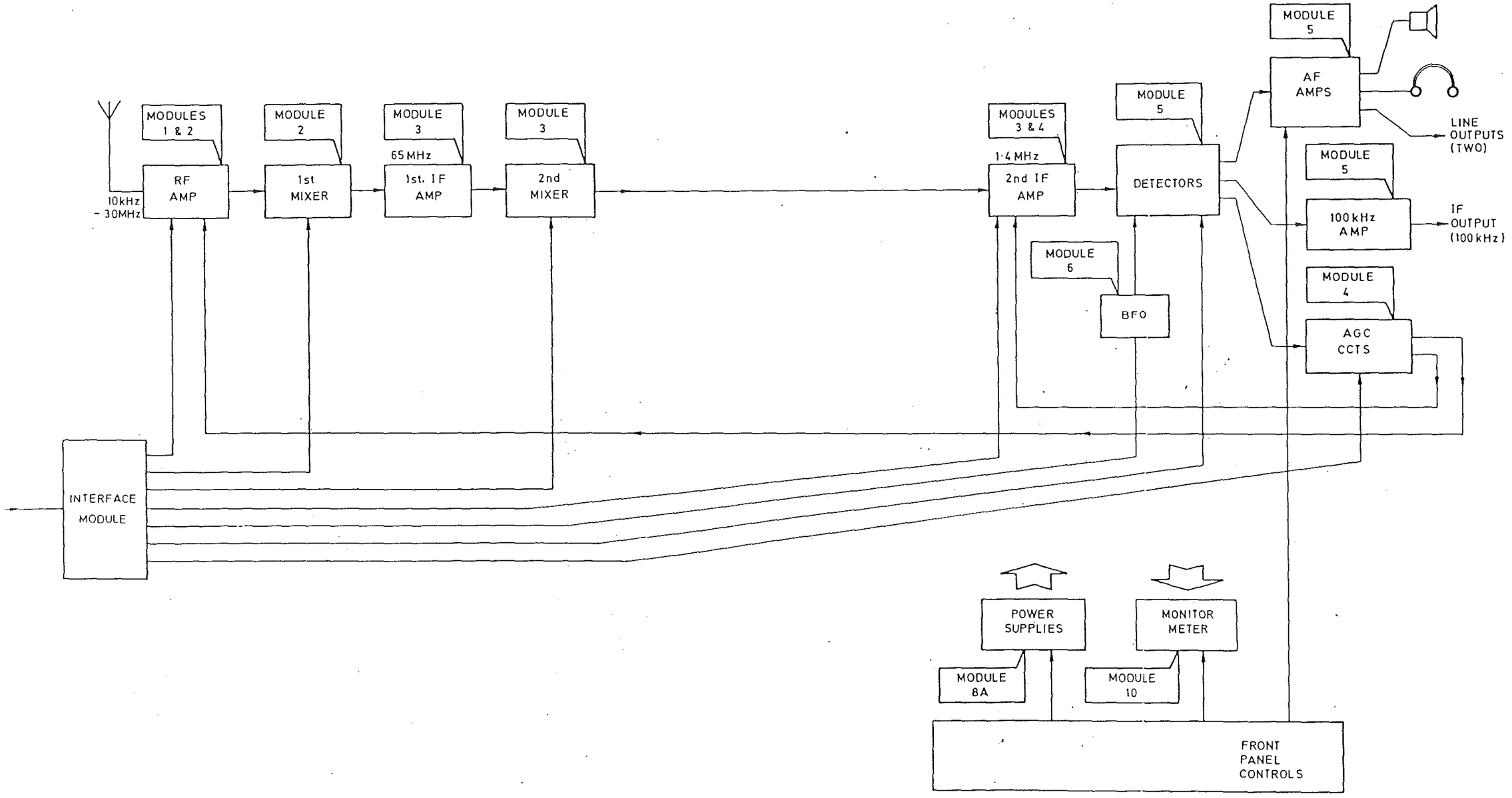


Fig. 8 DEFECTIVE MEMORY



PR2250 AND PR2252 RECEIVERS — BASIC BLOCK DIAGRAM — FIG. 1



PR 2251 RECEIVER

BASIC BLOCK DIAGRAM

FIG. 2

CHAPTER 2

FUNCTIONAL DESCRIPTION

CONTENTS

TABLES

ILLUSTRATIONS

FUNCTIONAL DESCRIPTION

1. INTRODUCTION

1.1 This description covers the PR2250 series of receivers which is defined in Table 1 of the GENERAL DESCRIPTION. Difference between the various models are confined to:

(a) Variations in Modules 1, 3, and 10.

(b) Use of either Module 11 or Module 12.

(c) Omission or inclusion of Modules 7 and 9.

1.2 Section 4 of the manual consists of a number of separate chapters, each covering one module. Each chapter contains a functional description, a circuit description, and a components list. All module chapters are included, irrespective of whether the module concerned is or is not fitted in a particular receiver. One mechanical description chapter in Section 3 covers all modules.

2. SIGNAL-FREQUENCY CIRCUITS

2.1 The 50 ohm antenna input is applied to filter circuits in either Module 1 or Module 1A, depending on the particular model of receiver. Module 1 is shown on the functional diagram Fig.2-1. The signal is fed via a low-pass filter to a set of sub-octave band-pass filters. At any time, one band-pass filter is switched into circuit. This filter is selected by the control circuits associated with the tuning control so as to be appropriate for the frequency being received. In Module 1A, these sub-octave filters are omitted.

2.2 The filtered output from Module 1 (or 1A) is applied to the r.f. amplifier in Module 2. This amplifier is a.g.c. controlled.

3. 1ST IF CIRCUITS

3.1 The amplified r.f. signal is applied to the 1st Mixer in Module 2. The secondinput to the mixer is supplied:

(a) in PR2250 and PR2252 receivers, from the synthesiser in Module 9.

(b) in PR2251 receivers, from the synthesiser in Module 9 of the associated PR2250 'master' receiver.

3.2 The synthesiser consists of a complex phase-lock loop circuit locked to the 1MHz reference output from the associated crystal frequency standard in Module 7. The phase-lock loop circuits are covered by Plessey Company patent rights. They produce an output frequency which is variable in 10Hz steps from 65 to 95MHz. Stability is 1 part in 2×10^8 maximum over 24 hours at constant temperature, and 1 part in 10^7 from 0°C to +50°C (32°F to 122°F). Frequency control of the 1st local oscillator output from the synthesiser is exercised digitally via Module 10 (the front panel and control circuit module). The desired frequency can be set as follows:

(a) in PR2250 receivers from the front panel keypad and manual tuning control, of from the memory. If Module 12 is fitted, it can also be set by remote control.

(b) in PR2251 receivers, control is slaved to the associated PR2250 'master' receiver.

(c) in PR2252 receivers, control is exercised only from a remote position via Module 12.

3.2 The lower sideband of the mixer output is selected by a crystal band-pass filter, and applied to an amplifier situated in Module 3. This amplifier provides the 65MHz 1st IF input to the 2nd mixer.

4. 2ND IF CIRCUITS

4.1 The second mixer, situated in Module 3, receives the 65MHz 1st IF output and a 2nd local oscillator input of 63.6MHz from the synthesiser in Module 9. This local oscillator signal is generated by circuits similar to those used to generate the 1st local oscillator signal, and similar stability is achieved. The same variations in origin apply as defined in 3.2 for the 1st L.O. The lower sideband of the 2nd mixer output is selected by one of a bank of five band-pass filters (three in the case of Module 3A). The centre frequencies of all filters are 1.4MHz; they differ, however in bandwidth as can be seen in Figure 2-1. These filters form the reception bandwidth control of the receiver, and are operator-selected by the 'BANDWIDTH' controls.

4.2 The 1.4MHz filtered output from the 2nd mixer is amplified in an a.g.c.-controlled circuit situated in Module 4, and applied via a 4-way path splitter to an A.M. filter and three band-pass filters. Filter bands are:

LSB : 1.4MHz	+ 250Hz - 3kHz	)
USB : 1.4MHz	+ 3kHz - 250Hz	) to -3dB points
0.1 : 1.4MHz	± 50Hz	)

4.3 The four outputs are switched by the MODE and BANDWIDTH controls from Module 10 to four 1 output lines as shown in Table 1.

TABLE 1 : 2ND IF OUTPUT SWITCHING

MODE	BANDWIDTH	ROUTE
AM	not relevant	(a) via A.M.filter to amplifier A (b) via 0.1 filter to amplifier C
CM	NOT 0.1	(a) via A.M.filter to amplifier B (b) via 0.1 filter to amplifier C
CW	0.1	via 0.1 filter to amplifiers B & C
F	NOT 0.1	(a) via A.M.filter to amplifier B (b) via 0.1 filter to amplifier C

TABLE 1 (Cont'd)

MODE	BANDWIDTH	ROUTE
LSB	NOT 0.1	(a) via LSB filter to amplifier D (b) via 0.1 filter to amplifier C
ISB	NOT 0.1	(a) via A.M.filter to amplifier A (b) via 0.1 filter to amplifier C (c) via LSB filter to amplifier D (d) via USB filter to amplifier B
USB	NOT 0.1	(a) via USB filter to amplifier B (b) via 0.1 filter to amplifier C

4.4 The outputs from amplifiers A, B, and D are fed to the detector and audio circuits in Module 5. The output from amplifier C is fed to the BFO circuit in Module 6 as a pilot carrier input.

4.5 In all operating modes except USB, ISB, and LSB, the input to the a.g.c. detectors is taken via the A.M. filter. In USB mode it is taken via the USB filter. In LSB mode it is taken via the LSB filter. In ISB mode two inputs are connected, one from the LSB filter and one from the USB filter, in order that the a.g.c. circuits may react to both sidebands.

5. AGC CIRCUITS

5.1 The varying d.c. output produced by the a.g.c. detector circuits is controlled in respect of rise and decay times by the time-constant and shaper circuits. The decay times can be selected by control from Module 10. Rise time is approximately 5mS, and decay time can be chosen from 0.2, 2, and 10 seconds. The circuit will react to a short noise pulse on a substantially steady signal with a rise time (for the pulse) of about 5mS and a decay time of about 50mS. The a.g.c. control output is applied to the r.f. amplifier and to the 2nd i.f. amplifier. The manual RF-IF GAIN control operates via the a.g.c. circuits: it is inoperative except when a.g.c. is switched off by the operator.

6. DETECTOR AND AUDIO CIRCUITS

6.1 The detector and audio circuits are situated in Module 5. They receive three signal inputs and two BFO inputs, although not all are applied at any one time. The three signal inputs are the outputs from amplifiers A, B, and D as defined in paragraph 4.3. The two BFO inputs are both supplied from Module 6: one is a 1.5MHz signal, while the other is a nominal 1.4 MHz signal. This nominal 1.4MHz signal may be, according to MODE setting, either

(a) 1.4MHz exactly,

(b) 1.4MHz $\pm$ 8kHz, the exact frequency being determined by the BFO control, or

(c) 1.4MHz + x, where the value of x is a preset amount capable of being set in steps of 100Hz by switches in Module 6.

6.2 The output from amplifier A (see para.4-4) is applied to an envelope detector. The output from amplifier B is applied to product detector No.1. The output from amplifier D is applied to product detector No.2. Whichever of these amplifier outputs is active is applied to product detector No.3: this detector employs the 1.5MHz BFO input to produce a '100kHz IF' receiver output.

6.3 The outputs from the envelope detector and from product detectors 1 and 2 are applied to a switching circuit controlled by the MODE logic. The outputs from the switching circuit are applied to the audio output stages. There are three output stages.

(a) One amplifier feeding speaker and phones.

(b) Line output amplifier No.1.

(c) Line output amplifier No.2.

6.4 The overall switching action, and the outputs produced, can be seen in Table 2. Note that when LSB, USB, or ISB mode is selected, the output to the phones and speaker amplifier is selected by the position of the MONITOR USB-MONITOR LSB switch: this means that only one sideband of an ISB signal can be audibly presented.

TABLE 2 : DETECTOR SWITCHING

MODE	AMPLIFIER	DETECTOR	OUTPUTS
AM	C	Env. Prod.3	Sp. & Ph., Line 1, Line 2 100kHz IF
CW	B C(to BFO)	Prod.1 Prod.3	Sp. & Ph., Line 1, Line 2 100kHz IF
F	B C(to BFO)	Prod.1 Prod.3	Sp. & Ph., Line 1, Line 2 100kHz IF
USB	B	Prod.1 Prod.3	Sp. & Ph., Line 1, Line 2 100kHz IF
LSB	D	Prod.2 Prod.3	Sp. & Ph., Line 1, Line 2 100kHz IF
ISB	A B D	Env. Prod.1 Prod.2 Prod.3	- Sp. & Ph., Line 1 Sp. & Ph., Line 2 100kHz IF

6.5 The manual volume control only affects the speaker and phones outputs. The two line output amplifiers have their own preset output level controls.

7. BFO

7.1 The same BFO (Module 6) is used in all PR2250 series receivers. It contains the oscillators and associated control circuits which produce the 1.5MHz and (nominal) 1.4MHz inputs to the detector circuits in Module 5. Three oscillators are employed. Oscillator 1 is permanently phase locked to the 1MHz reference input from module 7. Oscillator 2 can be locked to either the 1MHz ref., the 1.4 MHz pilot carrier from amplifier C of Module 4, or the output from Oscillator 3. Oscillator 3 can be either phase-locked to the 1MHz ref. or can be directly controlled by either the remote or local BFO control.

7.2 Oscillator 1 produces a constant 1.5MHz output to Phase Detector 3 in Module 5. It is controlled by a phase-lock loop employing a 50kHz reference input divided down from the 1MHz ref. input.

7.3 Oscillator 2 can be controlled by either one of two phase detectors. With receiver RE-INSERTED CARRIER control set to XTAL, the oscillator is controlled by the upper of the two phase detectors on Fig.2-1. The reference input to this detector is one of two signals, depending on the receiver operating mode. If the mode is not either CW or F the reference input is 100kHz signal divided down from the 1MHz ref., and an exact 1.4MHz output is obtained. If the mode is either CW or F the reference input is the output from Oscillator 3.

7.4 Oscillator 3 output frequency can be controlled in two ways, according to whether the receiver mode is CW or F. In F mode Oscillator 3 is connected in a phase-lock loop employing a 100Hz reference input divided down from the 1MHz ref., and an output frequency of 100kHz $\pm$ x is produced where x is the value (8kHz max) set (insteps of 100Hz) by the offset switching: Oscillator 2 then produces an output frequency of 1.4MHz $\pm$ x. In CW mode, Oscillator 3 is directly controlled by either the remote or loca BFO control, and can be manually varied $\pm$ 8kHz from 100kHz: Oscillator 2 then produces an output frequency of 1.4MHz $\pm$ 8kHz.

7.5 With the receiver RE-INSERTED CARRIER control set to RECON, Oscillator 2 is controlled by the lower of the two phase detectors on Fig.1. The reference input to this detector is the 1.4MHz pilot carrier output from amplifier C of Module 4, and Oscillator 2 then produces an output of 1.4MHz $\pm$ any variation in the frequency of the pilot carrier. Under these conditions, a monitor phase detector compares Oscillator 2 output frequency with the pilot carrier frequency to produce a ZERO BEAT indition for use on the front-panel monitor meter.

8. CONTROL

8.1 General

The control circuits are housed in Module 10, 10A, or 10B, according to the receiver model. The name 'Module 10' embraces the front panel itself and the circuit board mounted upon it. These items embody all the controls and logic which form the interface between the operator and the receiver proper. The control operates in conjunction with memory circuits contained in either Module 11 or Module 12, whichever is fitted. Where Module 12 is fitted, remote control of the receiver can be exercised.

8.2 PR2250 Control

The PR2250 receiver has full manual control, and employs Module 10. Control functions can be separated into six parts, namely:

(a) Frequency (or tuning) control.

(b) Local-remote control.

(c) Module control.

(d) Bandwidth control.

(e) AGC control.

(f) Memory control.

8.2.1 Frequency Control

Frequency control can be exercised over an unbroken range from 10kHz to 29.99999MHz from the front-panel in two ways.

(a) By setting in the desired frequency on a keypad, or

(b) By use of a manual tuning knob.

In either case, the frequency is displayed on a bank of 7-segment LEDs. The minimum frequency step is 10Hz. Control is exercised over the sub-octave filters in Module 1 and over the 1st Local Oscillator output frequency from the synthesiser. Frequency data is continuously applied to the memory interface and can be read in whenever this is desired. Similarly, stored frequency data is continuously available at the memory interface and may be used to set up the tuning logic whenever this is desired.

8.2.2 Local-Remote Control

Local and Remote push-button controls are fitted to PR2250B, D, and F receivers only. In 'Local' the front-panel controls are operative; in 'Remote', control can only be exercised via the remote interface of Module 12. PR2250A, C, and E receivers have a pair of buttons marked 'Local' and 'Inhibit'. On these receivers the front-panel controls are operative in 'Local', and are inoperative in 'Inhibit'.

8.2.3 Mode and Bandwidth Control

8.2.3.1 Mode and Bandwidth controls are to a certain extent interdependent, inasmuch as selecting some modes automatically selects an appropriate bandwidth. However, where this is so the automatically-selected bandwidth can be over-ridden if so desired. Mode control sets the receiver up to receive any one of six types of signal, namely:

(a) AM

(b) CW

(c) FSK (in F, or 'fixed BFO offset' mode)

(d) USB

(e) LSB

(f) ISB

Mode control is applied to the BFO, and 2nd IF switching, and the detector switching (Modules 4, 5, and 6).

8.2.3.2 Bandwidth control selects the 2nd IF bandwidth from either five or three choices, depending on the type of receiver. Where Module 3 is fitted five 2nd IF filters are available: where Module 3A is fitted, only 3 are available (these three may be any selected three of the five used in Module 3). The five filter bandwidths are:

(a) 8kHz

(b) 6kHz

(c) 1.2kHz

(d) 0.3kHz

(e) 0.1kHz

8.2.4 AGC Control

The AGC keys select the desired a.g.c. decay time-constant or switch off a.g.c. entirely. The decay time-constant can be selected from:

(a) 10 sec.

(b) 2 sec.

(c) 0.2 sec.

Control is exercised on the a.g.c. circuit in Module 4.

8.2.5 Memory Control

The associated memory (in either Module 11 or Module 12) has sixteen channels. The front-panel channel selection control allows any one to be selected. All control settings described in paras.8.2.1. to 8.2.4 can be stored in a memory channel. Similarly, settings for all these controls may be called up from a memory channel and set on the controls. One channel (channel 0) is normally reserved as a temporary 'dump' stores (see Operators Manual).

8.3 PR2251 Control

The PR2251 is a slave receiver for operation in conjunction with a PR2250 or a PR2252. It contains neither Module 7 (frequency standard) nor Module 9 (1st and 2nd LO), and no Module 10 control circuits are fitted. The lines which would in a PR2250 carry the outputs from Modules 7, 9, and 10 are brought out to external connectors via a buffer interface module on a PR2251. These external connectors are wired to the corresponding points of the associated 'master' PR2250 or PR2252 receiver.

8.4 PR2252 Control

The PR2252 is a 'remote-control only' version of the PR2250. Module 10 is replaced by Module 10B, which carries monitoring controls only. Receiver control can only be exercised via the remote interface to Module 12, which replaces Module 11 in PR2252 receivers. Otherwise, the PR2252 is identical with the PR2250.

9. MONITOR FACILITIES

All versions of the receiver carry a monitor meter and associated selector switch. Power supply and signal monitoring is catered for. The signal monitor points (M on Fig.) are:

(a) 1st LO output level (LO1)

(b) 2nd LO output level (LO2)

(c) AGC level (RF)

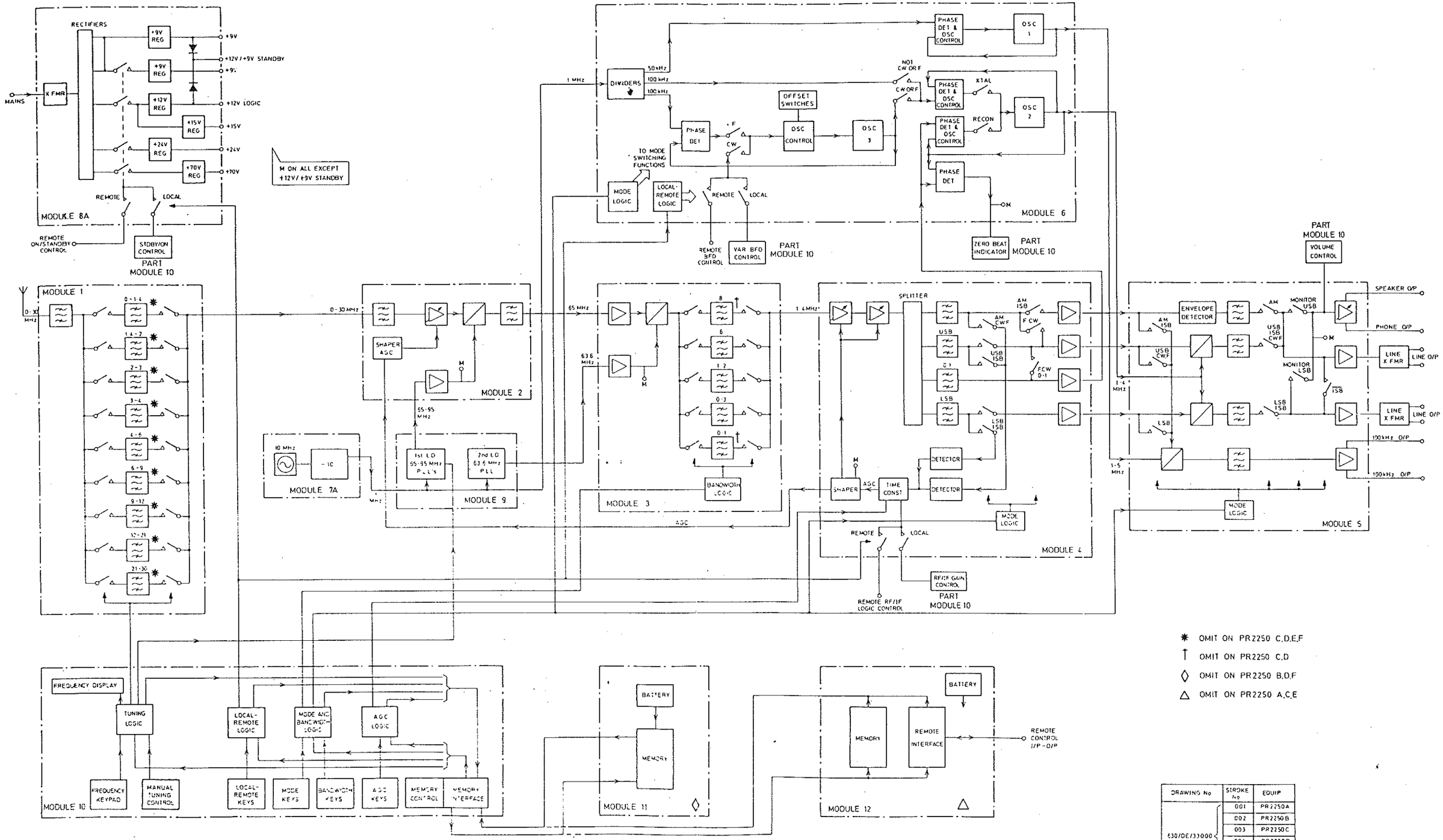
(d) Audio line output level (AF)

(e) Zero beat

(f) D.C. supplies

10. POWER SUPPLIES

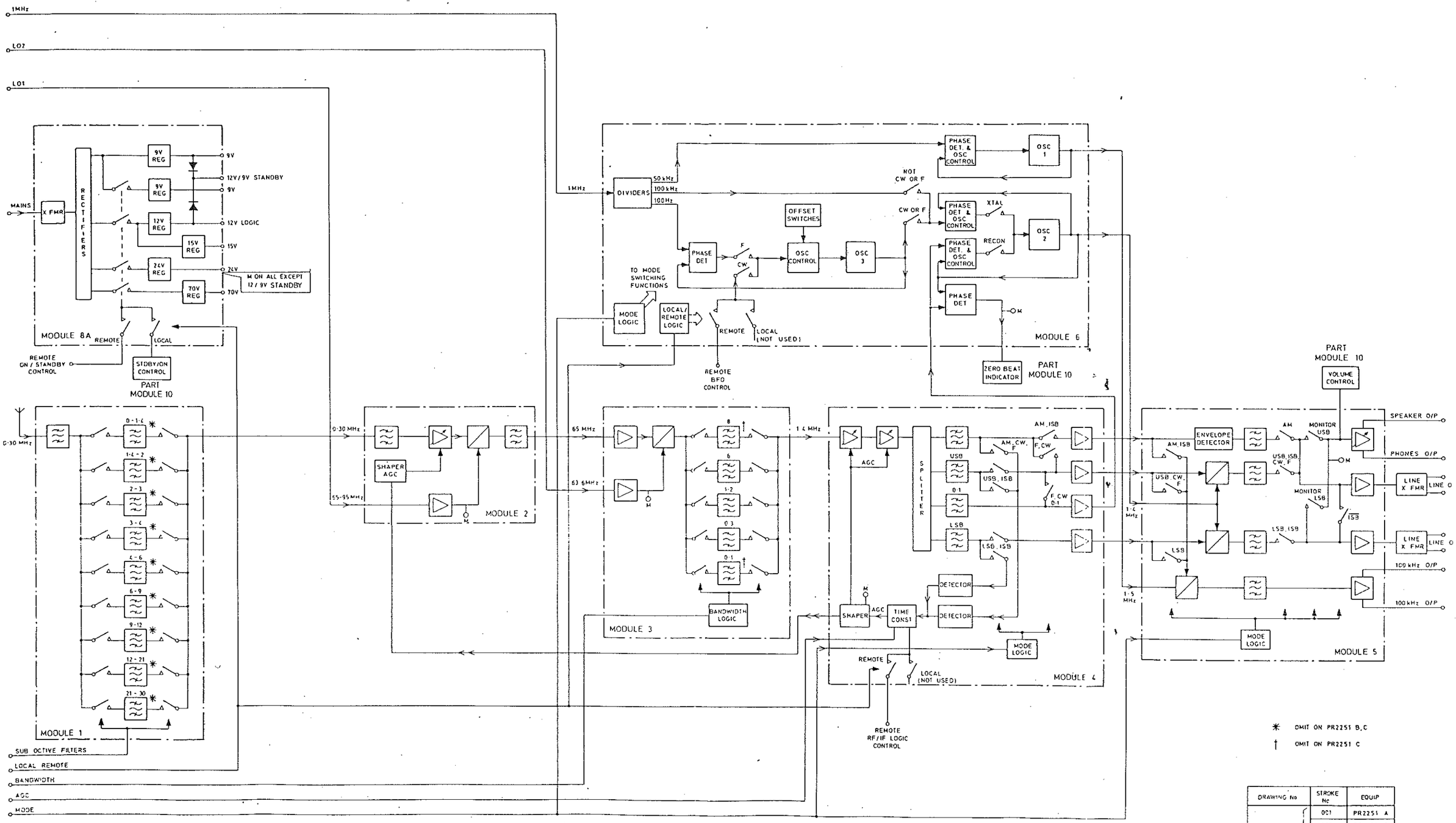
The power supplies are contained in Module 8A. The receiver is powered from a single-phase a.c. supply of any frequency between 45 and 450Hz. Voltage can be either between 105 and 130V or between 200 and 250V. Power consumption is 65VA. Either one of two power states can exist after the a.c. supply is connected: these are STANDBY and OPERATE. In standby certain circuits (such as the memory) are powered. All d.c. outputs are fully regulated and protected.



DRAWING No	STROKE No	EQUIP
630/DE/33000	001	PR2250A
	002	PR2250B
	003	PR2250C
	004	PR2250D
	005	PR2250E
	006	PR2250F

PR2250 FUNCTIONAL BLOCK DIAGRAM

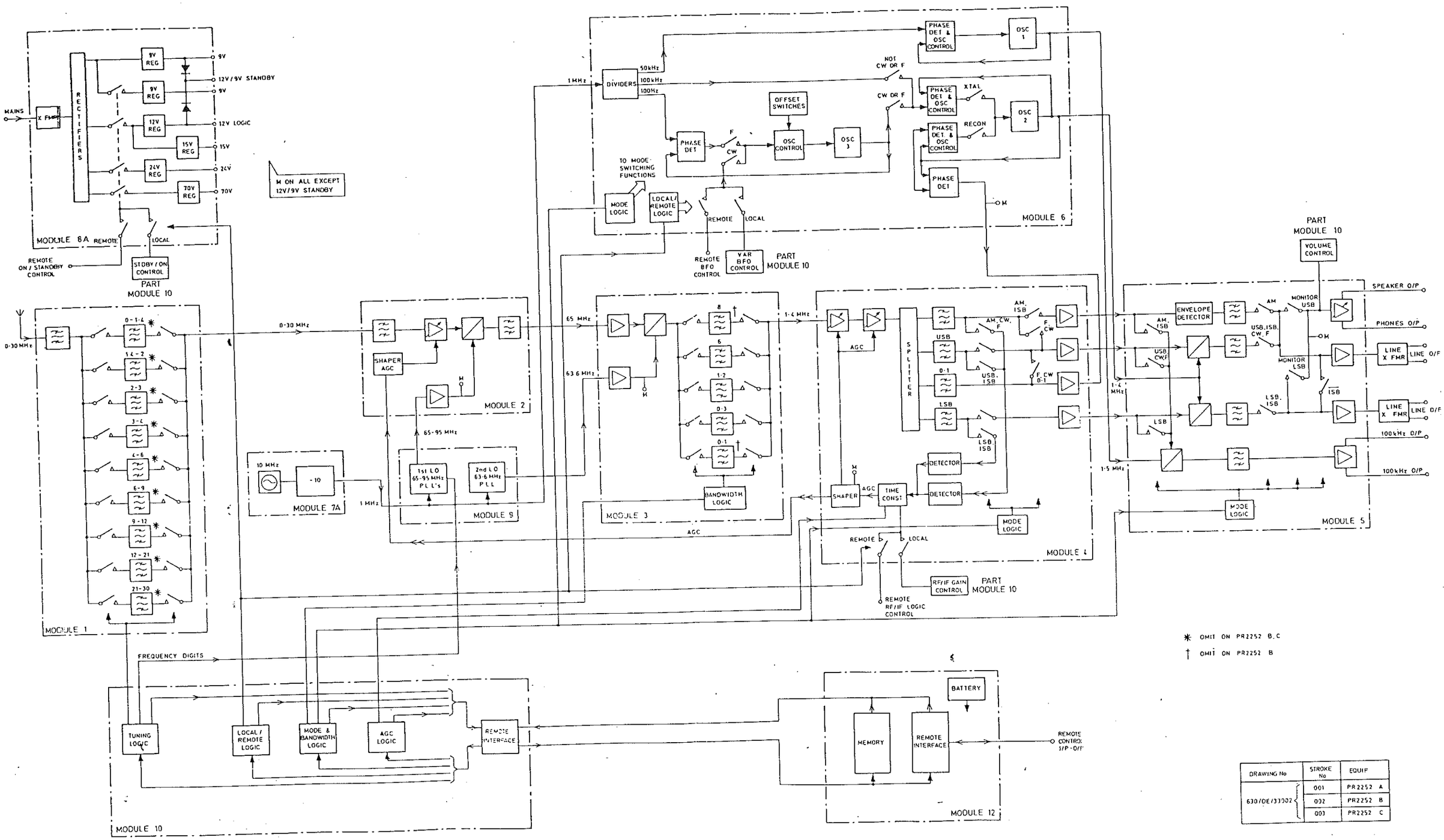
FIG 1



DRAWING No	STROKE No	EQUIP
633/DE/33001	001	PR2251 A
	002	PR2251 B
	003	PR2251 C

PR 2251 FUNCTIONAL BLOCK DIAGRAM

FIG 2



✱ OMIT ON PR2252 B,C

† OMIT ON PR2252 B

DRAWING No	STROKE No	EQUIP
630/DE/33002	001	PR2252 A
	002	PR2252 B
	003	PR2252 C

PR 2252 FUNCTIONAL BLOCK DIAGRAM

FIG 3

CHAPTER 1

MECHANICAL DESCRIPTION

CONTENTS

CONTENTS LIST (Cont'd)

ILLUSTRATIONS

MECHANICAL DESCRIPTION

1. INTRODUCTION

1.1 This chapter covers the receiver from the mechanical standpoint. The structure of each separate major item is described in descending order of mechanical complexity, and dismantling instructions are given where applicable.

1.2 The receiver is made throughout to metric standards. All dismantling can be carried out with tools commonly available in an electronics maintenance workshop.

1.3 The receiver uses an a.c. power supply cable which is coded to current British Standards. The electronics of the receiver employ CMOS components. Handling warnings on these two points are given on page (iv) of this manual.

2. RECEIVER FRAME

2.1 General

The receiver frame is a welded aluminium alloy box structure which houses the various modules and to which all interconnection wiring is secured. The front of the structure is closed by the hinged front panel (Module 10, 10A, or 10B).

2.2 Structure

2.2.1 The receiver frame is a welded box structure of 2.6 mm (12SWG) aluminium alloy sheet, open at both front and rear. The interior of the receiver is divided into three compartments by vertical aluminium alloy sheet bulkheads which are also secured to the case and to each other. Plastic runner rails to carry the various modules are sprung into place in holes punched in the upper and lower surfaces of the box structure. At each side of the frame a handle is secured to two machine screws.

2.3 Interconnection Harness

2.3.1 All interconnection wiring mounted on the receiver frame is situated on the two internal bulkheads and on the rear door. These items, together with the wiring and components carried on them, form Connector and Routing Board Assembly 630/1/32965. The layout of the harness is shown in diagrammatic form in Figure (a).

2.3.2 The harness is essentially built round a rigid routing board on the 'fore and aft' internal bulkhead of the receiver frame, and a multiway flexible connector on the transverse internal bulkhead of the receiver frame. These two groups of connections join at the junction of the two bulkheads, the flexible connector being soldered to pins on the rigid routing board to produce a 'T' of connections.

2.3.3 The front end of the routing board carries two multi-pin plugs which mate with the sockets on two of the flexible connectors on Module 10. The rear end of the routing board carries a multiway flexible connector which terminates in a multi-pin socket which mates with the corresponding plug on Module 9. Near the rear end of the routing board a small conventional cable harness runs from the routing board to the multi-pin sockets on the rear door.

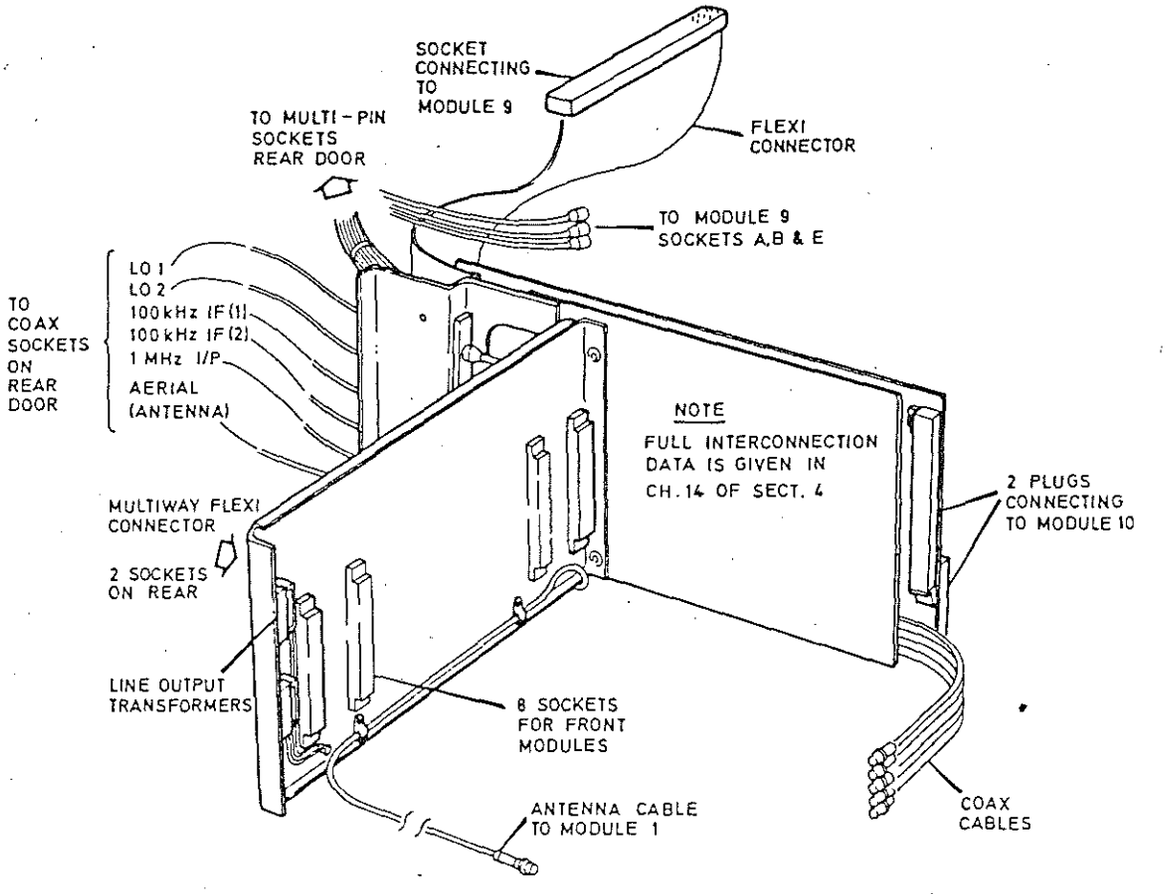


FIG (a) INTERCONNECTION HARNESS LAYOUT

2.3.4 The flexible connector clamped to the transverse bulkhead carries a total of ten multi-pin sockets into which all modules except Module 9 are plugged. At its extreme end, it carries the two line output transformers associated with the 'Line' outputs from Module 5.

2.3.5 Co-axial cabling is run alongside the two bulkheads, as can be seen from Figure (a). The antenna cable runs directly from the rear door to the connector which mates with Module 1: the remainder pass via a small plate carrying connectors which can be separated easily if required.

2.3.6 A full statement of all interconnections can be found in Section 4, Chapter 14, 'Interconnections'.

2.3.7 All connections on the rear door terminal strip are made by 4BA machine screws (3.6mm (0.142ins) dia., 38.5 TPI), which are very near to 6-40NF. Terminal tags having a 3.7mm (or No 26 drill) hole or fork spacing should be employed.

3. MODULES 10, 10A, AND 10B

3.1 General

This description covers Modules 10, 10A and 10B, as Modules 10A and 10B only differ from Module 10 in respect of the omission of some items. Module 10 is used in PR2250 receivers, Module 10A is used in PR2251 receivers, and Module 10B is used in PR2252 receivers.

3.2 Structure

3.2.1 Module 10 consists in essentials of three basic items; the front-panel, a pressed sheet-metal chassis, and a frame carrying a large printed-circuit panel. The front-panel is hinged to the receiver frame, and is held shut by two 1/4-turn DZUS fasteners situated in the two left-hand corners. The chassis is secured to the front-panel by four slot-head machine-screws; these are the four chrome-plated screws visible at the corners of the front-panel. A frame carrying a large printed-circuit panel is hinged to the lower edge of the chassis: it is held closed by a single captive screw at the top centre.

3.2.2 The front-panel display and control components are mounted either on the front-panel itself or on the chassis immediately behind it. The majority of the wiring is in the form of flat flexible multiway connectors. Removal and replacement of control components appears at first sight to be difficult, but is not so provided that the procedures laid down under 'Dismantling' are followed.

3.3 Electronic Servicing

3.3.1 Electronic servicing normally requires no mechanical dismantling during the diagnostic stage, but does require access to components. To gain access to components mounted on the large printed-circuit panel, release the two DZUS fasteners which secure the front-panel and swing the front panel open. Note that there is no catch to hold the front-panel in the open position.

3.3.2 To reach the track side of the printed-circuit panel and some of the front-panel controls, release the captive screw at the top centre of the p.c. panel and swing the panel down to lie flat on the bench. It can swing through 180°, if required, to hang vertically downward without damage to wiring.

3.3.3 When lying flat on a bench, the corner of the p.c. panel can foul the front of the receiver case. It is advisable to engage the boss of the top left-hand p.c. panel fixing screw in the first groove in the bottom of the receiver frame: this forms a support and helps to stop the front-panel swinging. Be careful not to let the p.c. panel rest on the front of the receiver frame with integrated circuit IC62 acting as a 'stop'; this produces forces which attempt to twist IC62 out of its socket.

3.4 Dismantling

3.4.1 Flexible Multiway Connectors.

Removal of a component may involve disconnecting a flexible multiway connector, either totally or in part. The terminations of these connectors are of two types; some are soldered and some employ 'push on' pin connectors. Where components are attached to the flexible connectors the joints are soldered.

3.4.2 Unsoldering a joint on these flexible connectors must be carried out with de-soldering braid ('solder-wick'). To unsolder a joint, place the wick on the joint and then place the soldering-iron on top until the solder has melted from the joint and has run into the wick. Making a soldered joint on these connectors is the same as on any printed-circuit panel. When unsoldering a multi-pin termination, de-solder each connection in turn. When all are de-soldered, the termination can be removed. Short-term soldering temperature should not exceed 300°C. A 25 watt iron with a chisel-point bit no larger than 3mm (1/8ins) diameter is recommended.

3.4.3 To remove a 'push-on' termination the special tool supplied in the Servicing Kit should be used to gently lever the end of the flexible connector away from the panel. If the supplied tool is not available, a satisfactory substitute can be made from a piece of plastic or hardwood about 3mm (1/8ins) thick, tapered to a chisel-point at one edge as shown below in Figure (b). Use a hard plastic such as 'Perspex' or 'Plexiglas'. Do not use metal tools to remove connectors.

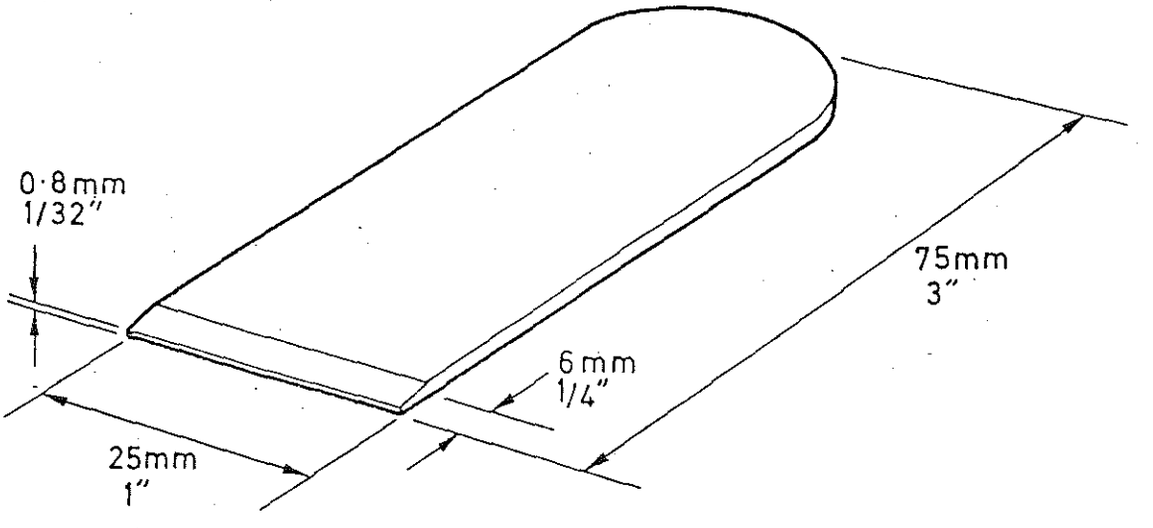


FIG (b) SUGGESTED CONNECTOR REMOVER TOOL

3.4.4 Frequency and Memory Displays

The Frequency and memory displays are mounted on the chassis. Each is secured to the chassis by two captive screws. To remove either display, remove the two captive screws. The display concerned can now be pulled straight out to the rear of the panel.

3.4.5 Chassis Removal

Before attempting to remove the chassis from the front-panel, detach Module 10 from the receiver frame. To separate the chassis from the front-panel, the knobs of the MONITOR, BFO, RF-IF GAIN and AUDIO GAIN controls must first be removed. Each is secured by two slot-head grub-screws at 90° to each other: the screwdriver blade should be 2.4mm (3/32ins) wide.

3.4.6 After removing the four knobs, support the chassis while removing the four slot-head chrome-plated screws visible at the corners of the front-panel. The chassis can then be separated from the front-panel. The front-panel carries the STANDBY-OPERATE switch, the power indicator LEDs, the speaker, the monitor meter, and the MANUAL TUNING optical encoder. The remainder of the front-panel controls are mounted on the chassis.

3.4.7 Rocker Switches

These are of two types; one type is used for the power switch, whilst another is used for the remainder. The power switch is mounted on the front-panel, and is held by two nylon snap clips. To remove, press together the clips and withdraw the switch from the front. The remainder are mounted on the chassis, which must be removed from the front-panel to change a switch. Each switch is secured by two nuts and bolts to the chassis.

3.4.8 Potentiometer Controls

In every case these items are secured by the usual nut on a threaded boss. Removal and replacement follows the conventional procedure.

3.4.9 Optical Encoder

This component is fixed to the front-panel by three M3 machine-screws. The MANUAL TUNING knob must be removed to expose these screws. When replacing the knob do not push it fully home on the shaft, as it will then rub against the encoder body: allow 1.5mm (1/16ins) clearance between the front-panel and the skirt of the knob.

3.4.10 LED Indicators

All LED indicators stand off on their own leads from their attachment points. When soldering a replacement LED in place, ensure that its position and lead length is such as to allow it to enter the appropriate front-panel hole easily. Use the jig provided in the servicing kit. All LED indicators except the two which indicate STANDBY and OPERATE are mounted on the chassis or on the display assembly; the two mentioned exceptions are mounted on the front-panel. The flat on the body of the LED is next to the cathode lead.

3.4.11 Push-button Controls

All push-button controls are mounted on the chassis, but the chassis need not be removed from the front panel to change a push-button. Each component is held by the two pins on its rear surface being soldered to a printed-circuit strip. To remove a component, de-solder the two connections and pull it straight out through the front-panel. The knob is a push fit on the control, and must be transferred to the new component. The new component is then inserted through the front-panel until its two

pins are visible through the appropriate holes in the printed-circuit strip. With an assistant holding the push-button down (i.e. pressed), solder the two pins to the strip. Cut off any excess pin length which protrudes after soldering.

3.4.12 Speaker

The speaker is attached to the back of the front-panel by nuts on four fixed studs. The grille and protective cloth are held between the speaker and the panel. It is necessary to separate the chassis from the front-panel to reach the fixing nuts.

3.4.13 Monitor Meter

The monitor meter is secured to the chassis by nuts on two 4-40UNC studs integral with the meter. These studs enter the chassis from the front. To remove the meter, take off the nuts from these studs and pull the meter out through the front of the panel.

4. MODULE 9

4.1 General

Module 9 is structurally more complex than the remainder of the modules. It consists in essentials of a metal box carrying a motherboard into which plug fourteen printed-circuit panels. The box provides a high level of r.f. screening which is vital to the operation of the receiver.

4.2 Structure

4.2.1 Module 9 consists of a brazed metal case carrying a motherboard on which are fourteen connectors. The assembly can be seen in Figure 1. A printed-circuit panel plugs into each connector, and all fourteen are held in place by a sheet metal cover plate secured by M2.5 machine-screws. The motherboard side of the box is enclosed by a similar coverplate. At one end of the box structure a separate cover protects a small printed-circuit panel and four power regulators. A multi-pin connector and six co-axial sockets carry the connections between Module 9 and the remainder of the receiver.

4.2.2 The r.f. screening provided by Module 9 box structure is vital to the operation of the receiver. If screening is inadequate due to missing cover screens or crinkle washers, the receiver cannot be guaranteed to meet its performance specification in respect of spurious responses and antenna re-radiation of local oscillator frequencies.

4.3 Dismantling

4.3.1 Testing of any one of the fourteen plug-in printed-circuit panels is carried out by mounting it on an extender card which is supplied in the receiver servicing kit. The top cover-plate is first removed by detaching either M2.5 machine-screws and crinkle washers: this exposes the fourteen p.c. panels. Note that they, and their sockets, are 'letter' coded but do not run in alphabetical order.

4.3.2 Each p.c. panel is held between runner rails, and is a push fit into an edge connector socket on the motherboard. Always insert or remove a panel with a straight push (or pull). Always use the removal tool from

the side of the case. Bending a printed-circuit panel beyond a very small amount may cause cracking; such cracks can develop later into intermittent faults which are difficult to diagnose and even more difficult to repair.

4.3.3 Access to the motherboard (PCB2) is gained by removing the bottom cover-plate. Normally no further dismantling is necessary, but if it should be necessary to remove the motherboard this can be done by first unsoldering the lines from the six co-axial sockets and from the multi-pin connector and then removing the machine-screws which secure the motherboard. The panel can then be lifted out. Never remove the motherboard without first making a clear sketch of the connections to be removed.

4.3.4 The small printed-circuit panel (PCB1) and the four power regulators can be reached by removing the small end cover: the panel is secured by two machine-screws. Each power regulator is secured to the main frame (employed here as a heat-sink) by a single machine-screw. Regulators IC1, IC2, and IC3 are in direct contact with the frame; IC4 is insulated from the frame by a square plastic washer and by a flanged insulating bush between the regulator and the retaining screw. In all four cases a film of heat-sink compound is applied in the manner usual for such assemblies.

5. MODULE 8A

5.1 General

Module 8A is the power supply unit and, when installed in the receiver, its rear face is exposed. This face carries the a.c. power input socket, the a.c. power voltage-selector panel, and the various power fuses.

5.2 Structure

5.2.1 The components of Module 8A are fitted on five of a total of six rectangular aluminium alloy plates, and are connected by a cable-harness which links the five plates. One plate carries a further assembly which houses regulators IC1, IC2, REC1, 2, and 3; this assembly is also linked by the harness to the remainder.

5.2.2 The six plates assemble into a rigid box structure. They are secured by machine screws which engage with the four square section bars mounted on the rear plate.

5.3 Dismantling

5.3.1 The layout of the items can be seen in Figure 2. After removing all machine screws, the whole module can be 'unfolded' to lay flat on a workbench with all electrical components facing upwards. Power may be applied for test purposes while the module is in this state, but it must be remembered that live a.c. power points are then exposed.

5.3.2 It is not always necessary to fully dismantle the module: the printed-circuit panel can be reached by unfastening the top plate only, and visual inspection can be carried out by removing either the top plate or a side plate.

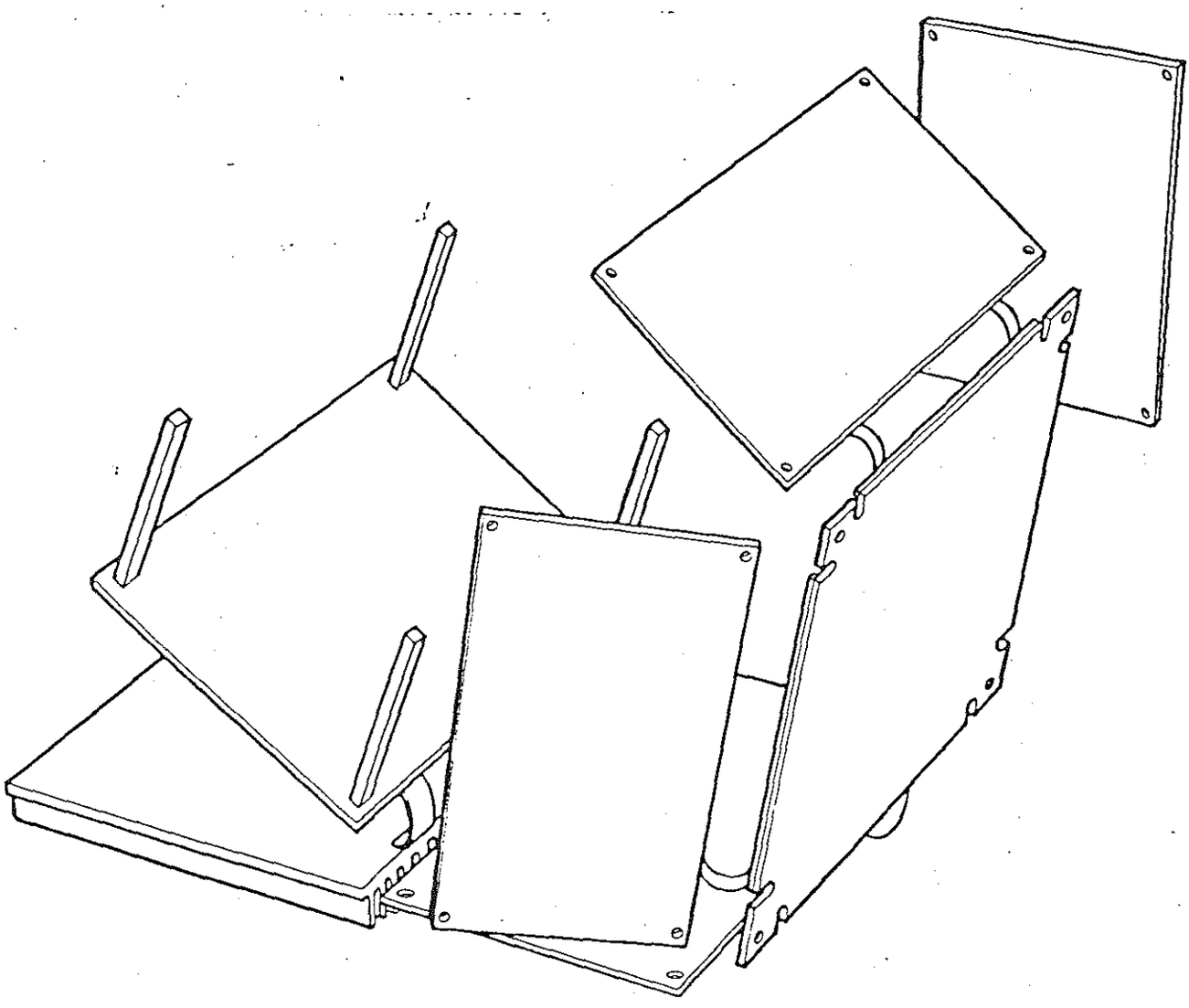


FIG (c) MODULE 8A BASIC STRUCTURE

6. MODULE 12

6.1 General

Module 12 is similar to the single-p.c.b. modules in construction, except that it houses two printed-circuit panels.

6.2 Structure

6.2.1 The module frame consists of two end-plates connected by four lengths of aluminium alloy section. Each end-plate is secured by four pan-head cross-point self-tapping screws. Each length of alloy section forms a rail which slides in a receiver frame groove to act as a runner and as a locking key.

6.2.2 Each side of the frame is closed by an aluminium alloy sheet cover secured to the frame by four self-tapping screws.

6.2.3 Each printed-circuit panel is 187mm (7 3/8 ins) line by 146mm (5 3/4 ins) wide. On each, a projecting edge-connector occupies one short side. These edge-connectors project through cut-outs in the sides of the frame back-plate to form module-to-chassis connectors. Each panel is secured to the frame rails by four self-tapping screws.

6.2.4 A multi-pin connector is mounted on hexagonal spacers behind the front end-plate and lies behind a slot in the front end-plate. This connector and the two printed-circuit panels are linked by a wiring harness.

6.2.5 A rechargeable battery is mounted on the inner surface of the rear back plate.

6.3 Dismantling

All components are mounted on the inner sides of the printed-circuit panels, and therefore access can only be gained by removing a cover and one printed-circuit panel. NOTE. It is not expected that electronic fault-finding to component level will be carried out on Module 12, as diagnosis in a micro-processor controlled circuit involves the use of a computer to replace the microprocessor. Module 12, if faulty, should be replaced on a manufacturer's 'service exchange' basis.

7. SINGLE PCB MODULES

7.1 General

This description is common to all modules except 8A, 9, 10 and 12. Modules 2 and 7A vary slightly in some respects, and these variations are covered in the text of this description.

7.2 Structure

7.2.1 The module frame consists of two end-plates connected by two lengths of aluminium alloy section. Each end-plate is secured by two pan-head cross-point self-tapping screws. Each length of alloy section forms a rail which slides in a receiver frame groove to act as a runner and as a locating key.

7.2.2 One side of the frame is closed by a flat aluminium alloy sheet secured to the frame by self-tapping screws; this covers the 'non-component' side of the printed-circuit. The other side is covered by a folded aluminium alloy sheet secured to the frame by self-tapping screws; this covers the 'component' side of the printed-circuit.

7.2.3 On Module 2, high dissipation transistors are used: these require heat-sinks. The transistors are mounted on the 'non-component' side of the printed circuit, and fit into cylindrical heat-sinks secured to the flat cover-plate. Each heat-sink is secured to the cover plate by a 6BA (2.8mm (0.1102 ins) dia 47.9 TPI) screw and insulating bush, and can move about ± 0.5mm (±.020ins) from its nominal position to allow for slight component and printed-circuit dimensional tolerances.

7.2.4 The printed-circuit panel is 175mm (6 7/8ins) long by 146mm (5 3/4ins) wide. Except in Module 7A, a projecting edge-connector occupies one short side. This edge-connector projects through a slot on the frame back-plate to form the module-to-chassis connection. Module 7A employs a multi-pin connector in place of the edge-connector.

7.2.5 The printed-circuit panel is secured to the frame rails by four self-tapping screws; in some modules it is held clear of the rails by tubular spacers. The panel is of glass re-inforced plastic, and carries tracks on both sides.

7.3 Dismantling

7.3.1 Removal of a printed-circuit panel from the frame is not necessary for normal servicing and component replacement.

8. INTERFACE MODULE

8.1 General

The interface module is installed at the rear of the receiver, next to Module 8A.

8.2 Structure

The module consists of an end plate which is secured to the chassis by means of two captive screws. Two brackets are mounted on the plate, to hold the p.c.b. in place. A multi-core cable from the p.c.b. leaves the end plate via a rubber grommet and terminates in a 50-way plug, PL2. A 50-way plug, PL1, is mounted on the end plate by means of two bolts.

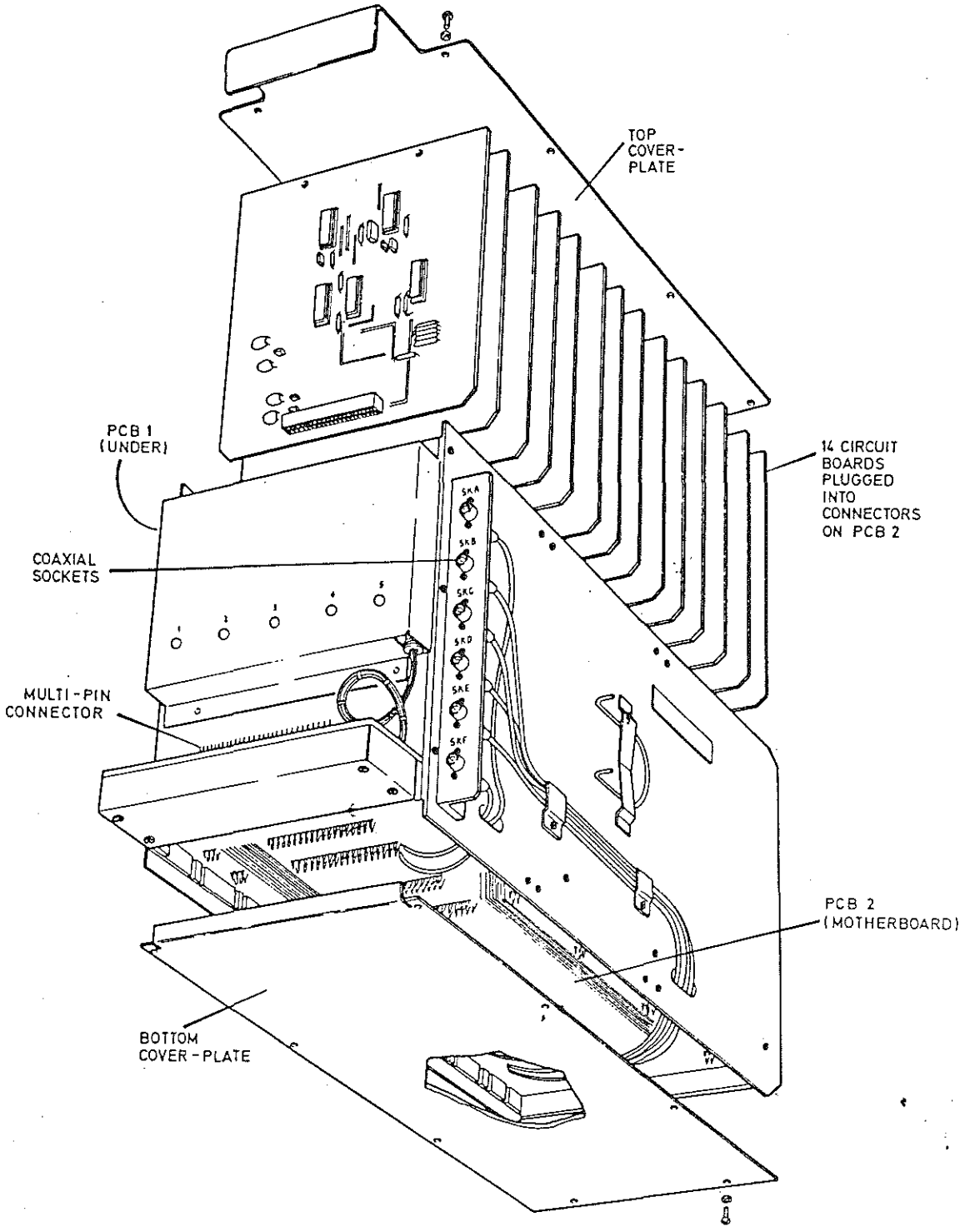
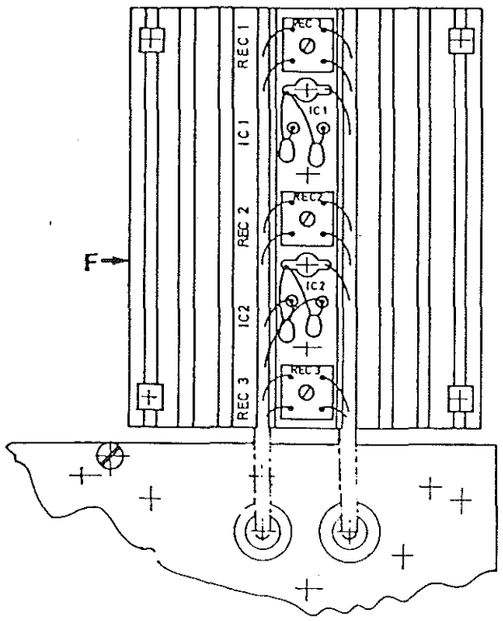
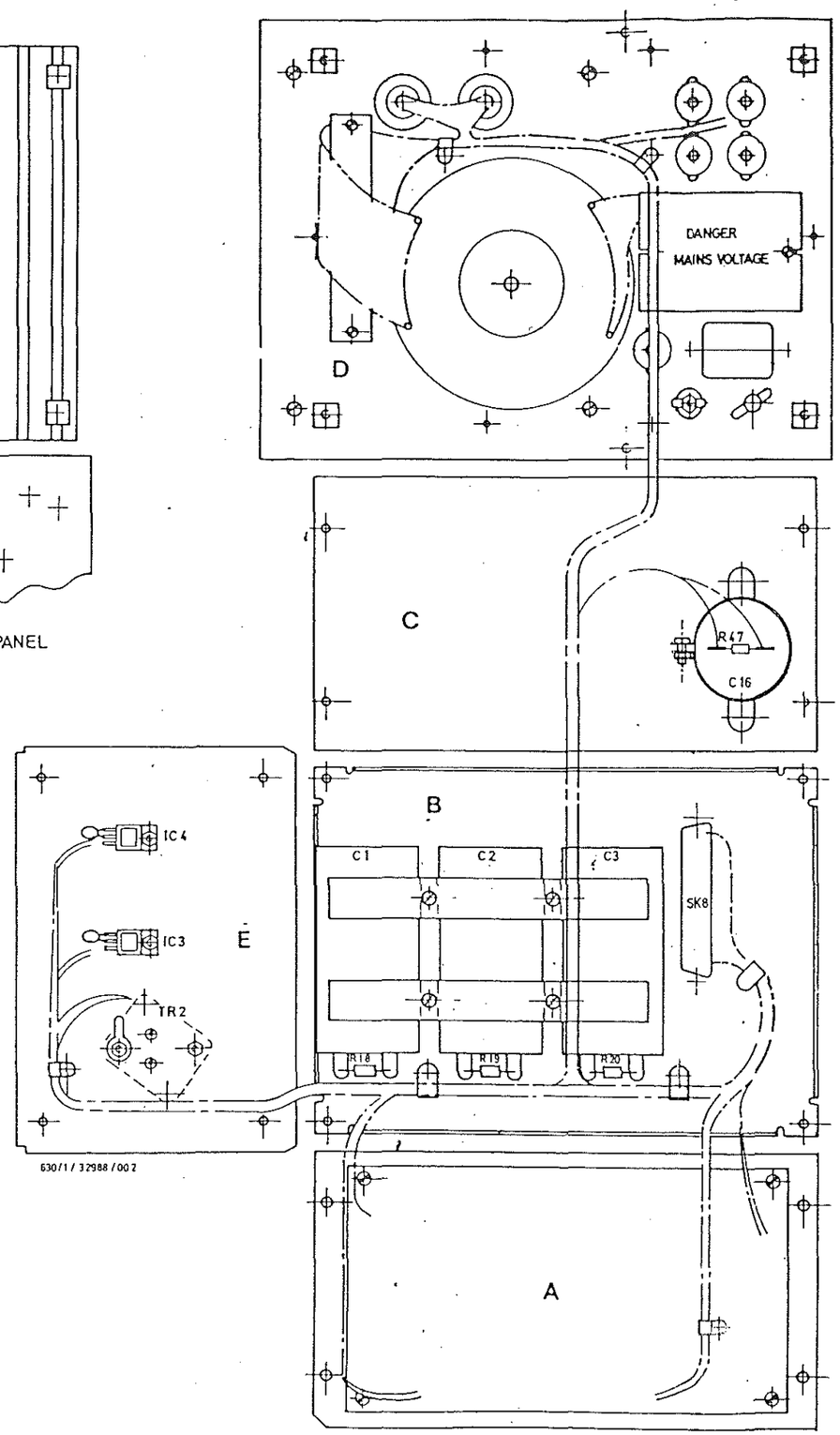
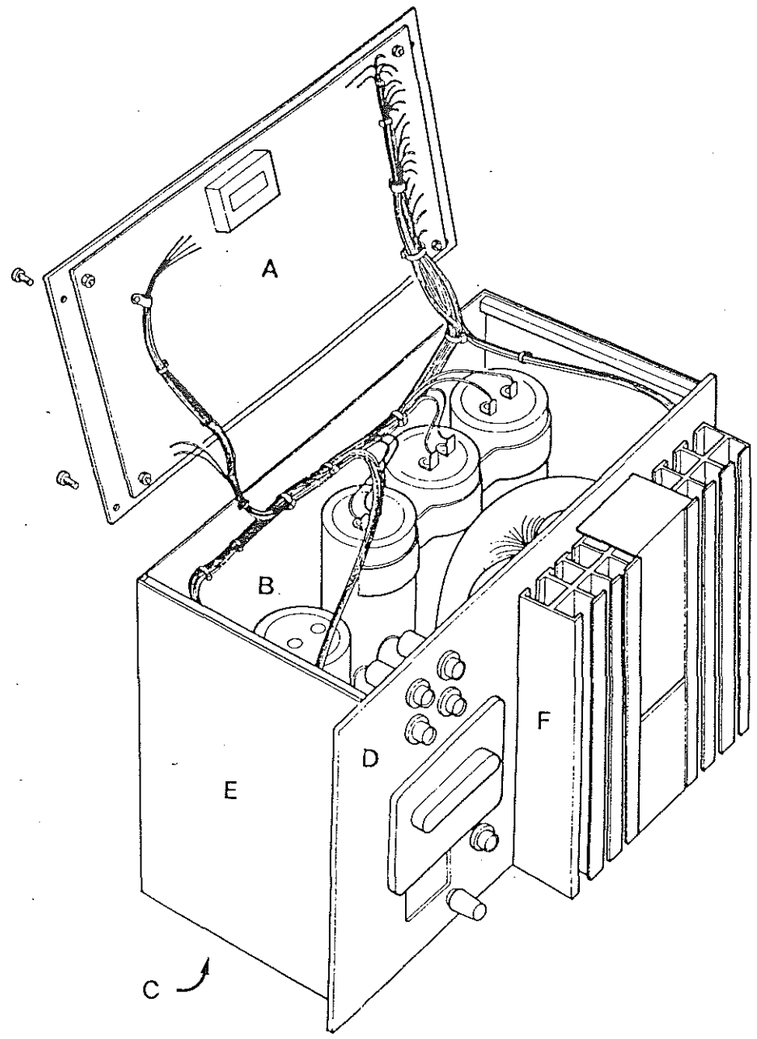


FIG.1 MODULE 9 EXPLODED VIEW



VIEW OF HEATSINK & FRONT PANEL





MODULE 8A PHYSICAL CONSTRUCTION

FIG 2

CHAPTER 2

RECEIVER BODY COMPONENTS LISTS

CONTENTS

Receiver Assembly Series

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	HF Receiver Assembly	Plessey PR2250A	630/1/33000/001
-	HF Receiver Assembly	Plessey PR2250B	630/1/33000/002
-	HF Receiver Assembly	Plessey PR2250C	630/1/33000/003
-	HF Receiver Assembly	Plessey PR2250D	630/1/33000/004
-	HF Receiver Assembly	Plessey PR2250E	630/1/33000/005
-	HF Receiver Assembly	Plessey PR2251A	630/1/33001/001
-	HF Receiver Assembly	Plessey PR2251B	630/1/33001/002
-	HF Receiver Assembly	Plessey PR2251C	630/1/33001/003
-	HF Receiver Assembly	Plessey PR2252A	630/1/33002/001
-	HF Receiver Assembly	Plessey PR2252B	630/1/33002/002
-	HF Receiver Assembly	Plessey PR2252C	630/1/33002/003

Receiver Assembly

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	HF Receiver Assembly	Plessey	630/1/33300/---- (from above)
-	Case Assembly	Plessey	630/1/32979
5B-4D	Connector Assembly	Plessey	702/1/20092/001
5C-6A	Connector Assembly	Plessey	702/1/20092/002
5D-4E	Connector Assembly	Plessey	702/1/20092/003
2C-3A	Connector Assembly	Plessey	702/1/20092/004
3B-4A	Connector Assembly	Plessey	702/1/20092/005
5A-4C	Connector Assembly	Plessey	702/1/20092/006
SKD-9B	Connector Assembly	Plessey	702/1/20092/007
SKE-9C	Connector Assembly	Plessey	702/1/20092/008
5E-6C	Connector Assembly	Plessey	702/1/20092/009
1H-2A	Connector Assembly	Plessey	702/1/20092/010
9F-SKA	Connector Assembly	Plessey	702/1/20092/011
4F-6E	Connector Assembly	Plessey	702/1/20092/012
6F-12C	Connector Assembly (2250B,D,F and 2252 only)	Plessey	702/1/20092/013
7A-Rear Door	Connector Assembly	Plessey	702/1/33364/001

Case Assembly (630/1/32979)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Routing board and Connector Plate Assembly	Plessey	630/1/32965/002
-	Tie Block	Plessey	630/2/35349
-	Frame Assembly	Plessey	630/1/33040

Routing Board and Connector Plate Assembly (630/1/32965)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Connector Plate Comp. Assy.	Plessey	630/1/32934
-	Divider Plate Assembly	Plessey	630/1/32938
-	Stop Plate Assembly	Plessey	630/1/32942
-	Bracket Assembly	Plessey	630/1/32945
-	Routing Board Assembly	Plessey	419/9/18116
-	Connector Assembly	Plessey	702/1/20091/001
-	Connector Assembly	Plessey	702/1/20091/002
-	Connector Assembly	Plessey	702/1/20091/003
-	Connector Assembly	Plessey	702/1/20091/004
-	Connector Assembly	Plessey	702/1/20091/005
-	Connector Assembly	Plessey	702/1/20097/001
-	Connector Assembly	Plessey	702/1/20097/002
-	Connector Assembly	Plessey	702/1/20097/003
-	Connector Assembly	Plessey	702/1/20097/004
-	Connector Assembly	Plessey	702/1/20097/005
-	Connector Assembly	Plessey	702/1/33385
-	Cableform Assembly	Plessey	702/1/33366
-	Cableform Assembly	Plessey	702/1/33367
-	Hinged Rear Panel Assembly	Plessey	630/1/33035
-	Retaining Plate	Plessey	630/1/32966
-	Spacer	Plessey	630/2/33060
-	Clamping Strip	Plessey	630/2/32996
-	Plug, Electrical Fixed	Cannon DC37P 37 way	508/4/28179/002
-	Socket Electrical Fixed	Cannon DE9S 9 way	508/4/22145/010
-	Socket Electrical Fixed	Cannon DD50S 50 way	508/4/28010/008
-	Sliding Lock Assembly	Cannon DE51224-1	508/4/28865/001
-	Sliding Lock Assembly	Cannon DD51223-1	508/4/28865/005
-	Sliding Lock Post	Cannon D53018	508/4/29198
	Terminal Board 12 way	Cinch R44/77/903D/12M	703/4/98025/011
-	Terminal Lug	Tucker G369-4	703/9/98048/018

Connector Plate Component Assembly (630/1/32934)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Connector Plate Assembly	Plessey	630/1/32961
-	Securing Block	Plessey	630/1/32973
-	Socket, Electrical 24 x 24 way	Cannon G05 Edge Conn.	508/4/22097/002
-	Socket, Electrical 24 way	Cannon G05 Edge Conn.	508/4/22097/001
-	Transformer AF	Gardner Type AM106	406/4/31756/007
-	Terminal Lug	Ross Courtney Type 201051XM3	703/9/03812/014

Divider Plate Assembly (630/1/32938)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Divider Plate	Plessey	630/1/32937

Stop Plate Assembly (630/1/32942)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Stop Plate	Plessey	630/2/32941

Bracket Assembly (630/1/32945)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Bracket	Plessey	630/2/32944

Connector Assemblies (702/1/20091/001 to /005)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Plug, Electrical RF Free	Belling Lee L1465A/K/FP	508/9/21838
-	Socket, Electrical RF Free	Belling Lee L1465/K/BS	508/4/22059
-	Cable R.F.	Suhner RF174/U 330 mm	998/4/70537/001

Connector Assemblies (702/1/20097/001 to /005)

Circuit Ref.	Description and Tolerance	Manufactuer and Ref.	Part No.
-	Socket, Electrical RF Fixed	Belling Lee BLL004/0703	508/4/22133
-	Plug, Electrical RF Fixed	Belling Lee L1465A/K/FP	508/9/21838
-	Cable RF	Suhner RF174/U 530 mm	998/4/70537/001

Rack Mounting Kit (630/1/33023)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Runner Telescopic Kit	Plessey	675/9/27806
-	Bag Linen	Plessey	992/4/01082
-	Special Screw	Plessey	999/4/02339/002
-	Adaptor Plate	Plessey	630/2/32245

CHAPTER 3

PR2250 SERIES DEFINITION

CONTENTS

TABLES

PR2250 SERIES DEFINITION

1. GENERAL

1.1 This chapter defines fully in tabular form the PR2250 series of receivers. There are three basic models at the time of publication; PR2250, PR2251, and PR2252. Each model can be supplied in a number of variants, each variant being identified by a letter suffix, e.g. PR2250B.

1.2 To cater for these variations, Modules 1, 3 and 10 are produced in 1A, 3A, and 10A and 10B forms. Table 1 defines the module content of PR2250 receivers, Table 2 defines the module content of PR2251 receivers, and Table 3 defines the module content of PR2252 receivers. Table 4 outlines the circuit of all modules.

TABLE 1 : PR2250 RECEIVERS - MODULE CONTENT

MODULES FITTED	PR2250					
	A	B	C	D	E	F
	1	1	1A	1A	1A	1A
	2	2	2	2	2	2
	3	3	3A	3A	3	3
	4	4	4	4	4	4
	5	5	5	5	5	5
	6	6	6	6	6	6
	7A	7A	7A	7A	7A	7A
	8A	8A	8A	8A	8A	8A
	9	9	9	9	9	9
	10	10	10	10	10	10
	11	-	11	-	11	-
	-	12	-	12	-	12

TABLE 2 : PR2251 RECEIVERS - MODULE CONTENT

	PR2251		
	A	B	C
MODULES FITTED	1	1A	1A
	2	2	2
	3	3A	3
	4	4	4
	5	5	5
	6	6	6
	8A	8A	8A
	10A	10A	10A
	I.F.	I.F.	I.F.

TABLE 3 : PR2252 RECEIVERS - MODULE CONTENT

	PR2252		
	A	B	C
MODULES FITTED	1	1A	1A
	2	2	2
	3	3A	3
	4	4	4
	5	5	5
	6	6	6
	7A	7A	7A
	8A	8A	8A
	9	9	9
	10B	10B	10B
	12	12	12

TABLE 4 : OUTLINE CIRCUIT CONTENT OF MODULES

MODULE	BASIC	A	B
1	Sub-octave and 30MHz LP Filters	30MHz LP Filter	-
2	1st Mixer, 65MHz 1st IF Filter	-	-
3	2nd Mixer, 1.4MHz 2nd IF Filters; 8, 6, 1.2, 3, and 0.1kHz	2nd Mixer, 1.4MHz 2nd IF Filters: 6, 1.2, and 0.3kHz	-
4	2nd IF amp., 3kHz SSB Filters. 0.1kHz filter	-	-
5	Audio processing	-	-
6	BFO, Recon. Car., ± 8kHz range internally set in binary	-	-
7A	1MHz ref source	-	-
8A	Power Supply Unit	-	-
9	Synthesiser; LO1, 65-95MHz: LO2 63.6MHz	-	-
10	Front panel, Mode, AGC, B/W, Freq. set, encoder manual controls	Front panel with monitor controls only and no control logic	Front panel with monitor controls only and full control logic for remote operation
11	Memory	-	-
12	Remote control and memory	-	-
I.F.	Control interface	-	-

CHAPTER 1

MODULES 1 AND 1A : RF FILTERS

CONTENTS

TABLES

ILLUSTRATIONS

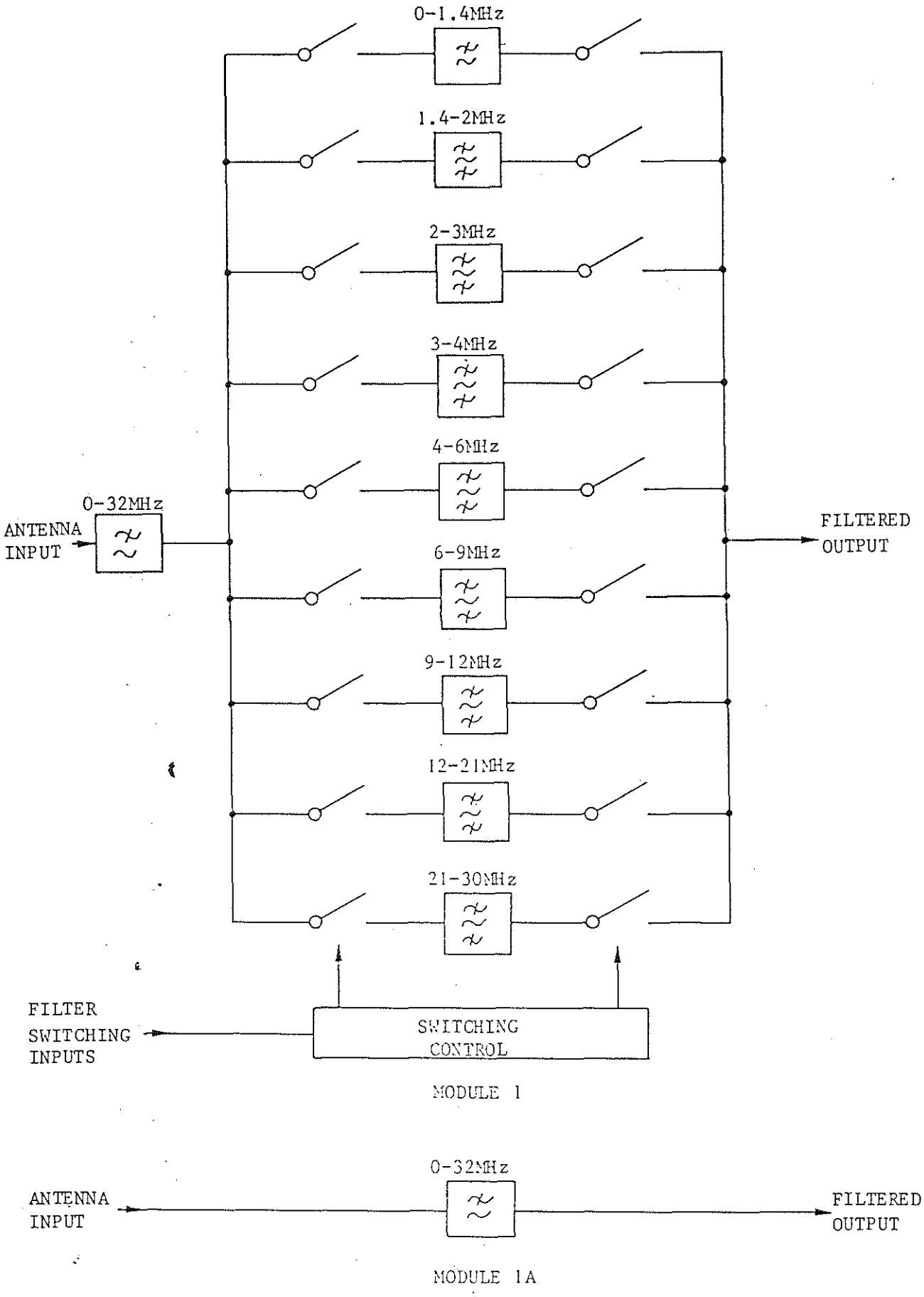


FIG. (a) MODULES 1 AND 1A FUNCTIONAL BLOCK DIAGRAM

MODULES 1 AND 1A : RF FILTERS

1. FUNCTIONAL DESCRIPTION

1.1 Modules 1 and 1A contain the r.f. filters via which the antenna input is applied to the r.f. amplifier in Module 2. Module 1 is used in the PR2250A, PR2250B, PR2251A, and PR2252A receivers and contains 8 band-pass filters, one low-pass filter, and one input low-pass filter. Module 1A is used in the PR2250C, PR2250D, PR2250E, PR2250F, PR2251B, PR2251C, PR2252B and PR2252C receivers, and contains one low-pass filter.

1.2 Functional block diagrams of Modules 1 and 1A are shown in Figure (a). In Module 1, one of the band of nine filters is automatically connected in circuit by the operation of the receiver tuning. In Module 1A, a single low-pass filter is permanently connected in circuit.

2. CIRCUIT DESCRIPTION

2.1 Module 1

2.1.1 Module 1 is used in PR2250A, PR2250B, PR2251A, and PR2252A receivers. The antenna signal is applied via SKA to a low-pass filter formed by L72, L73, and L74 together with associated capacitors; 3dB point is 32MHz. The output from L74-C127 junction is applied via RL1 to the input of a 1.4MHz high-pass filter formed by L11, L12 and L14, together with associated capacitors. The purpose of this 1.4MHz high-pass filter is to reduce the high noise levels generated below 1.4MHz; a large amount of noise is generated below this frequency, which the higher frequency band-pass filters will not alone reject.

2.1.2 The output of the 1.4MHz high-pass filter is applied to the inputs of a 2MHz low-pass filter and seven band-pass filters, one of which is switched into circuit according to the receiver tuning setting. The 3dB points of the nine filters are:-

(1) 1.5MHz (low-pass)

(2) 1.3MHz and 2.1MHz)
(3) 1.9MHz and 3.1MHz)
(4) 2.9MHz and 4.1MHz)
(5) 3.9MHz and 6.1MHz) (band-pass)
(6) 5.9MHz and 9.1MHz)
(7) 8.9MHz and 14.1MHz)
(8) 13.9MHz and 21.1MHz)
(9) 20.9MHz and 30.1MHz)

2.1.3 The inputs and outputs of the input low-pass filter are switched by RL1 and RL2 under the control of the CMOS logic level applied to edge-pin 19. A '1' level applied to pin 19 connects the filter. Relay switching is used on this filter as the PIN diode method is not suitable for frequencies below 1MHz.

2.1.4 The inputs and outputs of the 2MHz low-pass filter and seven band-pass filters are switched by PIN diodes D1 to D16. All are held reverse-biased by the potential across R45 applied to their cathodes; anode potentials follow the emitter potentials of the switching transistors, which are OV for a logic '0' control input. When a logic '1' control input is applied to a switching transistor, emitter potential rises and renders the associated pair of PIN diodes conductive. All outputs are connected via d.c. blocking capacitor C128 to SKH.

2.2 Module 1A

Module 1A is used in PR2250C, PR2250D, PR2250E, PR2250F, PR2251B, PR2251C, PR2252B, and PR2252C receivers. The antenna signal is applied via SKA to a low-pass filter identical with that formed by L72, L73, and L74 (and associated capacitors) in Module 1. The output from this filter is connected directly to SKH. The module contains no other circuitry.

3. TEST DATA

The procedures outlined in the following paragraphs form a complete test procedure and need not be used to locate individual faults on the module.

3.1 List of Test Equipment

Signal Generator range 10kHz-50MHz, O/P level of 100mV EMF into 50 ohms. Frequency Counter (up to 35MHz) e.g. Racal 9911.

R.F. Millivoltmeter, range 1 to 100mV, frequency range 100kHz to 30MHz 50 ohm load.

Polyskop. (Test equipment which will display the response curve of a tuned circuit, i.e. a frequency swept oscillator combined with a suitable display). These tests are written on the assumption that a Rhode & Schwarts polyskop is used.

3.2 Alignment and Functional Tests

3.2.1 The cores of the inductors in the Low Pass Filter section should be adjusted for minimum inductance, i.e. the cores fully unscrewed. Hence 'Cores out' for L4-6, L8-10, L17-19, L25-27, L33-35, L41-43, L49-51, L57-59, L65-67, L72-74. The cores of the inductors in the High-Pass Filter sections should be adjusted for maximum inductance, i.e. the cores fully screwed in. Hence 'Cores in' for L11-14, L20-22, L28-30, L36-38, L44-46, L52-54, L60-62, L68-70.

3.2.2 Connect the +15V supply to edge-pin 22 and OV to edge-pin 1. A +12V supply is required to generate a logic '1' level at each of the edge-pins shown in Table 1.

TABLE 1 : FREQUENCY INPUT CONNECTIONS

MHz Band	Edge-pin No.
0 - 1.4	19
1.4 - 2	14
2 - 3	7

continued ...

TABLE 1 continued ...

MHz Band	Edge-pin No.
3 - 4	5
4 - 6	6
6 - 9	15
9 - 14	16
14 - 21	4
21 - 30	3

3.2.3 Select '21-30'MHz by applying a +12V (logic 1) level to pin 3, and check that the current consumption of the +15V supply is 225 ± 50mA.

3.2.4 Connect the RF millivoltmeter and 50 ohm load to SKTH, and the counter to signal generator high level output so as to read the output frequency.

3.3 Tuning Procedure

3.3.1 Low-pass Filters

Set the signal generator at the required frequency and connect to SKA. Slowly screw-in the inductor core until the response on the millivoltmeter just starts to drop (= 0.2dB). This may follow a slight increase in reading.

3.3.2 High-pass Filters (Not module 1A)

Set the signal generator at the required frequency. Slowly unscrew the inductor core until the response on the millivoltmeter just starts to drop. Sometimes there may be a drop followed by a slight increase in reading and then another drop. The second drop in meter reading is the setting required.

3.3.3 Check the overall response of the filter firstly on the Polyskop and then by varying the signal generator frequency and noting the millivoltmeter response.

3.4 Tuning (Not Module 1A)

3.4.1 Set the signal generator output to 300mV. Select the appropriate filter, set the frequency (± 10kHz tolerance) and adjust the appropriate inductors as indicated in Table 2.

TABLE 2 : INDUCTOR FREQUENCIES

Selected Filter	Frequency Setting (MHz)	Inductors Adjust
21-30	32	L72-74
21-30	30.1	L65-67
21-30	20.9	L68-70

continued ...

TABLE 2 continued ...

Selected Filter	Frequency Setting (MHz)	Inductors Adjust
14-21	21.1 13.9	L57-59 L60-62
9-14	14.1 8.9	L49-51 L52-54
6-9	9.1 5.9	L41-43 L44-46
4-6	6.1 3.9	L33-35 L36-38
3-4	4.1 2.9	L25-27 L28-30
2-3	3.1 1.9	L17-19 L20-22
1.4-2	2.1 1.3	L8-10 L11-14
0-1.4	1.5	L1-6

3.4.2 Connect the module to the Polyskop and examine each filter in turn. Retune any cores as necessary to obtain the smoothest possible shape without affecting the position of the cut-off frequencies.

3.5 Response

Select each filter in turn and by varying the signal generator frequency and noting the response on the millivoltmeter, record the maximum insertion loss within the indicated pass-band of the filter. Record the frequency at the 40dB insertion loss points (high and low frequencies), e.g. for the 21-30MHz filter, the pass-band is 21MHz to 30MHz, tolerance ± 10kHz. The pass-band insertion loss should not be more than 3dB.

TABLE 3 : FILTER INSERTION LOSSES

Selected Filter	40dB I/L points (MHz)
0- 1.4	less than 2.0
1.4- 2	greater than 1, less than 2.8
2 - 3	greater than 1.5, less than 4
3 - 4	greater than 2, less than 6

continued ...

TABLE 3 continued ...

Selected Filter	40dB I/L points (MHz)
4 - 6	greater than 3, less than 8
6 - 9	greater than 4.5, less than 12
9 -14	greater than 7, less than 18
14 -21	greater than 10.5, less than 28
21 -30	greater than 15, less than 38

3.6 Inspection

The module should be inspected to ensure that no damage has been caused during testing and that no inductor cores are loose.

4. COMPONENT LISTS

Module 1 Main Assembly (630/1/32981/001)
Module 1A Main Assembly (630/1/32981/002)

Note: Items marked * are used in Modules 1 and 1A, the remainder in Module 1 only.

Panel Electronic Circuit (419/1/18801)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
	Panel Printed Circuit	Plessey	419/2/18002
C108	Capacitor 10pF ± 1pF 30V	Suflex HSC 30	437/4/30011/081
C122*	Capacitor 12pF ± 1pF 30V	Suflex HSC 30	437/4/30011/082
C93	Capacitor 22pF ± 1pF 30V	Suflex HSC 30	437/4/30011/083
C79	Capacitor 39pF ± 1pF 30V	Suflex HSC 30	437/4/30011/084
C126*	Capacitor 45pF ± 1pF 30V	Suflex HSC 30	437/4/30011/085
C65	Capacitor 56pF ± 1pF 30V	Suflex HSC 30	437/4/30011/086
112,127*	Capacitor 68pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/009
C124*	Capacitor 70pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/037
C51	Capacitor 82pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/024
C97,110, 113,116	Capacitor 100pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/011
C121,125*	Capacitor 100pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/088
C107,118	Capacitor 120pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/013
C38,83,95, 98,114	Capacitor 130pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/089
C123	Capacitor 145pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/090
C101,111	Capacitor 150pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/025
C103,109	Capacitor 160pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/091
C24,92, 117,120	Capacitor 180pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/015
C81,84,96, 99	Capacitor 200pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/092
C69,87	Capacitor 220pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/017
C94,105, 119	Capacitor 240pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/093
C10,78,89, 102	Capacitor 270pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/026
C55,67,70, 82,85	Capacitor 300pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/094
C73	Capacitor 330pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/027
C3,80,104	Capacitor 360pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/095
C75,91	Capacitor 390pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/096
C53,64,88	Capacitor 430pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/097
C42,56,68, 71	Capacitor 470pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/019
C59	Capacitor 510pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/098
C66,90	Capacitor 560pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/028
C28,50,61, 74,77	Capacitor 620pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/099
C40,43,46, 54,57	Capacitor 680pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/029
C26,48,52	Capacitor 820pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/030
C14,29,37, 44,60,63, 76,115	Capacitor 910pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/100

Panel Electronic Circuit (Cont'd)

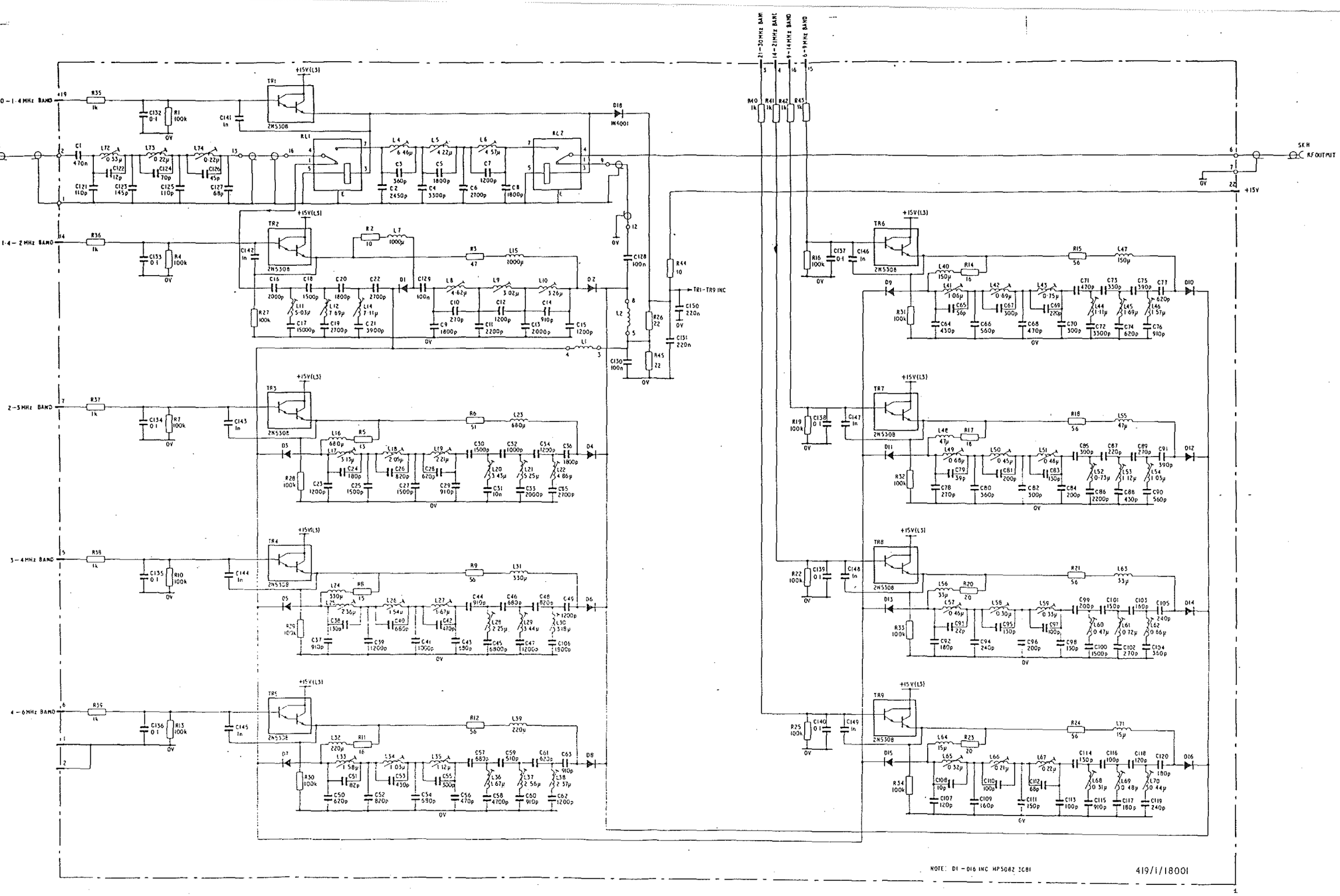
Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
C32,41	Capacitor 1000pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/021
C7,12,15, 23,34,39, 47,49,62	Capacitor 1200pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/034
C18,25,27, 30,100	Capacitor 1500pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/001
C5,8,9,20, 36,106	Capacitor 1800pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/101
C13,16,33	Capacitor 2000pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/102
C11,86	Capacitor 2200pF ± 2.5% 30V	Suflex HSC 30	437/4/30043/002
C2	Capacitor 2450pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/103
C6,19,22, 35	Capacitor 2700pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/104
C4,72	Capacitor 3300pF ± 2.5% 30V	Suflex HSC 30	437/4/30043/004
C21	Capacitor 3900pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/080
C58	Capacitor 4700pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/105
C45	Capacitor 6800pF ± 2.5% 30V	Suflex HSC 30	437/4/30043/006
C31	Capacitor 10,000pF ± 2.5% 30V	Suflex HSC 30	437/4/30043/007
C17	Capacitor 15.000pF ± 2.5%	Suflex HSC 30	437/4/30043/106
C141-149	Capacitor 1nF +80% -20%	Erie 8101A-100	400/4/19440/007
C128,129*, 130,132-140	Capacitor 0.1uF ± 5% 100V	Siemens B32560	435/4/90317/014
C1(Mod.1)	Capacitor, 470nF		425/4/90317/019
C1(Mod.1A)	Capacitor, 220nF	As C131 and C150	-
C131,150	Capacitor 0.22uF + 5%	Siemens B32560 100V	435/4/90317/017
L64,71	Inductor 15uH ± 10%	Sigma SC30	406/4/31753/026
L56,63	Inductor 33uH ± 10%	Sigma SC30	406/4/31753/030
L48,55	Inductor 47uH ± 10%	Sigma SC30	406/4/31753/032
L40,47	Inductor 150uH ± 10%	Sigma SC30	406/4/31753/038
L32,39	Inductor 220uH ± 10%	Sigma SC30	406/4/31753/040
L24,31	Inductor 330uH ± 10%	Sigma SC30	406/4/31753/042
L16,23	Inductor 680uH ± 10%	Sigma	406/4/31754/018
L7,15	Inductor 1000uH ± 10%	Sigma SC30	406/4/31753/048
L42	Inductor 0.69uH ±	Plessey	406/9/29660/001
L43	Inductor 0.75uH	Plessey	406/9/29660/002
L34	Inductor 1.03uH	Plessey	406/9/29661/001
L41	Inductor 1.06uH	Plessey	406/9/29660/003
L44	Inductor 1.11uH	Plessey	406/9/29660/004
L35	Inductor 1.12uH	Plessey	406/9/29660/005
L26	Inductor 1.54uH	Plessey	406/9/29661/002
L33,46	Inductor 1.58uH	Plessey	406/9/29660/006
L27,36	Inductor 1.67uH	Plessey	406/9/29660/007
L45	Inductor 1.69uH	Plessey	406/9/29660/008
L18	Inductor 2.05uH	Plessey	406/9/29661/003

Panel Electronic Circuit (Cont'd)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
L19	Inductor 2.21uH	Plessey	406/9/29661/004
L28	Inductor 2.25uH	Plessey	406/9/29661/005
L25	Inductor 2.36uH	Plessey	406/9/29661/006
L38	Inductor 2.37uH	Plessey	406/9/29660/009
L37	Inductor 2.56uH	Plessey	406/9/29660/010
L9	Inductor 3.02uH	Plessey	406/9/29661/007
L17	Inductor 3.13uH	Plessey	406/9/29660/011
L30	Inductor 3.18uH	Plessey	406/9/29660/012
L10	Inductor 3.26uH	Plessey	406/9/29661/008
L20	Inductor 3.43uH	Plessey	406/9/29661/009
L29	Inductor 3.44uH	Plessey	406/9/29661/010
L5	Inductor 4.22uH	Plessey	406/9/29661/011
L6	Inductor 4.57uH	Plessey	406/9/29661/012
L8	Inductor 4.62uH	Plessey	406/9/29661/013
L22	Inductor 4.86uH	Plessey	406/9/29660/013
L11	Inductor 5.03uH	Plessey	406/9/29661/014
L21	Inductor 5.25uH	Plessey	406/9/29660/014
L4	Inductor 6.46uH	Plessey	406/9/29660/015
L14	Inductor 7.11uH	Plessey	406/9/29661/015
L12	Inductor 7.69uH	Plessey	406/9/29660/016
L1,2	Inductor 1.4mH ± 20%	Plessey	406/9/31750/010
L66,67,73, 74	Inductor .198-.242uH	Cambion 558-7107-05	406/4/31750/005
L58,59,65, 67,72*	Inductor .297-.363uH	Cambion 558-7107-07	406/4/31750/007
L50,51,57, 60,69,70	Inductor .423-.517uH	Cambion 558-7107-09	406/4/31750/009
L49,52,61, 62	Inductor .612-748uH	Cambion 558-7107-11	406/4/31750/011
L54	Inductor .900-1.10uH	Cambion 558-7107-13	406/4/31750/013
L53	Inductor 1.08-1.32uH	Cambion 558-7107-14	406/4/31750/014
R35-43	Resistor 1k ± 2% 0.25W	Electrosil TR4	403/4/05523/100
R2,44	Resistor 10R ± 2% 0.5W	Electrosil TR4	403/4/05321/100
R5	Resistor 13R ± 1% 0.5W	Electrosil TR4	403/4/05311/130
R8	Resistor 15R ± 2% 0.5W	Electrosil TR4	403/4/05321/150
R11,14	Resistor 16R ± 1% 0.5W	Electrosil TR4	403/4/05311/160
R17	Resistor 18R ± 2% 0.5W	Electrosil TR4	403/4/05321/180
R20,23	Resistor 20R ± 1% 0.5W	Electrosil TR4	403/4/05311/200
R6	Resistor 51R ± 1% 0.5W	Electrosil TR4	403/4/05311/510
R3	Resistor 47R ± 2% 0.5W	Electrosil TR4	403/4/05321/470
R9,12,15, 18,21,24	Resistor 56R ± 2% 0.5W	Electrosil TR4	403/4/05321/560
R26,45	Resistor 22R ± 5% 2.5W	Electrosil TR4	403/4/04521/220
R1,4,7,10, 13,16,19, 22,25, 27-34	Resistor 100k ± 2% 0.25N	Electrosil TR4	403/4/05525/100
D1-16	Diode	Hewlett Packard HP5082-3081	415/9/05565
TR1-9	Transistor	Texas 2N5308	417/4/01877
RL1,2	Relay	Thorn RS-12V	507/4/98291/003

Connector Assembly (702/1/20093/004)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
SKA,H	Socket, RF (Fixed)	Belling Lee L1465/K/BS	508/4/22059
-	Cable RF	Suhner RG174/U 190 mm	998/4/70537/001



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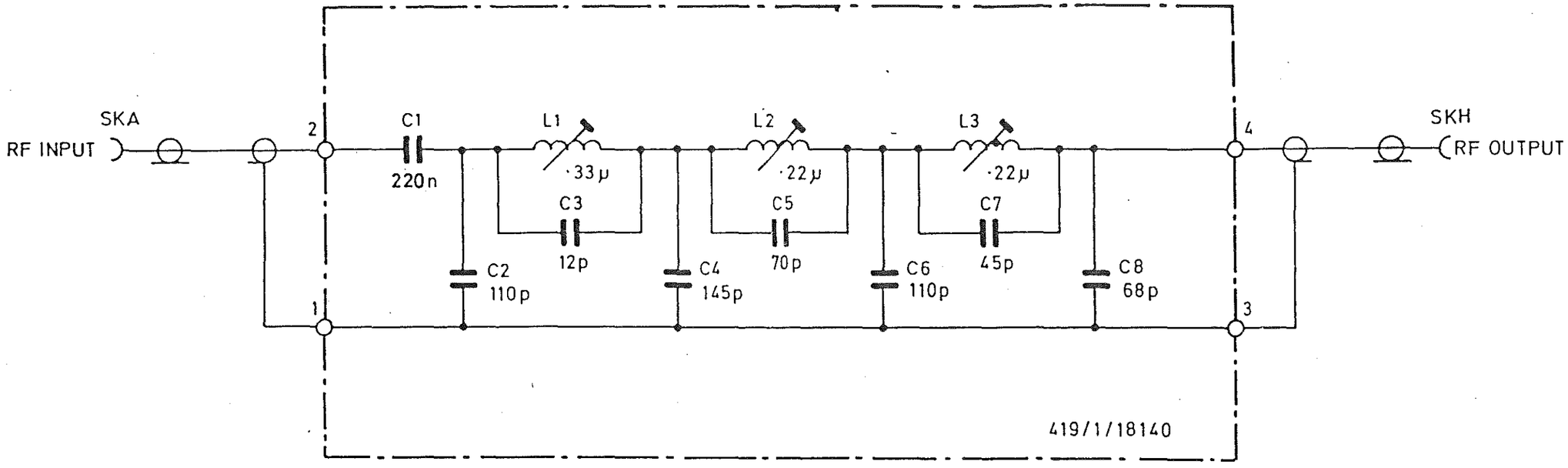
MODULE 1 : RF FILTERS CIRCUIT DIAGRAM

FIG 1



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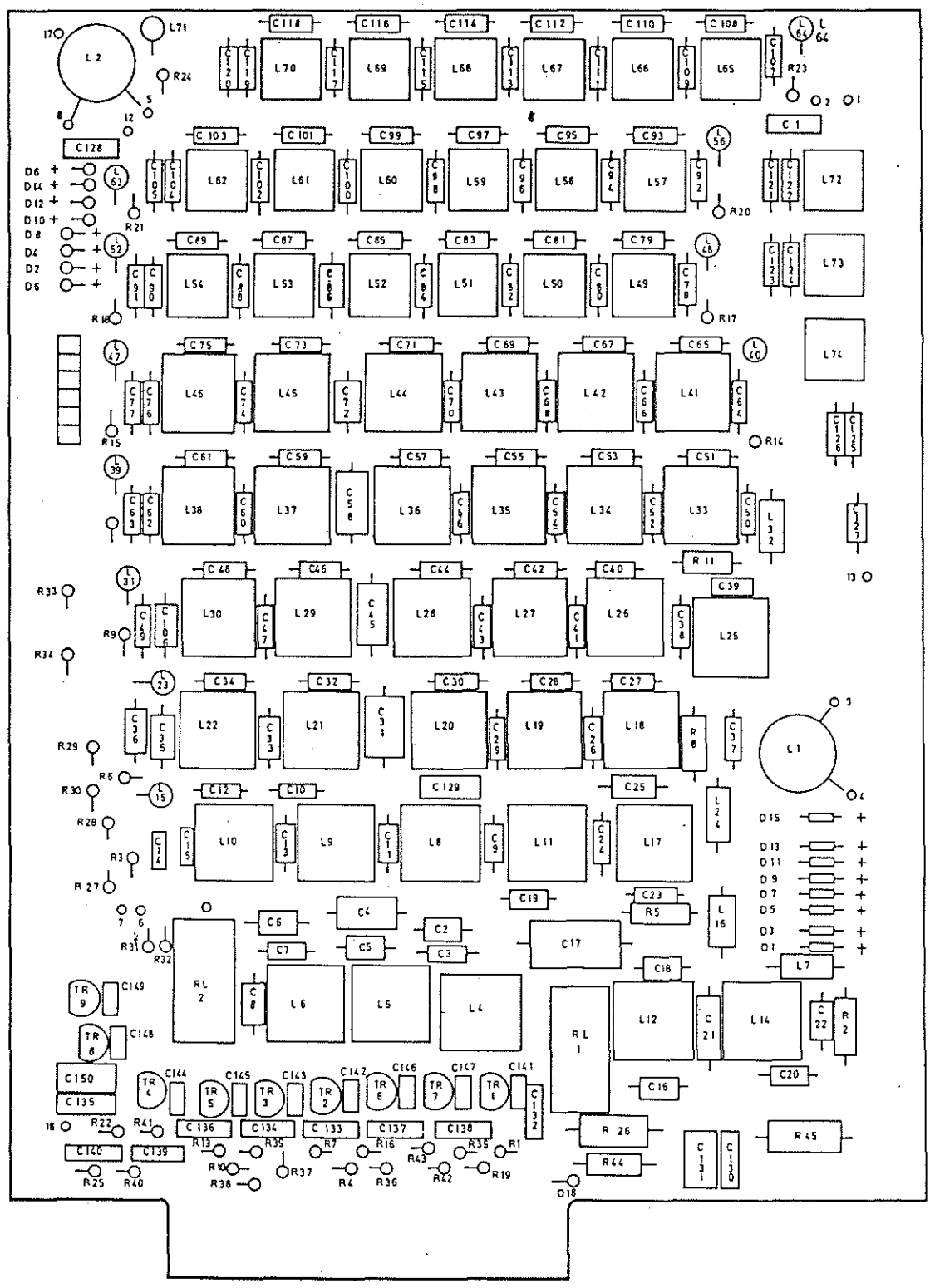
MODULE IA CIRCUIT DIAGRAM

FIG 2



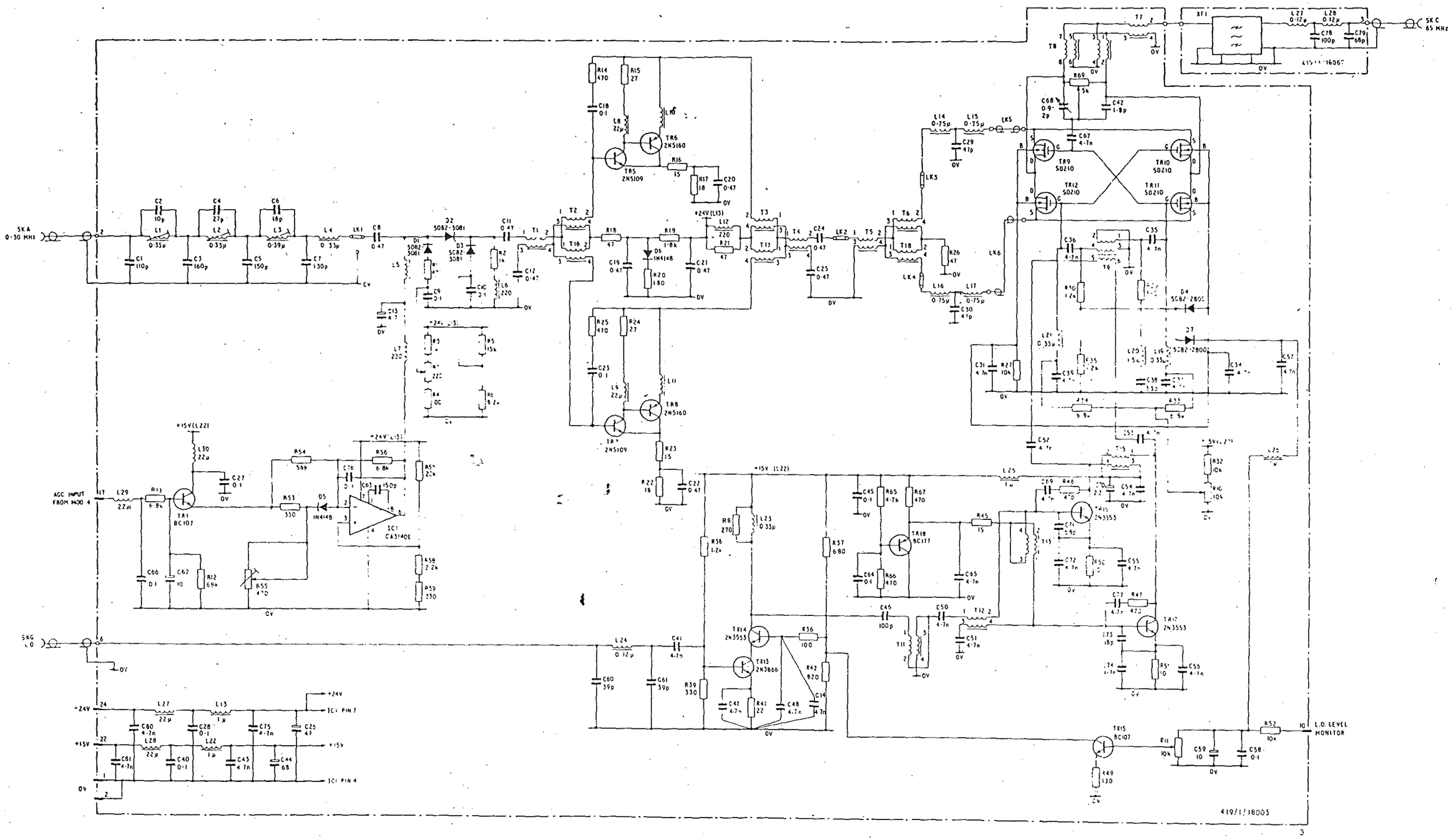
MODULE 1 PANEL COMPONENT LAYOUT FIG 3

CHAPTER 2

MODULE 2 - RF AMPLIFIER/1ST MIXER

CONTENTS

ILLUSTRATIONS



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MODULE 2 : RF AMPLIFIER AND IST MIXER CIRCUIT DIAGRAM

FIG 1

MODULE 2 - RF AMPLIFIER/1ST MIXER

1. FUNCTIONAL DESCRIPTION

1.1 Module 2 is used in all PR2250 series receivers. It contains the r.f. amplifier and first mixer stages. A functional block diagram can be seen in Figure (a).

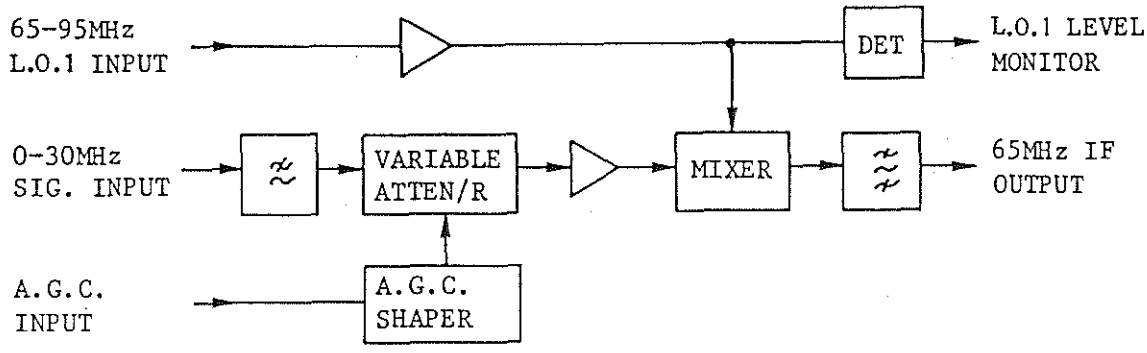


FIG (a) MODULE 2 FUNCTIONAL BLOCK DIAGRAM

1.2 The filtered r.f. output from Module 1 is applied to an a.g.c.-controlled attenuator via a 0-32MHz low-pass filter. A d.c. control input is applied to the shaper circuit, which reduces control sensitivity with increase of signal strength. The amplitude-controlled r.f. signal is applied via a broad-band amplifier to a mixer. The local oscillator input frequency is controlled by the receiver tuning at 65MHz above the displayed frequency. The difference frequency is extracted by a band-pass filter, forming the 65MHz IF output. Sideband reversal occurs at this point but is only significant in respect of SSB signals.

2. CIRCUIT DESCRIPTION

2.1 Input Filter and AGC Attenuator

The filtered r.f. output from Module 1 is applied via SKA to a low-pass filter formed by L1, L2, L3, L4, and associated capacitors; 3dB attenuation is produced at 32MHz. The output from the filter is connected via d.c. blocker C8 to a PIN-diode controlled variable pi attenuator formed by the components between d.c. blocker capacitors C8 and C11. Characteristic Impedance is 50 ohms; attenuation range is from 0dB to -35dB, dependent upon the d.c. level applied via L7 and L5. A +24V level at L7 produces 0dB attenuation; attenuation increases to about 14dB at +2V, and increases to a maximum for a d.c. level of aproximately +0.5V.

2.2 AGC Shaper

Control of the pi attenuator is exercised by the a.g.c. input to edge-pin 17, via the a.g.c. shaper formed by TR1, IC1 and associated components. Emitter-follower TR1 provides the d.c. input to shaper operational amplifier IC1. For low input levels, IC1 gain is set at approximately 6.8 by R54, R53 and R56, as D5 is forward-biased due to the d.c. level set by R55. When the voltage at TR1 emitter passes a level set by R55, D5 reverse-biases, and IC1 gain is set by R54 and R56 at about 0.2.IC1 output level is fed to the pi attenuator via filter L7, C13, L5.

2.3 R.F. Amplifier

2.3.1 The a.g.c.-controlled r.f. signal is applied via transmission-line (Ruthroff) transformers T1-T2-T16 to a complementary pair push-pull r.f. amplifier formed by TR5, TR6, TR7, and TR8. Transmission-line transformers provide very great bandwidth and are of small size. The arrangement of T1, T2, and T16 produces precise broad-band phase splitting between the inputs to TR5 and TR7 bases: this splitting precision is largely independent of load values.

2.3.2 The outputs from complementary pairs TR5-TR6 and TR6-TR7 are applied to a further set of Ruthroff transformers, T3, T4 and T17; the output signal is fed via d.c. blocking capacitor C24 to one input of the mixer circuit formed by TR9, TR10, TR11, TR12, and associated components. The other mixer (1st local oscillator) input is provided by a local oscillator signal amplifier formed by TR13, TR14, TR16, TR17, and associated components.

2.4 Local Oscillator Amplifier

2.4.1 The 1st Local Oscillator input (65 to 95MHz) is applied via capacitor C41 to common-emitter amplifier TR13. The amplified signal is fed via impedance-matching transformer T11 and d.c. blocker capacitors C46 and C50 to phase-splitter transformer T12 for application to TR16 and TR17 bases. The arrangement of T12 and T13 produces a fine degree of balance between the antiphase signals applied to TR16 and TR17 bases. Bias to TR16 and TR17 is generated by voltage source TR18, and fed via R45 and T13.

2.4.2 TR16 and TR17 form a push-pull amplifier having transformer T15 as collector load to aid balance. The signal output is fed via d.c. blocker capacitors C52 and C53 to the input winding of T9, forming the local oscillator input to the mixer.

2.4.3 A.G.C. is applied to the local oscillator amplifier via TR14 base circuit. A positive-going d.c. level proportional to local oscillator input signal amplitude is produced by D7, and amplified via amplifier stage TR15 to controller stage TR14. The collector current of TR14 is proportional to the d.c. level applied from the mixer to TR15 base; this varies the a.c. impedance of TR13 collector circuit, so controlling its gain. Operating levels are set by R11.

2.5 Mixer

2.5.1 The mixer circuit formed by TR9, TR10, TR11 and TR12, is essentially a ring modulator formed by four field effect transistors, with inputs and outputs fed via Ruthroff balancing transformers. The basic circuit can be seen in Figure (b).

2.5.2 The gates of the four MOSFETS are positively biased by the voltage set by R10: R33, L19, and C37 decouple the lines to TR9 and TR11 gates, while R34, L21, and C39 decouple the lines to TR10 and TR12 gates. Substrate bias for all four transistors is set at approximately -4.5V; this voltage is produced by diode D4 rectifying a proportion of the local oscillator signal across pins 3 and 4 of T9 (as reduced by potentiometer chain R30 and R35) and applying it to the parallel RC circuit R27, C31, C34 connected between the substrates and OV.

2.5.3 The r.f. signal input to the ring modulator mixer circuit is applied via balance transformers T5, T6, and T18, the outputs from which are two

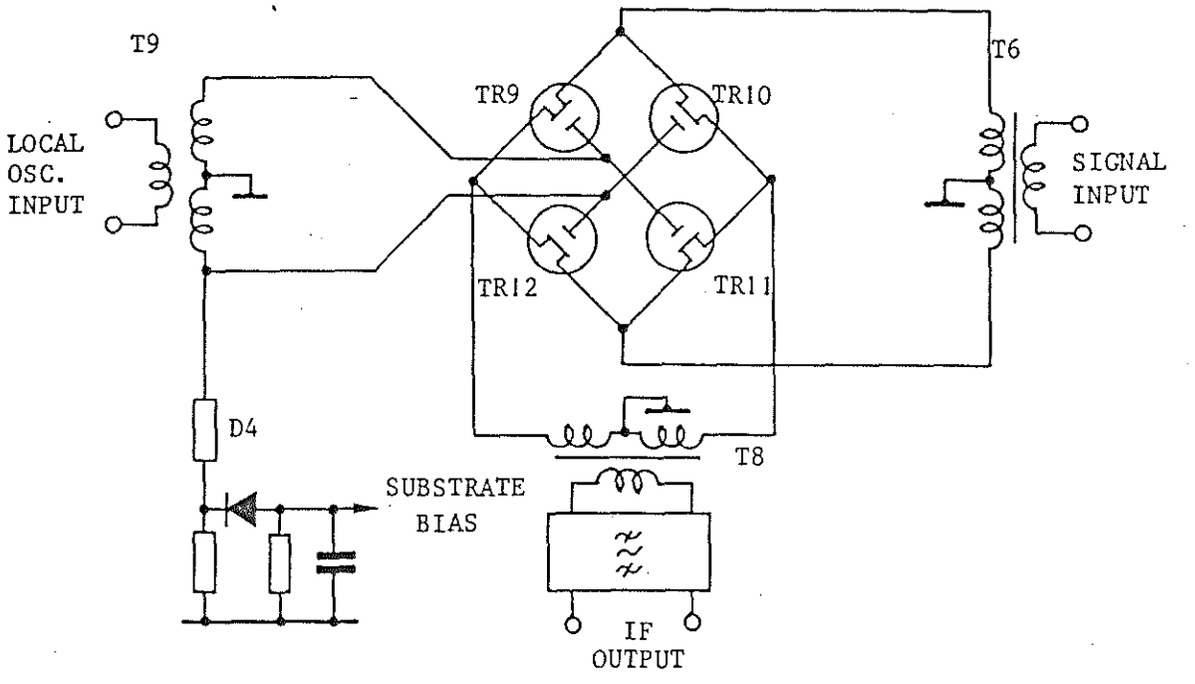


FIG (b) BASIC MIXER CIRCUIT

balanced antiphase signals on pins 2 and 4. These are applied to TR9-TR10 junction, and to TR11-TR12 junction. The local oscillator input is applied via T9 to produce two balanced antiphase signals on pins 1 and 4. These are applied via d.c. blocker capacitors C35 and C36 to TR9-TR11 gates and to TR10-TR12 gates.

2.5.4 The output of the circuit is taken from TR9-TR12 junction and from TR10-TR11 junction. These two points produce antiphase signals which are applied via T8 and T7 to encapsulated crystal band-pass filter XF1. The filter extracts the 65MHz IF frequency from the output of the mixer. The 65MHz band-pass filter has a rising pass-band characteristic at approximately 100MHz and so a low-pass filter, consisting of L27, L28 and associated capacitors, is inserted in series to overcome this. The output of the low-pass filter is applied to SKC as the 1st IF output signal.

2.5.5 A proportion of the local oscillator signal across pins 3 and 4 of T9 appears across R35, and is rectified by D7: the resultant d.c. level appears on edge-pin 10 as a monitor output, and is also applied to TR15 base as AGC control input.

2.5.6 C68/R69 are tuned to minimise LO1 breakthrough at f_{LO1} = 65.0MHz.

3. TEST DATA

3.1 General

The procedure outlined in the following paragraphs forms a complete test procedure and need not be used to locate individual faults.

3.2 Test Equipment

The following items of test equipment are required:

Signal Generator, 95MHz, 10mV to 1V O/P at 13MHz. (1)

Signal Generator, .78MHz, for LO1 input (2).

R.F. Millivoltmeter, 1.4MHz 1k ohm input impedance.

Resistive matching pad, 50-100 ohms, to match signal generator to a 100 ohm system.

100 ohm ± 2% Resistor (TR4).

AVO meter.

Valve Voltmeter e.g. Marconi TF2604.

3.3 Power Supplies

Separate +15V, 450mA amd +24V, 200mA power supplies.

A variable, 0-12V, 5mA DC power supply for the AGC input (a suitable resistor and potentiometer across the +15V supply will suffice).

3.4 Alignment and Functional Tests

3.4.1 On the module set R7, R11, R55 and R69 at the mid-position. Use the variable 0-12V DC supply to set the AGC INPUT on edge-pin 17 at 0V. Note that R10 setting is a factory adjustment and must not be disturbed.

3.4.2 32MHz LPF

Unsolder Link 1 (LK1) on the printed circuit panel. Connect the signal generator to SKTA, the millivoltmeter across LK1 (connected to L4) and earth. Set the signal generator to 30.1MHz at an output level of 300mV rms and unscrew the cores of L1, L2, L3 and L4. Screw in the cores of L1 to L4 in turn until the meter reading just starts to drop in each case. Vary the frequencies on the signal generator from 30MHz to 0MHz and ensure that the filter output does not give greater than 2dB loss for 0 to 30MHz, and not less than 30dB loss at 40MHz. (Reference level for filter loss is 300mV assuming that the filter has no loss). Lock the cores and resolder LK1.

3.4.3 32MHz LPF Mixer Inputs

Unsolder links, LK3 to 6, and connect the 100 ohm resistor across LK5 (connected to L15) and earth. Connect the millivoltmeter, via high impedance probe across the 100 ohm resistor. Set the signal generator to 32MHz at 300mV output and connect via Matching pad to LK3 (input to L14). Unscrew the cores of L14 and L15 to give a minimum inductance and then slowly screw in the cores, in turn, until the reading on the millivoltmeter just starts to drop in each case. Vary the signal generator frequency and confirm the response of the filter - 0 to 30MHz, not more than 1dB loss, 60MHz, not less than 12dB loss. Lock the cores and repeat the tests of L16, L17 and C30 with links, LK4 and 6. When the tests have been completed lock the cores and resolder LKS3 to 6.

3.4.4 LO Drive Amplifier Mixer Balance

Connect the power supplies, +15V 450mA to edge-pin 22, +24V 200mA to edge-pin 24 and 0V to edge-pin 1. Set the signal generator to 78.000MHz at 650mV rms and connect to SKT G. Connect the millivoltmeter and 50 ohm load to SKT C and adjust signal generator frequency to give maximum read-

ing on the millivoltmeter. Monitor pin 4 of T9 with the valve voltmeter. Adjust, if necessary, R11 on the module to give a 15V a.c. reading. Adjust C68 and R69 alternately until millivoltmeter reads not less the 5mV.

3.4.5 RF AGC Delay Setting

Set the Avometer on the 10V d.c. range and connect between the wiper of R7 and earth. Adjust R7 to give a reading on the Avometer of 2.15V. Set the 'AGC INPUT' voltage at 4.0V, by means of the 12V variable supply. Set the Avometer on the 2.5V d.c. range and connect across the wiper of R55 and earth and adjust R55 to give a reading of 1.7V. Reset the 'AGC INPUT' to 0V.

3.4.6 Gain

Set the signal generator (2) to 78MHz, 10 $\pm$ 2dBm and connect to SKT G. Set the signal generator (1) to 13MHz 10mV rms, and connect to SKT A. Connect the millivoltmeter and 50 ohm load across SKT C. Adjust the signal generator (1), if necessary, for maximum reading on the millivoltmeter; not less than 10.0mV (i.e. +3dB reference 10mV). Increase signal generator (1) output by 20dB and adjust the AGC volts to bring the output back to previous reading. Measure the AGC volts which should be 5.5 - 7 volts. Set the 'AGC INPUT' to maximum (12V), and measure the drop in the millivoltmeter reading from the previous reading. The difference in meter reading should not be less than 15dB (i.e. at least 35dB AGC range). Reset the AGC to 0V.

3.4.7 Compression Point

Set the signal generator output for 1V rms at 13MHz: note the millivoltmeter reading obtained across a 50 ohm load connected to SKC. Decrease the signal generator output by 10dB and note the drop in the millivoltmeter reading. This reading must not be less than 8dB, i.e. 2dB compression at 1V.

3.4.8 Inspect the module to ensure that no damage has been caused during testing.

4. COMPONENT LISTS.

Main Assembly (630/1/32982)
Panel Electronic Circuit (419/1/18803)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Panel Printed Circuit	Plessey	419/2/18004
-	Socket Semi Conductor	Texas C930802	508/4/22096/001
C38	Capacitor 3.3pF ± 0.25pF 100V	Mullard 632-09338	400/4/20647/004
C2	Capacitor 10pF ± 1pF 30V	Suflex HSC 30	437/4/30011/081
C6	Capacitor 18pF ± 1pF 30V	Suflex HSC 30	437/4/30011/111
C4	Capacitor 27pF ± 1pF 30V	Suflex HSC 30	437/4/30011/112
C29,30	Capacitor 47pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/113
C5,63	Capacitor 100pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/025
C1	Capacitor 110pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/088
C7	Capacitor 130pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/089
C3	Capacitor 160pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/091
C69	Capacitor 1.8pF ± 0.25% 100V	Mullard 632-09138	400/4/20647/001
C60,61	Capacitor 39pF ± 2% 100V	Mullard 632-34399	400/4/20674/017
C46	Capacitor 150pF ± 5% 100V	Erie 8121M-100-C09	400/4/20672/005
C31,34-37, 39,41,43, 47,48,50-56,65,67, 72,74,75, 80,81,57, 69,77,14	Capacitor 4.7nF ± 10% 100V	Erie 8111M-X7R	400/4/21280/001
C9,10,18,23, 27,28,40, 45,58,64, 66,76	Capacitor 0.1uF ± 5% 100V	Siemens B32560	435/4/90317/014
C6,11,12,19, 20,21,22, 24,25	Capacitor 0.47uF ± 5% 100V	Siemens B32560	435/4/90317/019
C13	Capacitor 4.7uF ± 20% 35V	ITT TAG	402/4/50757/005
C59,62	Capacitor 10uF ± 20% 35V	ITT TAG	402/4/50757/006
C68	Capacitor Variable 7.3pF min. 375V	Oxley SDMT9/7.3 Ref 2	401/4/14555/005
C70	Capacitor 2.2uF ± 20% 35V	ITT TAG 2.2/35	402/4/57057/004
C71,73	Capacitor 68pF ± 2% 100V	Mullard 632-34689	400/4/20674/020
C26	Capacitor 47uF ± 20% 35V	ITT Type TAG	402/4/55748/017
C44	Capacitor 68uF ± 20% 25V	ITT Type TAG	402/4/55747/018
L19,21,23	Inductor 0.33uH ± 10%	Sigma SC10	406/4/31749/003
L22,25,26	Inductor 1uH ± 10%	Sigma SC10	406/4/31749/004
L20	Inductor 1.5uH ± 10%	Sigma SC10	406/4/31749/004
L8,9,27,28, 29,30	Inductor 22uH ± 10%	Sigma SC10	406/4/31749/002
L13	Inductor 100uH ± 10%	Sigma SC10	406/4/31741/002
L6,7,12	Inductor 220uH ± 10%	Sigma SC10	406/4/31741/006
L5	Inductor 1.4mH ± 20%	Plessey	406/9/29617/010
L10,11	Inductor	Plessey	406/1/29691
L14,15,16,17	Inductor 0.75uH	Plessey	406/1/08324/004
L24	Inductor 0.12uH ± 10%	Plessey	406/9/08470/001
L1,2,4	Inductor 0.297-0.363uH	Cambion 558-7107-07	406/4/31750/007
L3	Inductor 0.351-0.429uH	Cambion 558-7107-08	406/4/31750/007

Panel Electronic Circuit (Cont'd)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
IC1	Integrated Circuit	RCA CA 3140E	445/4/03072/004
R15,24	Resistor 27R ± 2%	Electrosil TR4	403/4/05521/270
R50,51	Resistor 10R ± 2%	Electrosil TR4	403/4/05521/100
R16,23,45	Resistor 15R ± 2%	Electrosil TR4	403/4/05521/150
R17,22	Resistor 18R ± 2%	Electrosil TR4	403/4/05521/180
R41	Resistor 22R ± 2%	Electrosil TR4	403/4/05521/220
R18,21,26	Resistor 47R ± 2%	Electrosil TR4	403/4/05521/470
R4,36,49	Resistor 100R ± 2%	Electrosil TR4	403/4/05522/100
R20,39	Resistor 180R ± 2%	Electrosil TR4	403/4/05522/180
R8	Resistor 270R ± 2%	Electrosil TR4	403/4/05522/270
R53,59	Resistor 330R ± 2%	Electrosil TR4	403/4/05522/330
R14,25,42, 46,66,67	Resistor 470R ± 2%	Electrosil TR4	403/4/05522/470
R37	Resistor 680R ± 2%	Electrosil TR4	403/4/05522/680
R42	Resistor 820R ± 2%	Electrosil TR4	403/4/05522/820
R3	Resistor 1k ± 2%	Electrosil TR4	403/4/05523/100
R30,35,38	Resistor 1.2k ± 2%	Electrosil TR4	403/4/05523/120
R19	Resistor 1.8k ± 2%	Electrosil TR4	403/4/05523/180
R58	Resistor 2.2k ± 2%	Electrosil TR4	403/4/05523/220
R65	Resistor 4.7k ± 2%	Electrosil TR4	403/4/05523/470
R33,34,13,56	Resistor 6.8k ± 2%	Electrosil TR4	403/4/05523/680
R6	Resistor 8.2k ± 2%	Electrosil TR4	403/4/05523/820
R27,32,52	Resistor 10k ± 2%	Electrosil TR4	403/4/05524/100
R5	Resistor 15k ± 2%	Electrosil TR4	403/4/05524/150
R57	Resistor 22k ± 2%	Electrosil TR4	403/4/05524/220
R54,52	Resistor 56k ± 2%	Electrosil TR4	403/4/05524/560
R12	Resistor 68k ± 2%	Electrosil TR4	403/4/05524/680
R1	Resistor 47R ± 2%	Electrosil TR5	403/4/05321/470
R29	Resistor 330R ± 2%	Electrosil TR5	403/4/05322/330
R2	Resistor 1k ± 2%	Electrosil TR5	403/4/05323/100
R7	Resistor Variable 220R ± 20%	Allen Bradley Type 90H	404/9/05047/013
R10,11	Resistor Variable 10k ± 20%	Allen Bradley Type 90H	404/9/05047/005
R69	Resistor Variable 5k ± 20%	Law A Spectrol 62-1-1-5K	404/4/08064/006
R55	Resistor Variable 470R ± 20%	Plessey	409/9/05047/002
D5,6	Diode	Texas 1N4148	415/4/05720
D4,7	Diode	Hewlett Packard 5082-2800	415/9/98532
D1,2,3	Diode	Hewlett Packard 5082-3081	415/9/05565
T1-6,16-18	Transformer R.F.	Plessey	406/9/29657/001
T12	Transformer R.F.	Plessey	406/9/29657/001
T11,13	Transformer R.F.	Plessey	406/9/29657/003
T15	Transformer R.F.	Plessey	406/9/29657/015
T7	Transformer R.F.	Plessey	406/9/29657/005
T8	Transformer R.F.	Plessey	406/9/29657/009
T9	Transformer R.F.	Plessey	406/9/29657/013
TR6,8	Transistor	Motorola 2N5160	417/4/01886
TR1,15	Transistor	Mullard BC107	417/4/01777
TR9,10,11,12	Transistor	Signetics SC210	417/4/01887/001
TR18	Transistor	Mullard BC177	417/4/01859

Panel Electronic Circuit (Cont'd)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
TR13	Transistor	Texas 2N3866	417/4/01775
TR5,7	Transistor	Texas 2N5109	417/4/01784
TR16,17,14	Transistor	Motorola 2N3553	417/9/01814
-	Heatsink	Jermyn A1004AX T05	418/4/44462/003

Connector Assembly (702/1/20092/004)

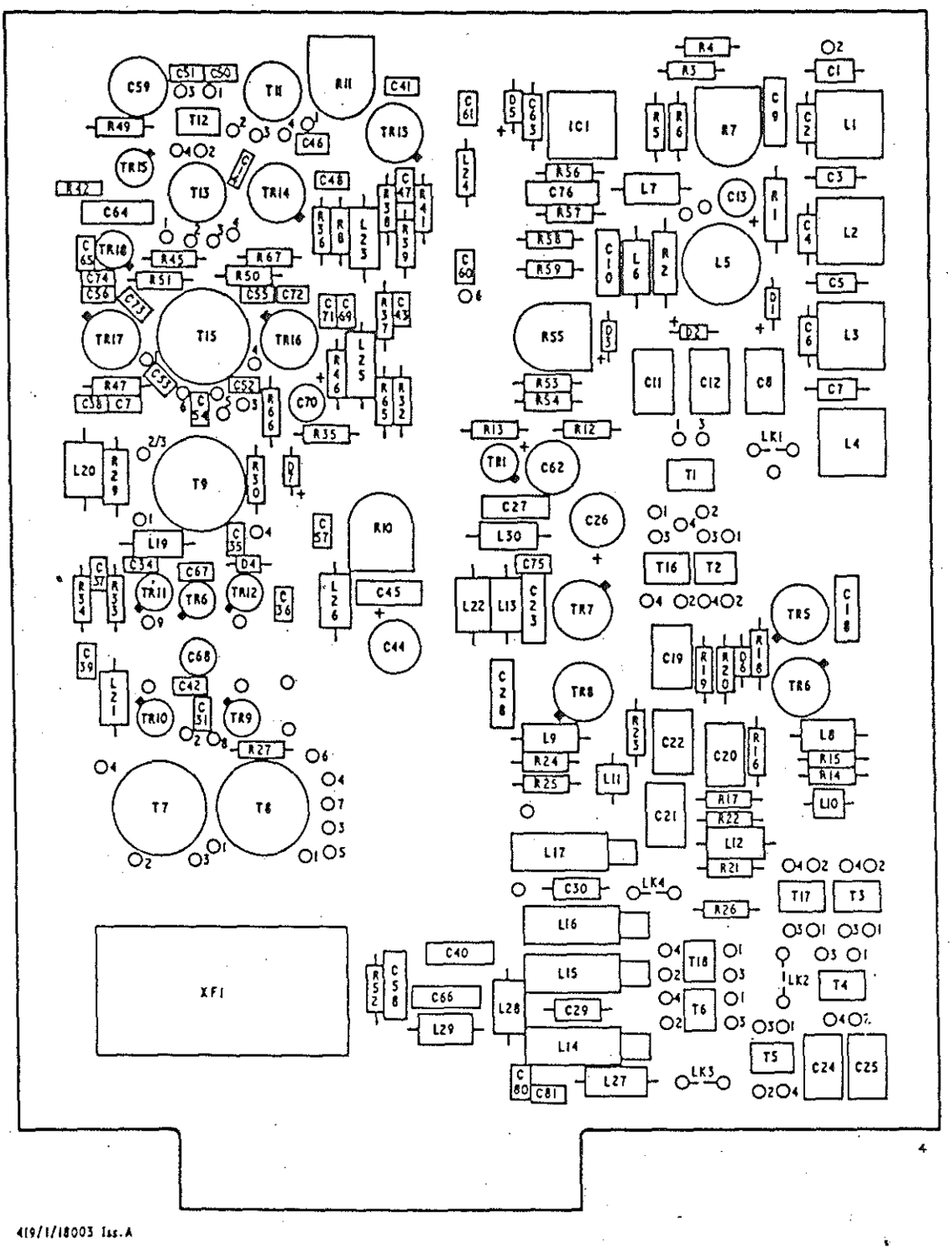
Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
SKA,G	Socket Electrical R.F.	Belling Lee L1465/K/BS	508/4/22059
-	Cable R.F.	Suhner R.G. 174/U 190 mm	998/4/20537/001

Connector Assembly (702/1/20093/007)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
SKC	Socket Electrical R.F.	Belling Lee L1465/K/BS	508/4/22059
-	Cable R.F.	R.G. 174/U/290 mm	998/4/20537/001

Inductor Assembly (406/1/29691)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Core Ferromagnetic Bead	Mullard FX1242	905/9/98052
-	Insulation Sleeving	PTFE 0.75mm x 0.20/0.30	998/4/82852/901
-	Wire Electrical	0.5 dia Unscreened	998/4/82834/009



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MODULE 2 PANEL - COMPONENT LAYOUT

FIG. 2

CHAPTER 3

MODULES 3 and 3A 1ST IF AMPLIFIER, 2ND MIXER AND 2ND IF FILTERS

CONTENTS

ILLUSTRATIONS

MODULES 3 and 3A 1ST IF AMPLIFIER, 2ND MIXER AND 2ND IF FILTERS

1. FUNCTIONAL DESCRIPTION

1.1 Modules 3 and 3A contain the 1st i.f. amplifier, second mixer, and i.f. bandwidth filters. Module 3 contains five filters, while Module 3A contains 3. Module 3 is used in PR2250A, PR2250B, PR2250E, PR2250F, PR2251A, PR2251C, PR2252A, and PR2250C receivers. Module 3A is used in PR2250C, PR2250D, PR2251B, and PR2252B receivers. A functional block diagram covering both modules can be seen in Figure (a).

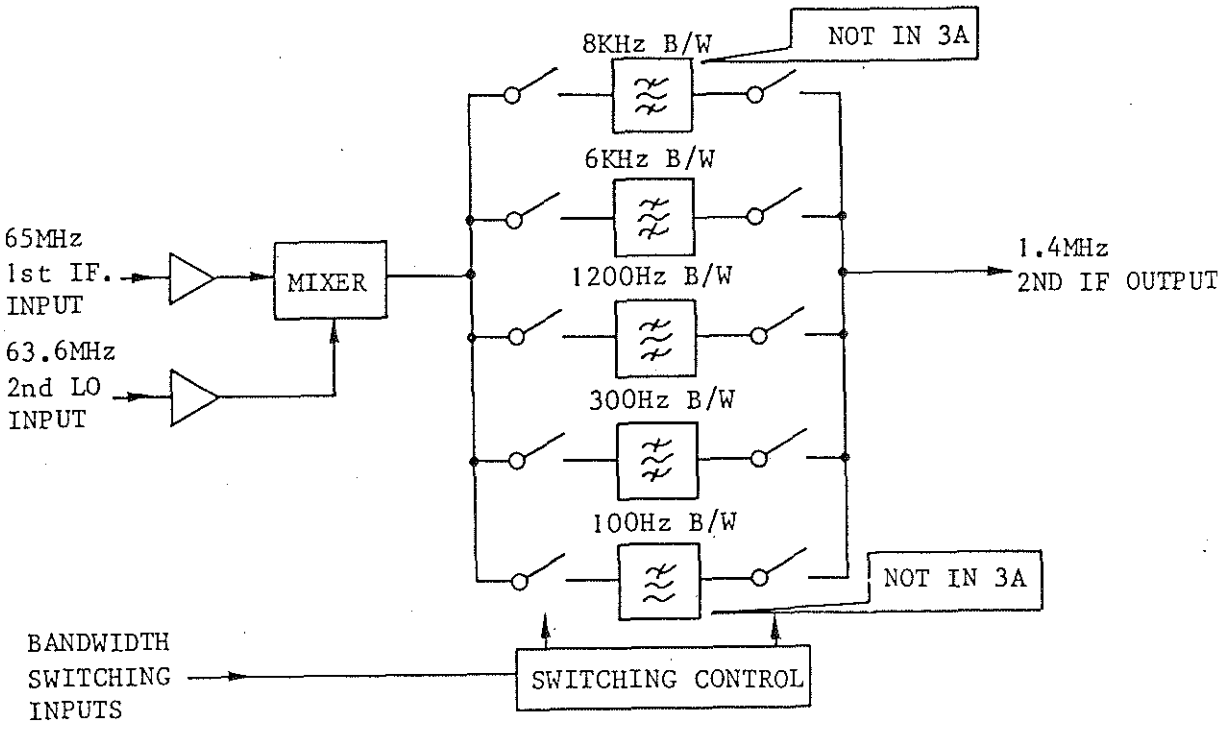


FIG (a) MODULES 3 and 3A FUNCTIONAL BLOCK DIAGRAM

1.2 The 65MHz 1st i.f. signal and the 63.6MHz 2nd L.O. input are amplified and fed to the mixer circuit. The 1.4MHz difference frequency output is selected by one of a bank of five (Module 3) or three (Module 3A) 1.4MHz centre frequency filters. The selection of a particular filter is dependent upon the setting of the front-panel MODE and BANDWIDTH controls.

2. CIRCUIT DESCRIPTION

2.1 1st IF Amplifier

The 1st IF amplifier is formed by TR1 and associated components. The 65MHz output from Module 2 is applied via SKA to a crystal filter feeding TR1 base. Collector-load transformer T1 matches the output to the load presented by mixer TR2-TR3.

2.2 Local Oscillator Amplifier

The 63.6MHz 2nd Local Oscillator output from the Synthesiser (Module 9) is applied via SKH to a series tuned circuit formed by C24 and L9. Transformer T5 matches the input signal to the load of TR4 (L8) and C20 form an output parallel tuned circuit at 63.6MHz.

2.3 2nd Mixer

2.3.1 TR2, TR3, and associated components form the mixer circuit, which is of the basic form shown in Figure (b).

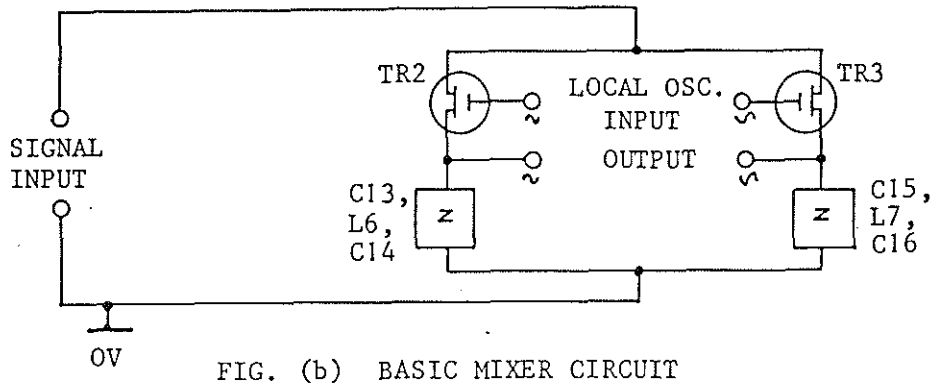


FIG. (b) BASIC MIXER CIRCUIT

TR2 and TR3 are switched on alternately by the local oscillator input, while the drain/source voltage is provided by the signal input. The impedances in series with the transistors form loads across which the output signal is developed. Output transformer T3 is connected so as to minimise spurious output signals, and transformer T4 matches the signal to the load presented by the selected IF filter circuit.

2.3.2 The level of local oscillator drive to the mixer can be monitored on the front-panel meter. The drive to TR2 base is fed via R7 to D13 and associated components, and provides a d.c. current level on edge-pin 10 which is proportional to drive: this d.c. level is fed to the metering circuits.

2.4 2nd IF Filters

2.4.1 The difference frequency component in the output from the mixer is selected by one of a number of crystal filters. Five are fitted in Module 3, and three are fitted in Module 3A: there are no other differences between Module 3 and Module 3A. Bandwidths to 3dB points are:

XF1: 1.4MHz ± 4kHz (Module 3 only)

XF2: 1.4MHz ± 3kHz

XF3: 1.4MHz ± 600Hz

XF4: 1.4MHz ± 150Hz

XF5: 1.4MHz ± 50Hz (Module 3 only)

The filters are separate encapsulated units, wired to numbered terminal pins on the printed-circuit panel.

2.4.2 The inputs of all filters are paralleled via PIN diodes D2, D4, D6, D8, and D10: the outputs are paralleled via PIN diodes D3, D5, D7, D9, and D11. Each pair of diodes is rendered conducting or non-conducting by the logic level applied to the base of the associated switching transistor; for example, D2 and D3 are controlled by the level applied to TR5 base.

2.4.3 At any time, one of switching transistors TR5 - TR9 has a +12V logic '1' level applied to its base, while the remainder are connected to (nominal) 0V logic '0' input levels. The emitter of one switching transistor is therefore at +11.5V, while the bases of the remainder are at (nominal) 0V. The two PIN diodes controlled by the conducting transistor are therefore forward biased, so connecting the associated filter between the mixer output and SKB. The +11.5V emitter level of the one conducting transistor is fed via the two associated conducting PIN diodes to R19 and R16, the junction of which is connected to 0V by zener diode D12. A +6.2V level is therefore always available to reverse-bias the remaining eight PIN diodes.

2.4.4 One control input line is provided for each one of five of the six switching transistors. The sixth, TR8, is controlled via an OR gate from any one of four logic input signals.

3. TEST DATA

3.1 General

The procedure outlined in the following paragraphs forms a complete test procedure and need not be used to locate individual faults.

3.2 Test Equipment

The following items of test equipment are required:

Signal Generator: 65MHz output, 1mV from 50 ohms, and a high level (100mV rms) output.

Signal Generator, 65MHz output level 10 $\pm$ 2dBm for LO2 input source.

Counter (up to 65MHz).

Avometer.

Millivoltmeter, 1.4MHz, 1k ohm input impedance.

3.3 Power Supplies

Separate +15V, 50mA and +24V, 100mA power supplies are required.

3.4 Alignment and Functional Tests

3.4.1 Connect power supplies, +15V to edge-pin 22, +24V to edge-pin 24 and 0V to edge-pin 9. Check the current consumption of both the supplies (+15V supply not more than 25mA, +24V not more than 100mA).

3.4.2 LO Level

Set the signal generator to 63.6MHz at 650mV level and connect to SKTH (LO2 input). Set the Avometer on the 100uA range and connect to edge-pin 10 and earth. Adjust C20 and C24 for maximum reading on the meter (70 to 100uA).

3.4.3 Gain

Set the signal generator to 65MHz at 100mV r.m.s. level and connect to SKTA (IF). Con- nect the millivoltmeter to SKTB (1.4MHz 2nd IF O/P).

Adjust the signal generator frequency to give a reading on the millivoltmeter of 350 ± 20mV. Apply a logic 1 level (+15V) to edge-pins 4, 5, 6, 7 and 8 and check that the millivoltmeter reading varies by less than 4dB overall (tuning to maximum reading each time).

3.4.4 Bandwidth Check

Select the narrowest bandwidth (100Hz for Module 3, 300Hz for Module 3A) by applying a logic 1 level (+15V) to the appropriate edge-pin (Module 3 - pin 4, Module 3A pin 5). Adjust the 65MHz input at SKA in the positive direction until a 6dB attenuation is indicated on the millivoltmeter. Select the next filter (apply a logic 1 level (+15V) to appropriate edge-pin) and check that the millivoltmeter reading increases again. Continue through all the filters from the narrowest to the widest, checking the selection of filters corresponds, firstly to the edge of one filter and then switching in the next. Repeat the above checks with 65MHz input adjusted in the negative direction.

3.4.5 SSB Switching

Select Bandwidth '6kHz' by applying a logic 1 level (+15V) to edge-pin 7, and find the edge of the filter by adjusting the 65MHz IF input signal at SKA (as in paragraph 3.4.4). Remove the logic 1 level from edge-pin 7 and select, in turn 'ISB', 'USB' and 'LSB' by applying the logic 1 level (+15V) to edge-pins 14, 12 and 13 respectively. In each case check that the 6kHz filter has been selected.

3.4.6 Inspection

Inspect the module to ensure that no damage has been caused during testing.

4. COMPONENT LISTS

Module 3 Main Assembly (630/1/20093/006)
Module 3A Main Assembly (630/1/32983/002)

Note: Items marked * are not used in Module 3A.

Panel Electronic Circuit (419/1/18806)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Panel Printed Circuit	Plessey	419/2/18006
-	Heatsink	Redpoint 5C	419/4/98002
C7,10	Capacitor 100pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/011
C8,74	Capacitor 120pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/013
C13-16	Capacitor 330pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/027
C1,3,4,11, 12,17,18, 19,21,22, 23,26,27, 32-35,37- 40,48-52, 71,72	Capacitor 4.7nF ± 10% 100V	Erie 8111M-X7R	400/4/21280/001
C5,25,28- 31,36,41- 47,53-57, 62-66,68- 70	Capacitor 0.1uF ± 5% 100V	Siemens B32560 100V	435/4/90317/014
C58,59	Capacitor 22pF ± 5% 100V	Erie 812M-100-C0G	400/4/20672/015
C73	Capacitor 180pF ± 2.5% 30V	Suflex HSC30	437/4/30011/015
C24	Capacitor Variable 2-18pF	Mullard 809-09003	401/4/32189/003
C20	Capacitor Variable 4-40pF	Mullard 809-09002	401/4/32131/001
L5	Inductor 0.12uH ± 10%	Sigma SC30	406/4/31753/001
L8	Inductor 0.33uH ± 10%	Sigma SC10	406/4/31749/003
L9	Inductor 0.47uH ± 10%	Sigma SC10	406/4/31749/007
L4	Inductor 1uH ± 10%	Sigma SC10	406/4/31749/004
L6,7	Inductor 6.8uH ± 10%	Sigma SC10	406/4/31749/008
L1,3,11,12	Inductor 100uH ± 10%	Sigma SC10	406/4/31741/002
L10,13-23	Inductor 220uH ± 10%	Sigma SC10	406/4/31749/006
L2,24,26-33	Inductor 22uH ± 10%	Sigma SC10	406/4/31749/002
R28	Resistor 4.7R ± 5%	ITT RDO 25J	403/4/04329/009
R14	Resistor 15R ± 2%	Electrosil TR4	403/4/05521/150
R15	Resistor 82R ± 2%	Electrosil TR4	403/4/05521/820
R16-27	Resistor 220R ± 2%	Electrosil TR4	403/4/05522/220
R5	Resistor 390R ± 2%	Electrosil TR4	403/4/05522/390
R8	Resistor 470R ± 2%	Electrosil TR4	403/4/05522/470
R9,12,29-33	Resistor 1k ± 2%	Electrosil TR4	403/4/05523/100
R7	Resistor 1.5k ± 2%	Electrosil TR4	403/4/05523/150
R13	Resistor 2.2k ± 2%	Electrosil TR4	403/4/05523/220
R3	Resistor 3.9k ± 2%	Electrosil TR4	403/4/05523/390
R10	Resistor 8.2k ± 2%	Electrosil TR4	403/4/05523/820
R1	Resistor 10k ± 2%	Electrosil TR4	403/4/05524/100
R6,11	Resistor 27k ± 2%	Electrosil TR4	403/4/05524/270
R34-39	Resistor 100k ± 2%	Electrosil TR4	403/4/05525/100
D1,14-17	Diode	Texas 1N4148	415/4/05720
D2-11	Diode	Hewlett Packard HP5082-3188	415/4/05743

Panel Electronic Circuit (Cont'd)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
D13	Diode	Hewlett Packard HP5082-2800	415/4/98532
D12	Diode	Mullard BZY88C6V2	415/4/05738/011
T1	Transformer	Plessey	406/9/29657/011
T2	Transformer	Plessey	406/9/29657/014
T3,4	Transformer	Plessey	406/9/29657/006
T5	Transformer		406/9/29657/002
T6	Transformer	Plessey	406/9/29712
T7	Transformer	Plessey	406/9/29713
TR1	Transistor	Texas 2N5109	417/4/01784
TR4	Transistor	Texas 2N3866	417/4/01775
TR5-9	Transistor	Mullard BC109	417/4/01776
TR2,3	Transistor	Signetics SD210	417/4/01887/001
XL1	Crystal	ITT FC2239	428/9/05039
XL2	Crystal	ITT FC2240	428/9/05040

Filters

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
XF1*	Filter Bandpass	ITT	422/9/07786/001
XF2	Filter Bandpass	ITT	422/9/07786/004
XF3	Filter Bandpass	ITT	422/9/07786/003
XF4	Filter Bandpass	ITT	422/9/07786/007
XF5*	Filter Bandpass	ITT	422/9/07786/002

Connector Assembly (702/1/20093/004)

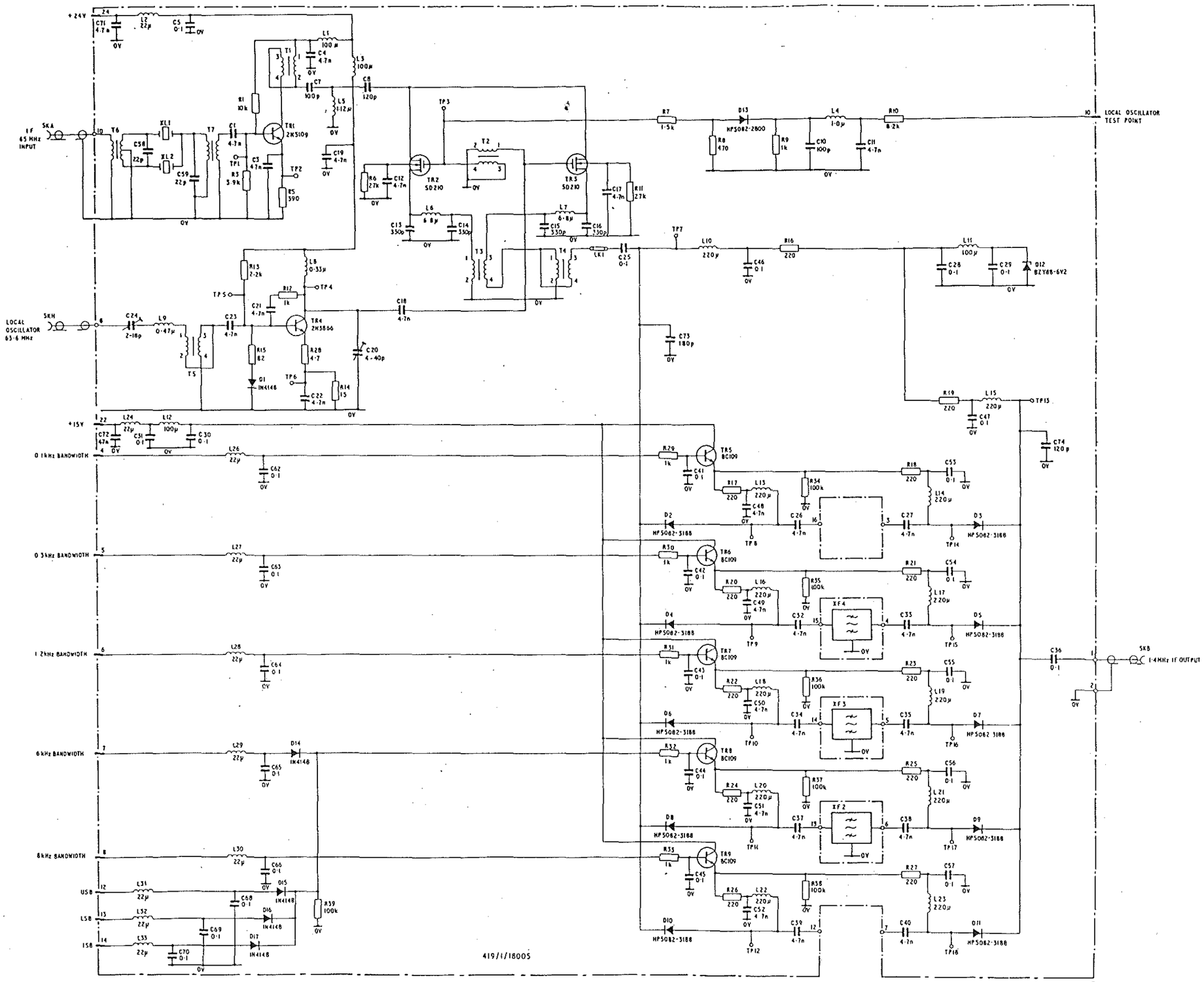
Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
SKB	Socket Electrical R.F.	Belling Lee L1465/K/BS	508/4/22059
-	Cable R.F.	R.G. 174/U 190mm	998/4/70537/001

Connector Assembly (702/1/20093/006)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
SKA	Socket Electrical R.F.	Belling Lee L1465/K/BS	508/4/22059
-	Cable R.F.	R.G. 174/U 230mm	998/4/70537/001

Connector Assembly (702/1/20093/008)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
SKH -	Socket Electrical R.F. Cable R.F.	Belling Lee L1465/K/BS R.G. 174/U 350mm	508/4/22059 998/4/70537/001



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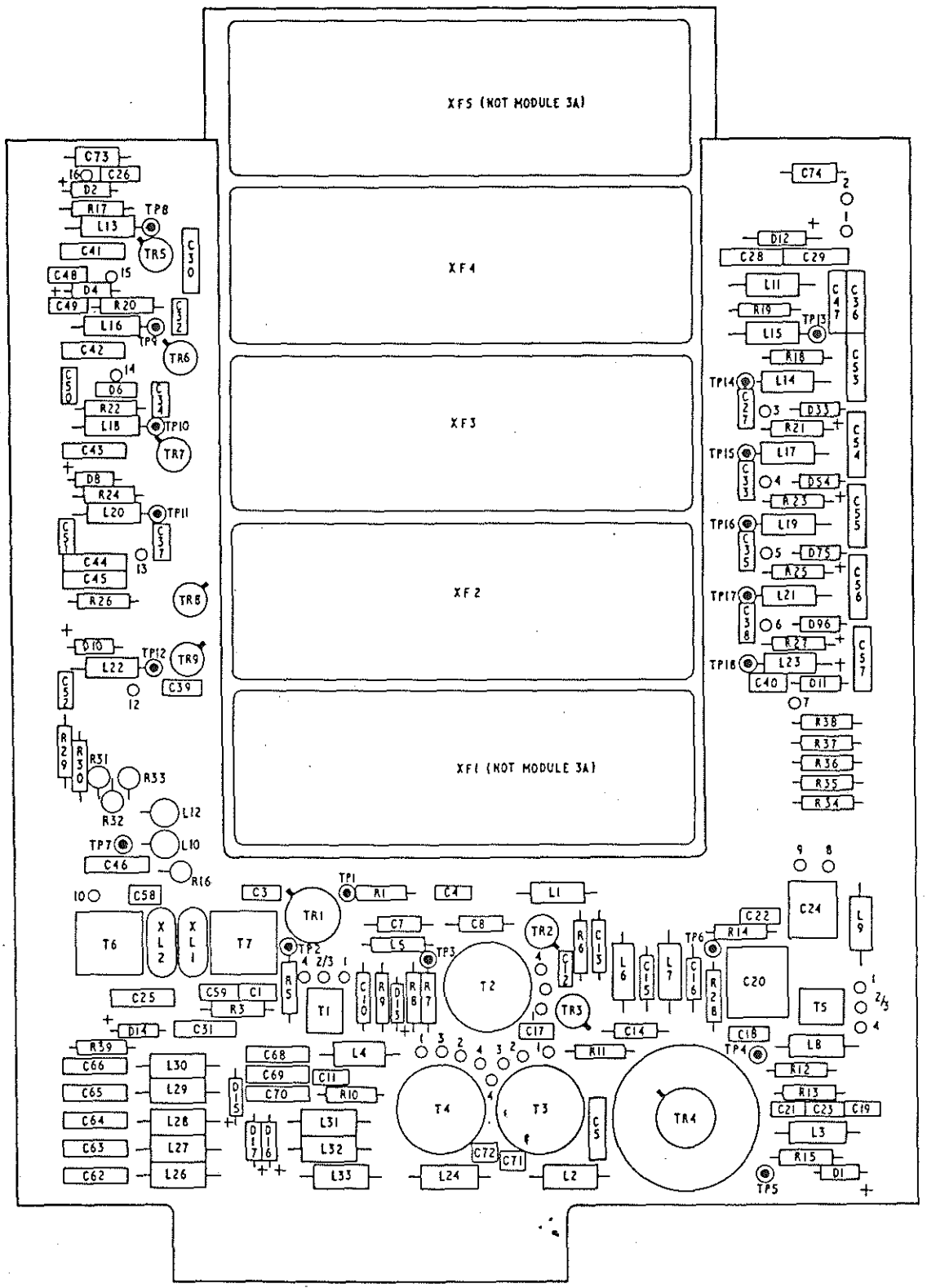
MODULE 3 : IST IF AMPLIFIER 2ND MIXER AND 2ND IF FILTERS CIRCUIT DIAGRAM

FIG 1



MODULE 3 PANEL - COMPONENT LAYOUT

FIG. 2

Connector Assembly (702/1/20093/008)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
SKH -	Socket Electrical R.F. Cable R.F.	Belling Lee L1465/K/BS R.G. 174/U 350mm	508/4/22059 998/4/70537/001

CHAPTER 4

MODULE 4 2ND IF AMPLIFIER, AGC CIRCUITS AND IF FILTERS

CONTENTS

TABLES

ILLUSTRATIONS

MODULE 4 2ND IF AMPLIFIER, AGC CIRCUITS AND IF FILTERS

1. FUNCTIONAL DESCRIPTION

1.1 Module 4 contains the 1.4MHz 2nd i.f. amplifier, the 2nd i.f. distribution circuits, and the a.g.c. detector and time-constant circuits. Module 4 is used in al PR2250 series receivers. A functional block diagram can be seen in Figure (a).

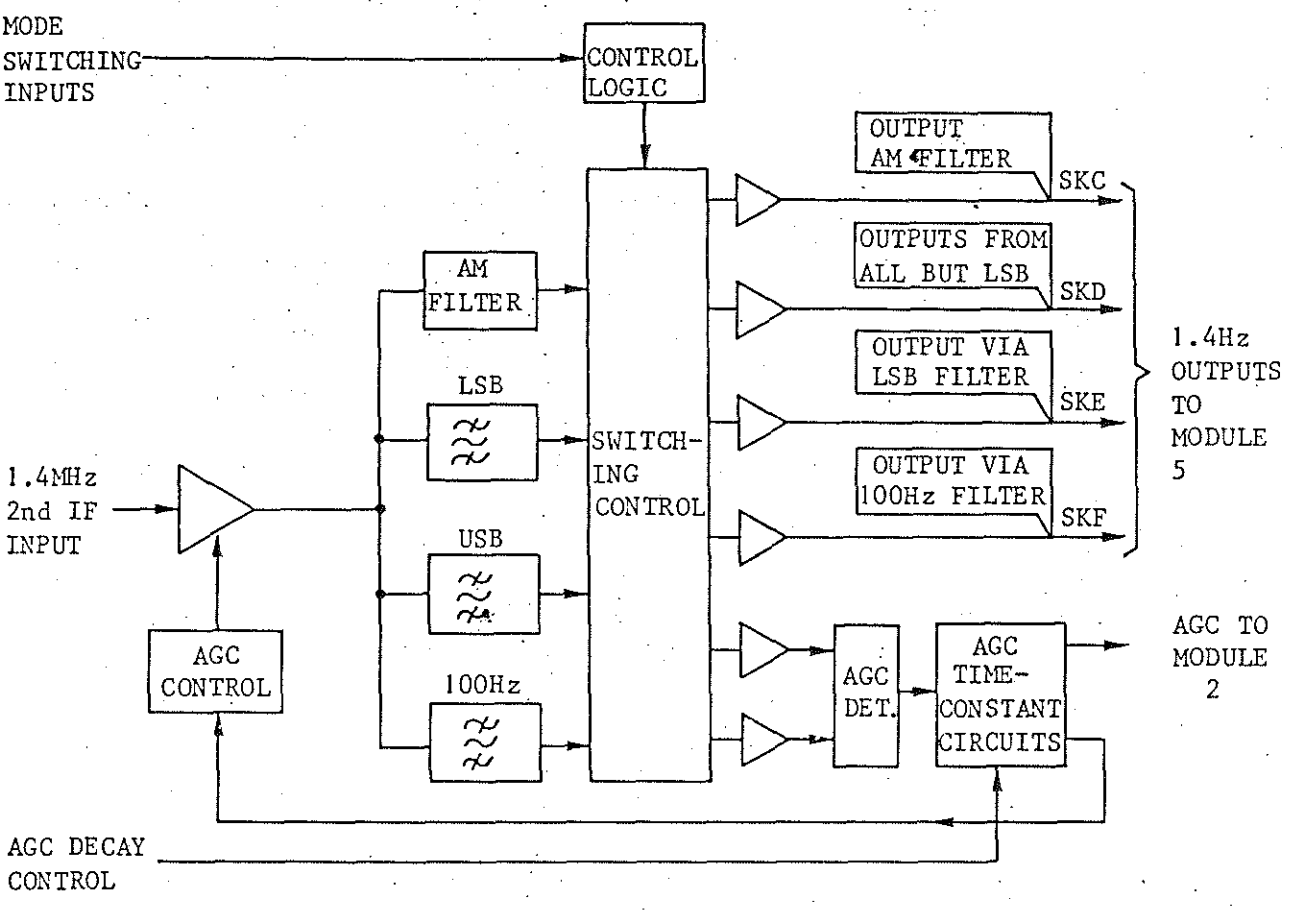


FIG (a) MODULE 4 FUNCTIONAL BLOCK DIAGRAM

1.2 The 1.4MHz 2nd i.f. signal from Module 3 is amplified in an a.g.c.-controlled circuit and applied to the parallel inputs of three band-pass filters 1.4MHz +250Hz -3kHz, 1.4MHz +3kHz -250Hz, and 1.4MHz ± 50Hz and an AM FILTER. Outputs from selected lines are switched by the MODE logic switching inputs to the flow output lines as follows:-

(1) AM mode : (a) from AM FILTER to SKC.
(b) from 100Hz filter to SKF.

(2) CW mode (not 0.1 bandwidth) : (a) from AM FILTER to SKD.
(b) from 100Hz filter to SKF.

(3) CW mode and 0.1 bandwidth : from 100Hz filter to SKD and SKF.

(4) F mode (not 0.1 bandwidth) : (a) from AM FILTER to SKD.
(b) from 100Hz filter to SKF.

(5) F mode and 0.1 bandwidth : from 100Hz filter to SKD and SKF.

(6) LSB mode (not 0.1 bandwidth) : (a) from LSB filter to SKE.

(b) from 100Hz filter to SKF.

(7) ISB mode (not 0.1 bandwidth) : (a) from AM filter to SKC.

(b) from 100Hz filter to SKF.

(c) from LSB filter to SKE.

(d) from USB filter to SKD.

(8) USB mode (not 0.1 bandwidth) : (a) from USB filter to SKD.

(b) from 100Hz filter to SKF.

1.3 In all operating modes except USB, ISB, and LSB, the a.g.c. detector input is connected to the i.f. output via the AM FILTER. In USB mode it is connected via the USB filter. In LSB mode it is connected via the LSB filter. In ISB mode, two inputs are connected, one from the LSB filter and one from the USB filter, in order that the a.g.c. circuits may react to both sidebands. The varying d.c. output produced by the a.g.c. detector is controlled in respect of rise and decay times by the a.g.c. time-constant circuits: the decay times can be selected by front-panel control. Rise time is approximately 5mS, and decay time can be selected at 0.2, 2, or 10 seconds. The circuit will react to a short noise pulse on a substantially steady signal with a decay time-constant of 50mS.

2. CIRCUIT DESCRIPTION

2.1 2ND IF Amplifier

2.1.1 The 1.4MHz second IF amplifier is formed by IC1, IC2, TR1, TR2, TR3, and associated components. The input signal is applied from SKA via capacitor C1 to a two-stage non-inverting amplifier formed by IC1 and IC2. The amplifier is a.g.c.-controlled by the inputs to pin 7 of both ICs; a positive-going increase in a.g.c. input level reduces gain. Zener diode D2 limits the a.g.c. input to IC2 at +3.3V. Maximum overall gain is 64dB ± 4dB.

2.1.2 The output from IC2 is applied via emitter-follower TR1 to an inverting cascade stage formed by TR2, TR3, and associated components. The negative feedback from TR3 collector to TR1 base is pre-set to produce a gain of approximately 3 between the input via C3 and the output via C8.

2.2 Bandpass Filters

The 1.4MHz amplified 2nd IF output from TR3 is applied via C8 to the parallel inputs of three bandpass filters. The output from TR3 is of very low impedance: the characteristic impedance of each filter is 1 kilohm, therefore the filter inputs are supplied via series resistors R13, R14, R15 and R16. XF1, XF2, and XF3 are encapsulated crystal filters. The 'AM FILTER' is formed by C11, C12, C13, C14, C15, L4 and L5. The output from each filter is taken via an emitter-follower buffer to the switching circuits. Sideband reversal occurs in Module 2 (Sect.4, Ch.2) and for this reason, XF1 in the USB path is a lower sideband filter and XF2 in the LSB path is an upper sideband filter.

2.3 Switching Logic

2.3.1 The output signals from the three filters are continuously available. According to the MODE and BANDWIDTH front-panel control settings in use, selected outputs are connected to particular output sockets, as shown in table 1.

TABLE 1 : SWITCHED SIGNAL PATHS

MODE:- B/WIDTH:-	AM	CW Not 0.1	CW 0.1	F Not 0.1	F 0.1	LSB Not 0.1	ISB Not 0.1	USB Not 0.1
FROM:- TO:-	AM FILTER SKC	AM FILTER SKD	XF3 SKD	AM FILTER SKD	XF3 SKD	XF2 SKE	AM FILTER SKC	XF1 SKD
FROM:- TO:-	XF3 SKF		XF3 SKF	XF3 SKF	XF3 SKF	XF3 SKF	XF3 SKF	XF3 SKF
FROM:- TO:-							XF1 SKE	
FROM:- TO:-							XF2 SKD	

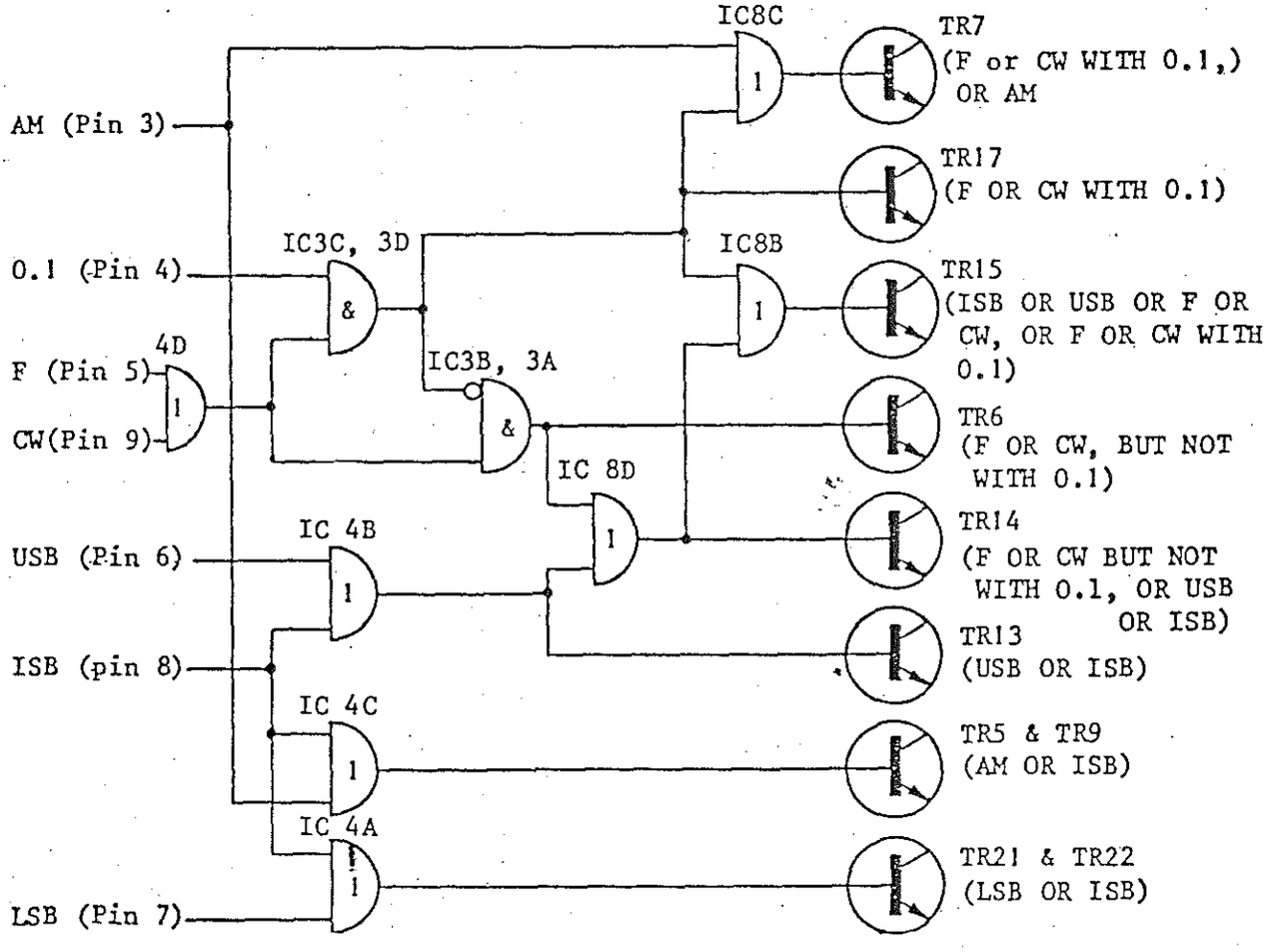


FIG (b) MODULE 4 MODE SWITCHING LOGIC

TABLE 2 : SWITCHING ACTION

	INPUTS AT LOGIC '1'							
	'AM'	'CW'	'CW' & '0.1'	'F'	'F' & '0.1	'LSB'	'ISB'	'USB'
TR5	ON						ON	
TR6		ON		ON				
TR7	ON		ON		ON			
TR9	ON							
TR13							ON	ON
TR14		ON		ON			ON	ON
TR15		ON	ON	ON	ON		ON	ON
TR17			ON		ON			
TR21						ON	ON	
TR22						ON	ON	

2.3.2 The connections defined in table 2 are made by logic circuits which operate ten switching transistors, TR5, 6, 7, 9, 13, 14, 15, 17, 21, and 22. The logic circuits are controlled by the levels applied to panel edge-pins 3 to 9 inclusive. The circuit is shown in Fig.(b) reduced to its basic functions.

2.3.3 All control inputs to the switching logic are quiescent at logic '0' in positive logic. Pin 4 ('0.1') level can only be set to '1'. When either pin 5 ('F'), pin 9 ('CW') or pin 3 ('AM') is also at logic '1'. Eight valid input combinations exist, as shown in table 2: each combination causes a particular set of switching transistors to conduct, as can be seen from Fig.(b) and table 2.

2.4 Action of Switching Transistors

The action of the ten switching transistors is as defined in this paragraph.

(1) TR5 : forward biases D4 to connect the AM filter output from TR4 to TR8 base.

(2) TR6 : forward biases D5 to connect the AM filter output from TR4 to TR16 base and to D7.

(3) TR7 : forward biases D6 to connect the AM filter output from TR4 to TR11 base.

(4) TR9 : applies collector voltage to output stage TR8.

(5) TR13 : forward biases D8 to connect XF1 output from TR10 to TR16 base.

(6) TR14 : forward biases D7 to connect the AM filter output via D5 to TR12 base.

(7) TR15 : applies collector voltage to output stage TR16.

(8) TR17 : forward biases D9 to connect XF3 output from TR18 to TR16 base.

(9) TR21 : forward biases D10 to connect XF2 output from TR20 to TR23 base.

(10) TR22 : applies collector voltage to output stage TR23.

2.5 AGC Input and Detector Circuits

2.5.1 Automatic gain control is applied to 1.4MHz 2nd IF amplifiers IC1 and IC2. The signal from which this control is derived is taken either from R32, the emitter load common to TR11 and TR12, or from R53 in TR23 base circuit. The signal across R32 feeds a.g.c. input amplifier IC10, while the signal across R53 feeds a.g.c. input amplifier IC9. The selection of the input signal to the a.g.c. circuits is carried out by switching transistors TR6, TR7, TR13, TR14, TR17, and TR21 under the control of the switching logic. The action can be seen in table 3.

TABLE 3 : AGC SIGNAL SELECTION

MODE	SWITCHES ON	SIGNAL PATH	AGC AMP FED
AM	TR7	AM Filter : -D6-TR11-R32	IC10
CW	TR6, TR14	AM Filter : -D5-D7-TR12-R32	IC10
CW & 0.1	TR7	AM Filter : -D6-TR11-R32	IC10
F	TR6, TR14	AM Filter : -D5-D7-TR12-R32	IC10
F & 0.1	TR7	AM Filter : -D6-TR11-R32	IC10
LSB	TR21	XF2-D10-R53	IC9
ISB	TR21	XF2-D10-R53	IC9) Both fed in
	TR13, TR14	XF1-D8-D7-TR12-R32	IC10) ISB mode
USB	TR13, TR14	XF1-D8-D7-TR12-R32	IC10

Note that the outputs from two filters are used when working ISB to cater for variations in both sidebands: XF2 is a lower sideband path filter, while XF1 is an upper sideband path filter.

2.5.2 The output from IC9 is fed via C51 to peak detector D14-D16 with R86 and C54. The output from IC10 is fed via C52 to peak detector D13-D15. D13-D14 junction is returned to +4.8V at the collector of voltage-source TR30: this potential is temperature-compensated by D17 and the base-emitter diode of TR30. D15-D16 junction is returned to +6V at the junction of R85 and R112: the diodes are therefore forward biased by 1.2V, which ensures that the a.g.c action is available for very small signal amplitudes.

2.5.3 The peak detector output rise time is determined by the 1 millisecond time-constant of R86 and C54. C55 provides a low impedance a.c. path to 0V, and takes no part in the time-constant: the 6V d.c. potential across C55 provides the reference voltage input to pin 2 of IC5.

2.5.4 The difference in potential between pins 2(-) and 3(+) of IC5 forms the initial unshaped a.g.c. signal: a positive-going change at pin 3 will reduce r.f. and i.f. gain, while a negative-going change will increase r.f. and i.f. gain. To remove a.g.c. control, a positive (logic 1) level is applied to panel edge-pin 14; this causes TR32 to conduct, so holding the level on pin 3 of IC5 below +1V. To mute the receiver, a maximum positive level is required on pin 3 of IC5; this is produced by earthing panel edge-pin 11, so causing TR31 to conduct and hold the level on pin 3 of IC5 above +11V.

2.5.5 The d.c. output level produced by IC5 is proportional to signal amplitude, and varies at no defined rate. The rates of rise and fall are controlled by the shaper circuits associated with TR33 to TR34 (inclusive).

2.6 AGC Shaper Circuits

2.6.1 The shaper circuits can be functionally divided into three parts:

(1) A fast time-constant circuit formed by TR33, TR34, and associated components.

(2) A slow time-constant circuit formed by TR35, TR36, TR37, and associated components.

(3) A combining circuit formed by TR38, TR39, and associated components.

The circuits produce a short (nominal 5mS) attack time-constant for all input level increases, and any selected one of three (nominal 0.2S, 2S, 10S) decay time-constants for signals of duration greater than approximately 75 mS. For signals of duration less than approximately 75mS, a decay time-constant of nominally 50mS is produced. The action will be described in terms of the response to an input signal as shown in Fig. (c), as this brings out every aspect of the circuit operation.

2.6.2 Long Time-Constant Circuit

2.6.2.1 The output from IC5 applied to TR35 base: it can (at a maximum) change from 0V to +24V. As full a.g.c. control is achieved over a 0V to +12V range, time-constant values of CR seconds (in which output voltage rises to 69% of input voltage) can truly be quoted as rise and fall times.

2.6.2.2 Assume that TR35 base potential is 0V and that C59 is completely discharged, when a positive-going input step is applied to TR35 base. (The fact that it is also applied to TR33 and TR34 bases is not relevant at the moment). C59 will charge via R98, the time-constant being approximately 65 milliseconds. If, after the voltage across C59 has reached a steady state, a negative-going step is applied to TR35 base, C59 will discharge via either R99, R100, or R103; the particular resistor in circuit will depend upon the front-panel selection of a.g.c. decay time-constant. The discharge time-constant will be nominally 0.2 seconds (R103), 2 seconds (R100) or 10 seconds (R99). Note that edge-pin 11 provides a monitor output: it is not a control input. The voltage across C59 (waveform C in Fig.(c)) is applied to TR38 base. The combining action of TR38 and TR39 cannot be considered until the short time-constant circuit has been described.

2.6.3 Short Time-Constant Circuit

2.6.3.1 The output from IC5 is applied to the bases of TR33 and TR34. C57 in TR33 emitter circuit charges via R93, and discharges via R94. C58 in TR34 emitter circuit charges via R95, and discharges via R97. C57 and C58 potentials are clamped within $\pm$ 1V by diodes D20, D21, D22, and D23.

2.6.3.2 Consider a positive-going step applied to TR33 and TR34 bases from a starting point where both C57 and C58 are completely discharged. C57

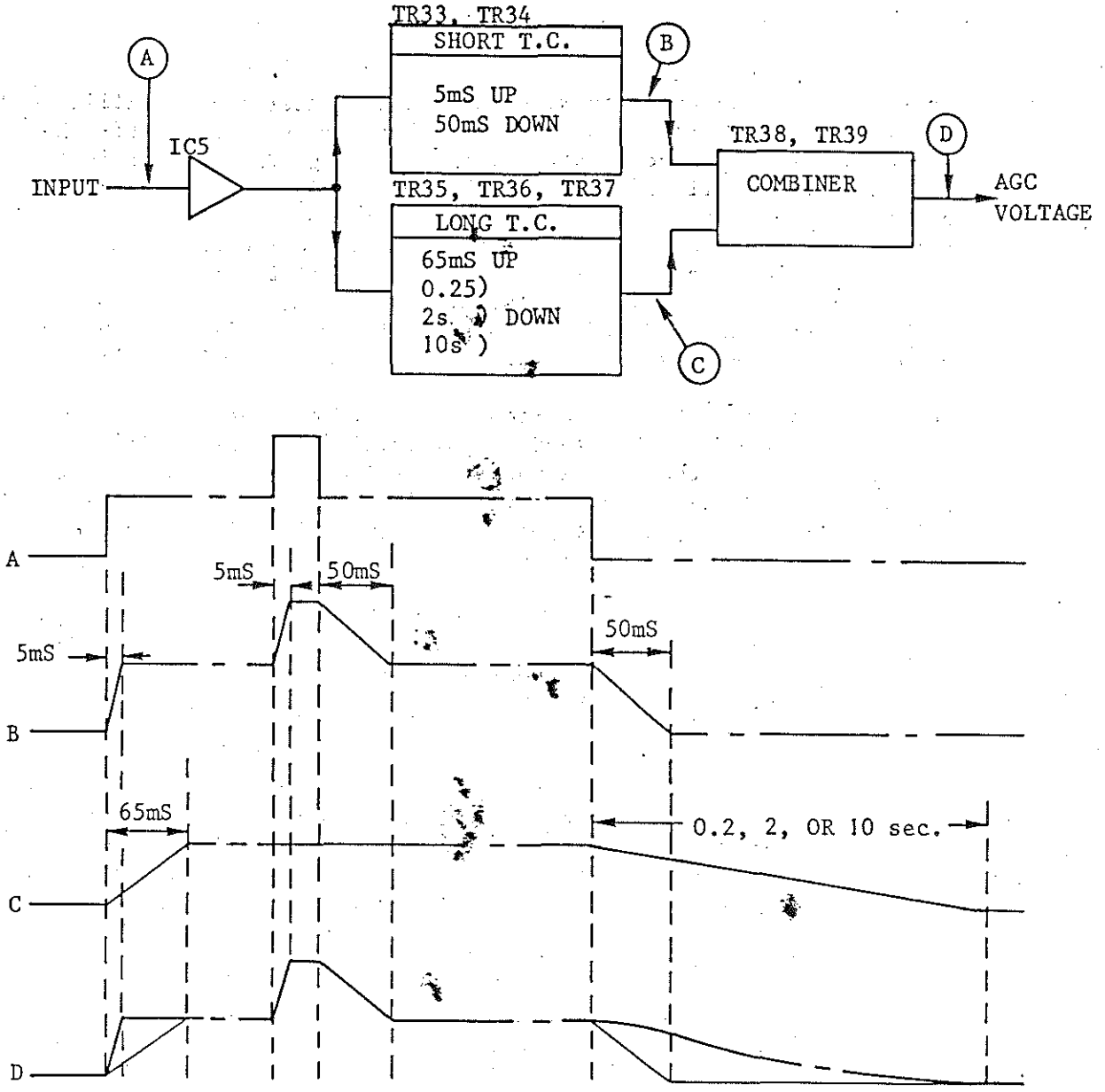


FIG. (c) AGC SHAPER CIRCUIT ACTION

and R93 form a 3 millisecond charging time-constant, while C58 and R95 form a millisecond charging time-constant. Initially the output from R96-R97 junction will rise at a 22 millisecond TC rate, but this will only apply until the voltage across C57 exceeds that across C58 by +1V. At this point D22 and D23 will conduct, parallel connecting the two emitter circuits to produce a 5 millisecond time-constant from C57 and C58 charging via R93 and R95 in parallel. The rate of voltage rise at R96-R97 junction will be determined by this time-constant.

2.6.3.3 Consider the arrival of a short noise pulse after the circuit has reached a steady state. A short pulse of some 10 millisecond duration will not significantly affect the potential across C59, as here the rise time-constant is 65 milliseconds. Initially C57, C58, and C59 potentials will be equal. The leading-edge positive step of a noise pulse will cause the voltage across C57 to rise until it is +1V greater than that across C58, at which point the 5 millisecond rise time-constant is produced. The voltage at R96-R97 junction will rise to take account of the noise pulse leading edge.

2.6.3.4 Assuming that the noise pulse duration is greater than 5 milliseconds, the voltage at R95-R97 junction will then remain steady until the arrival of the negative-going step of the trailing edge. On arrival of this step, C58 will initially discharge via R95 and R97 (a time-constant of 288 milliseconds). This will only apply until the 27 millisecond time-constant of C57 and R94 has reduced the potential across C57 to 1V below that across C58. At this point D20 and D21 will conduct, parallel connecting the two discharge time-constants to produce a circuit of 20uF (C57 and C58) discharging via 2.47k ohm (R95-R97 in parallel with R94), a time-constant of approximately 50 milliseconds.

2.6.3.5 The potential at R95-R97 junction will therefore decay at a 50 millisecond TC rate until the steady input level is reached. This level will remain until the end of the steady input level period, when the potential at R95-R97 junction will again decay at a 50 millisecond TC rate: at the same time, the potential across R59 will decay at either a 0.2 second, 2 second, or 10 second rate.

2.6.4 Combiner

The output from the short time-constant circuit is taken from R95-R97 junction and is applied to TR39 base. The output from the long time-constant circuit is taken from TR35 base and is applied to TR38 base. The potential across R106 is governed by the more positive of the two base potentials. The effect is to produce a combined output in which the short (5mS) time-constant governs all rise times, and in which the 50 millisecond time-constant governs the decay rate of signals shorter than 70 milliseconds. The decay rate of signals of longer duration is governed by the long (0.2s, 2s, or 10s) time-constant. The overall response to the input waveform A shown in Figure (c) will be that shown by the heavy line in waveform D of Figure (c).

3. TEST DATA

3.1 General

The procedure outlined in the following paragraphs forms a complete test procedure and need not be used to locate individual faults.

3.2 Test Equipment

The following items of test equipment are required:

Signal Generator, 1.4MHz, 8uV r.m.s., -8mV r.m.s., 50 ohms.

Matching Network, 50 ohms to 1k ohms, 6dB loss, to match the signal generator to Module 4 input impedance. The network is shown in Figure (d).

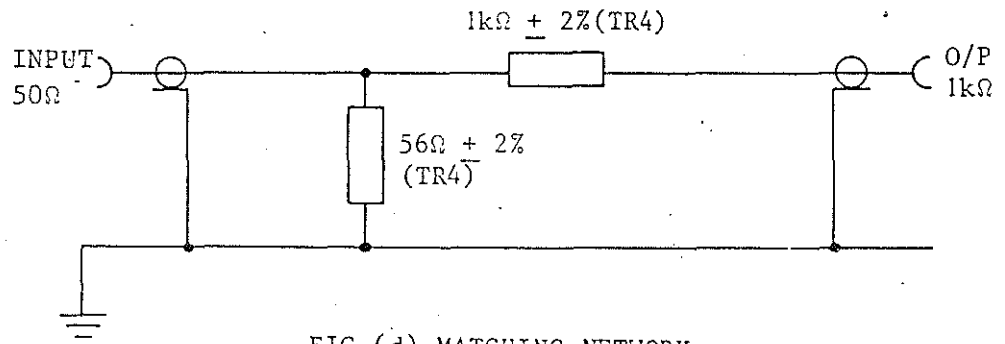


FIG (d) MATCHING NETWORK

Millivoltmeter, 1.4MHz to read 10mV, 50 ohm impedance and high impedance.

Avometer.

Variable DC supply (0-12V).

3.3 Power Supplies

Separate +15V and +9V DC power supplies are required.

3.4 Alignment and Functional Tests

3.4.1 Connect the +15V supply to edge-pin 22, +9V to edge-pin 20 and 0V to edge-pin 1. Check the current consumption of the supplies, +15V not more than 250mA, +9V not more than 25mA. Using the Avometer check the d.c. voltage level at IC6 pin 2 (12 $\pm$ 0.6V), and at IC7 pin 2 (6 $\pm$ 0.3V).

3.4.2 To allow individual selection of the following modes, LSB, AM, ISB, USB, CW, F, EXT AGC and MUTE a logic '1' level (+15V) should be applied to all the appropriate edge-pins. To switch an individual mode on, the logic 1 is removed.

3.4.3 Gain Setting (USB)

Set the signal generator to 1.4MHz, 6uV r.m.s. and connect via the matching network to the IF INPUT, SKTA. Select the USB mode by removing the logic 1 level from edge-pin 6. Connect the millivoltmeter to USB/ISB/F/CW output SKTD. Adjust the signal generator to give a maximum reading on the millivoltmeter (approximately 1kHz below 1.4MHz: note that an LSB filter is used in the USB mode position as the signal is inverted at this point). Adjust R8 on the module to give a 10mV reading on the millivoltmeter. Remove the signal input to SKTA and check that the fall in millivoltmeter reading is not less than 25dB. Re-connect the input signal to SKTA. Select all of the modes, in turn, by removing the logic '1' from the appropriate edge-pin and check that the signal present, on the millivoltmeter, is on modes USB, ISB, CW and F only.

3.4.4 LSB

Select LSB by removing the logic '1' level from edge-pin 7. Connect the millivoltmeter to LSB/ISB output SKTE, and adjust the signal generator to give a reading on the millivoltmeter of 10 $\pm$ 2mV. Select all modes in turn (remove logic '1' from appropriate edge-pins) and check that the signal is present on modes LSB and ISB only.

3.4.5 Pilot Carrier

Connect the millivoltmeter to 'RECON CARRIER' SKTF, and adjust the signal generator to give a reading on the millivoltmeter of 10 $\pm$ 2mV.

3.4.6 AM

Select mode 'AM' by removing the logic '1' from edge-pin 3. Connect the millivoltmeter to AM/ISB output SKTC and check that the reading is 10 $\pm$ 2mV. Select all modes in turn (remove logic '1' from appropriate pin) and check that the signal is present on modes AM and ISB only.

3.4.7 AGC

Connect the millivoltmeter to SKED. Select mode 'USB' (remove logic '1' from edge-pin 6) and 'AGC SHORT' (apply logic '1', +15V, to edge-pin 13). Adjust the signal generator to give a maximum reading on the millivoltmeter and note the reading. Select AGC 'MED' (apply logic '1' to edge-pin 12) and AGC 'LONG' (absence of a logic '1' on pins 12 and 13 gives AGC long), and check that the reading is unchanged. Select AGC 'SHORT' and increase the signal generator output by 10dB. Adjust R112 to give a reading on the millivoltmeter 1dB higher than the first reading noted for AGC 'SHORT'. Increase signal generator output by a further 60dB and note the rise in millivoltmeter reading from the first reading noted. (should not be more than 3dB). Connect a 100uA FSD meter to edge-pins 16 (RF METER) and 1 (0V) and check that the meter reading is 70 to 85uA. Decrease the signal generator output by 30dB and check that the meter reading is 40 to 50uA. Select mode 'LSB' and check that the meter indication drops to '0'. Adjust the signal generator for maximum reading on the millivoltmeter (40 to 50uA on RF meter). Select mode 'USB' and check that the RF meter drops to '0'. Connect a 0-12V variable d.c. supply to edge-pin 18 (simulates LOCAL RF/IF GAIN Control) and a logic '1' level (+15V) to edge-pin 10 (LOCAL). Slowly adjust the supply from 0V to 12V noting that the RF meter indication follows the operation of the control to full scale deflection of the meter. Reset the variable supply to 0V and repeat for REMOTE RF/IF (0-12V variable supply to REMOTE RF/IF edge-pin 19, and logic '1' (+15V) to pin 15). Adjust the signal generator for maximum indication on the millivoltmeter. Select 'MUTE ON' by removing the logic '1' on edge-pin 11a and check that the RF meter indicates FSD and the millivoltmeter reading drops. Select 'MUTE OFF'. Decrease signal generator output by 40dB (back to threshold). Select AGC 'LONG' (absence of logic '1' on pins 12 and 13 gives AGC LONG) and check that the meter reading is '0'. Increase the signal generator output by 40dB. Disconnect the output from the signal generator and check that the time taken for the meter to drop to 0.5 FSD is approximately 10 seconds. Select AGC 'MED' (logic '1' on edge-pin 12) and reconnect the signal generator output. Disconnect the output and check that the meter drops to 0.5 FSD in approximately 2 seconds. Select AGC 'SHORT' (logic '1' on edge-pin 13) and reconnect the signal generator output. Disconnect the output and check that the meter drops to 0.5 FSD immediately (0.2 sec).

3.5 The module should be inspected to ensure that no damage has been caused during testing.

4. COMPONENT LISTS

Main Assembly (630/1/32984)
Panel Electronic Circuit (419/1/18013)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Panel Printed Circuit	Plessey	419/2/18014
-	Mounting Pad	Jermyn TO5-007N	915/9/98768/000
-	Socket Semi-Conductor	Texas 14LD1L C931402	508/4/22096/002
C70	Capacitor 33pF ± 5% 100V Ceramic	Erie 812M-100 COG	400/4/20672/010
C23,24,31, 32,40,42	Capacitor 68pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/009
C11,13	Capacitor 100pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/011
C69	Capacitor 180pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/015
C12,14	Capacitor 430pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/097
C2,3	Capacitor 1000pF ± 10% 400V	Siemens B32510	435/4/90820/015
C1	Capacitor 0.01uF ± 5% 400V	Siemens B32510	435/4/90820/021
C4-10,16,18, 61	Capacitor 0.1uF ± 5% 100V	Siemens B32510	435/4/90820/014
C17,19-22, 25-29,33-36,38,39, 41,43,44, 46-52,54, 65,66	Capacitor 0.1uF ± 5% 100V	Siemens B32560	435/4/90317/014
C64,67	Capacitor 0.33pF ± 5% 100V	Siemens B32560	435/4/90317/018
C37	Capacitor 0.47uF ± 5% 100V	Siemens B32560	435/4/90317/019
C53,55,60, 62,63	Capacitor 10uF ± 20% 35V	ITT TAG	402/4/57057/006
C57-59	Capacitor 22uF ± 20% 35V	ITT TAG	402/4/55748/015
C15	Capacitor Variable 2-9pF	Mullard 80909002	401/4/32189/002
L1,6,11,15, 18,27	Inductor 22uH ± 10%	Sigma SC10	406/4/31749/002
L10,14,17,20	Inductor 100uH ± 10%	Sigma SC10	406/4/31749/009
L4,5	Inductor 150uH ± 10%	Sigma SC10	406/4/31741/003
L2,7-9,12, 13,16,19	Inductor 220uH ± 10%	Sigma SC10	406/4/31749/006
IC1,2,9,10	Integrated Circuit	Plessey SL612C	445/4/02387
IC3	Integrated Circuit	Motofola MC4011 CP	445/4/02383/011
IC4,8	Integrated Circuit	Motorola MC4071 CP	445/4/02383/071
IC5	Integrated Circuit	Motorola RCA3140 E8	445/4/03072/004
IC6	Integrated Circuit	Fairchild NA7812 UC	445/9/03051/004
IC7	Integrated Circuit	Fairchild NA7806 UC	445/9/03051/002
IC11	Integrated Circuit	Motorola MC4066 CP	445/4/02383/066
R24,37,47,54	Resistor 22R ± 2%	Electrosil TR4	403/4/05521/220
R10	Resistor 51R ± 2%	Electrosil TR4	403/4/05521/510
R26,40,43,56	Resistor 56R ± 2%	Electrosil TR4	403/4/05521/560
R2,5	Resistor 100R ± 2%	Electrosil TR4	403/4/05522/100
R25,33,46, 55,121-124	Resistor 180R ± 2%	Electrosil TR4	403/4/05522/180
R3,18,31,42, 50	Resistor 270R ± 2%	Electrosil TR4	403/4/05522/270
R93	Resistor 390R ± 2%	Electrosil TR4	403/4/05522/390
R7,12,19-22, 32-34,39, 43,51,53, 128	Resistor 470R ± 2%	Electrosil TR4	403/4/05522/470

Panel Electronic Circuit (Cont'd)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
R94	Resistor 560R ± 2%	Electrosil TR4	403/4/05522/560
R109	Resistor 680R ± 2%	Electrosil TR4	403/4/05522/680
R11,80,108	Resistor 820R ± 2%	Electrosil TR4	403/4/05522/100
R4,13-17,23, 30,41,49,59-64,87,113, 120	Resistor 1k ± 2%	Electrosil TR4	403/4/05523/100
R1,89,91,95	Resistor 2.2k ± 2%	Electrosil TR4	403/4/05523/220
R103	Resistor 3.3k ± 2%	Electrosil TR4	403/4/05523/330
R98	Resistor 3.9k ± 2%	Electrosil TR4	403/4/05523/390
R83-85,106	Resistor 4.7k ± 2%	Electrosil TR4	403/4/05523/470
R97	Resistor 5.6k ± 2%	Electrosil TR4	403/4/05523/560
R6	Resistor 6.8k ± 2%	Electrosil TR4	403/4/05523/680
R90,110	Resistor 8.2k ± 2%	Electrosil TR4	403/4/05523/820
R45,86,88,101, 104,107,129, 130	Resistor 10k ± 2%	Electrosil TR4	403/4/05524/100
R111	Resistor 15k ± 2%	Electrosil TR4	403/4/05524/150
R9	Resistor 18k ± 2%	Electrosil TR4	403/4/05524/180
R100	Resistor 82k ± 2%	Electrosil TR4	403/4/05524/820
R27-29,35,36, 44,52,65-71, 102,105, 114-119, 125(Oman).	Resistor 100k ± 2%	Electrosil TR4	403/4/05525/100
R125 (not Oman).	Resistor 1M ± 5%	Allen Bradley CB	403/4/04631/003
R92	Resistor 120k ± 2%	Electrosil TR4	403/4/05525/120
R82	Resistor 270k ± 2%	Electrosil TR4	403/4/05525/270
R99	Resistor 470k ± 2%	Electrosil TR4	403/4/05525/470
R112	Resistor Variable 4.7k	Allen Bradley Type 90H	404/9/05047/004
R8	Resistor Variable 10k ± 20%	Plessey	404/9/05047/005
D2	Diode	Mullard BZY88C3V3	415/4/02792/003
D1,4-31	Diode	Texas 1N4148	415/4/05720
TR1,4-23,26, 32-39	Transistor	Mullard BC107	417/4/01777
TR30,31,40-42	Transistor	Mullard BC177	417/4/01859
TR2,3	Transistor	Texas 2N3866	417/4/01775
XF1	Filter Bandpass	ITT	422/9/07786/005
XF2	Filter Bandpass	ITT	422/9/07786/006
XF3	Filter Bandpass	ITT	422/9/07786/002

Connector Assembly (702/1/20093/001)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
SKA	Socket Electrical R.F.	Belling Lee L1465/K/BS	508/4/22059
-	Cable R.F.	Suhner R.G. 174/U 110 mm	998/4/70537/001

Connector Assembly (702/1/20093/002)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
SKF	Socket Electrical R.F.	Belling Lee L1465/K/BS	508/4/22059
-	Cable R.F.	Suhner R.G. 174/U 150 mm	998/4/70537/001

Connector Assembly (702/1/20093/006)

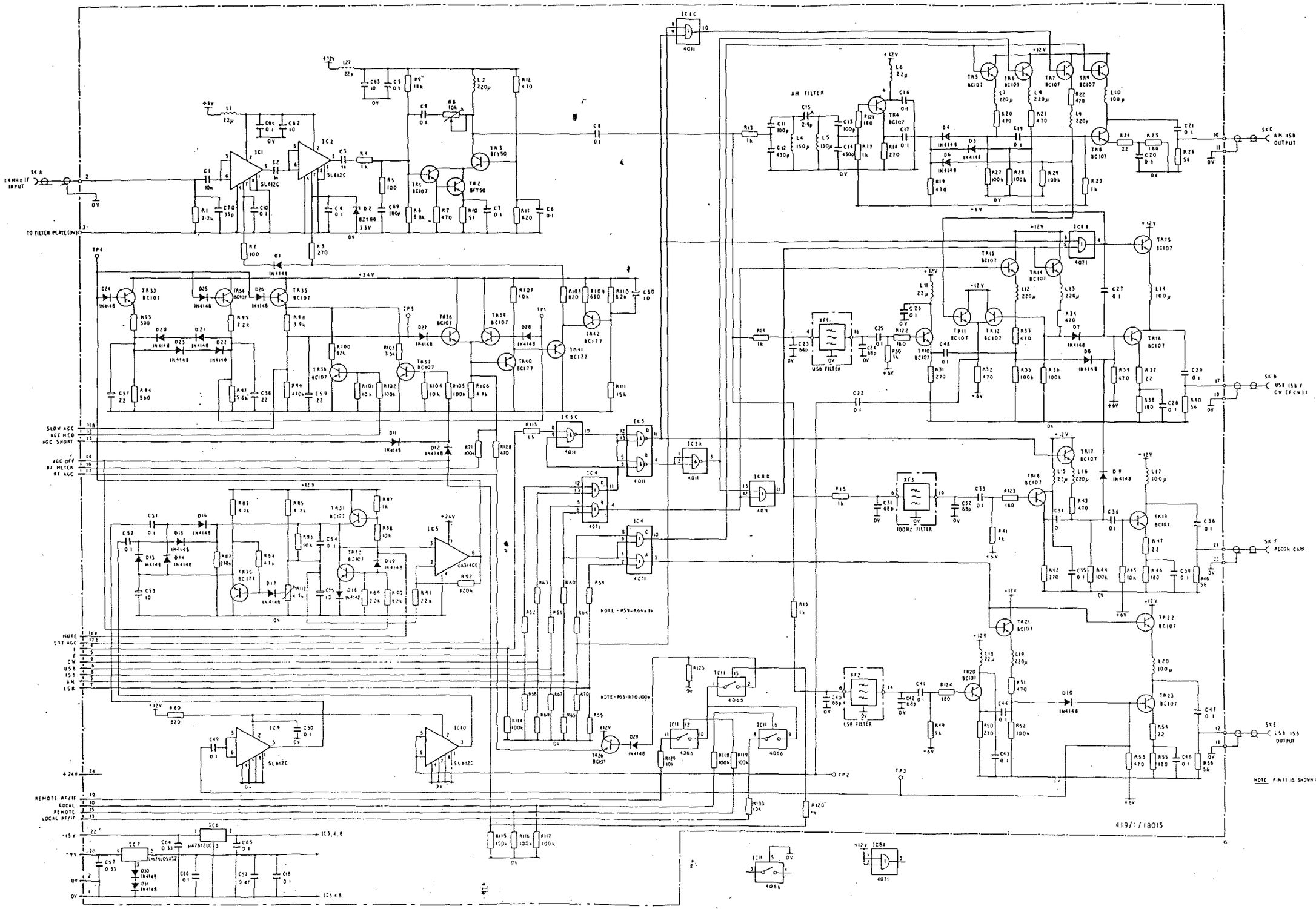
Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
SKD	Socket Electrical R.F.	Belling Lee L1465/K/BS	508/4/22059
-	Cable R.F.	Suhner R.G. 174/U 230 mm	998/4/70537/001

Connector Assembly (702/1/20093/007)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
SKC	Socket Electrical R.F.	Belling Lee L1465/K/BS	508/4/22059
-	Cable R.F.	Suhner R.G. 174/U 290 mm	998/4/70537/001

Connector Assembly (702/1/20093/008)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
SKE	Socket Electrical R.F.	Belling Lee L1465/K/BS	508/4/22059
-	Cable R.F.	Suhner R.G. 174/U 350 mm	998/4/70537/001
-	Screening Cover	Plessey	630/2/33037/003
-	Screening Cover	Plessey	630/2/33037/004



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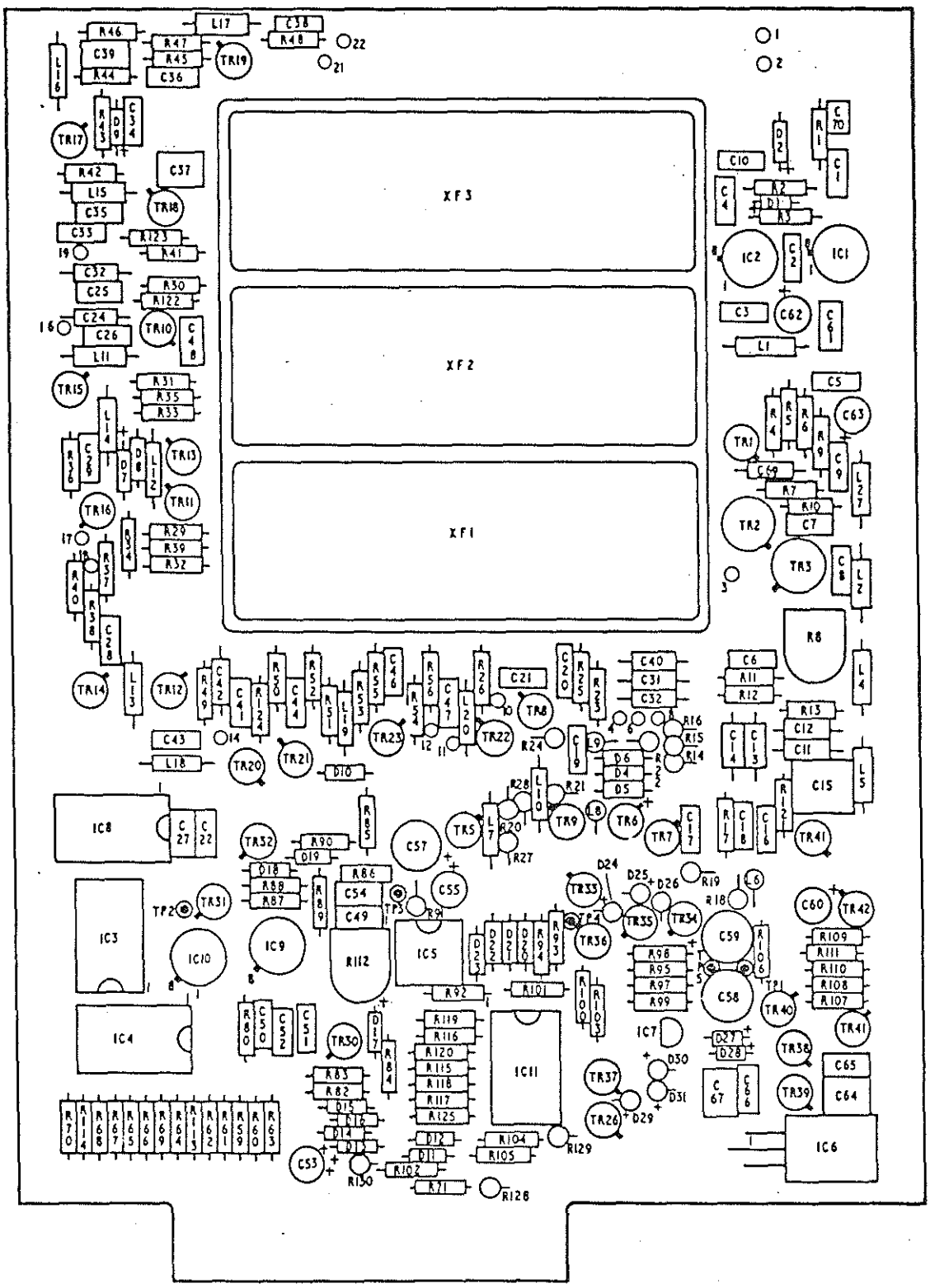
MODULE 4 : 2ND IF AMPLIFIER, A.G.C. CIRCUITS AND IF CIRCUIT DIAGRAM

FIG 1



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MODULE 4 PANEL - COMPONENT LAYOUT FIG. 2

CHAPTER 5

MODULE 5 DETECTORS AND OUTPUT AMPLIFIERS

CONTENTS

TABLES

ILLUSTRATIONS

MODULE 5 DETECTORS AND OUTPUT AMPLIFIERS

1. FUNCTIONAL DESCRIPTION

1.1 Module 5 contains the detector and output circuits of the receiver, together with the associated switching and control circuits. A block diagram can be seen in Figure (a).

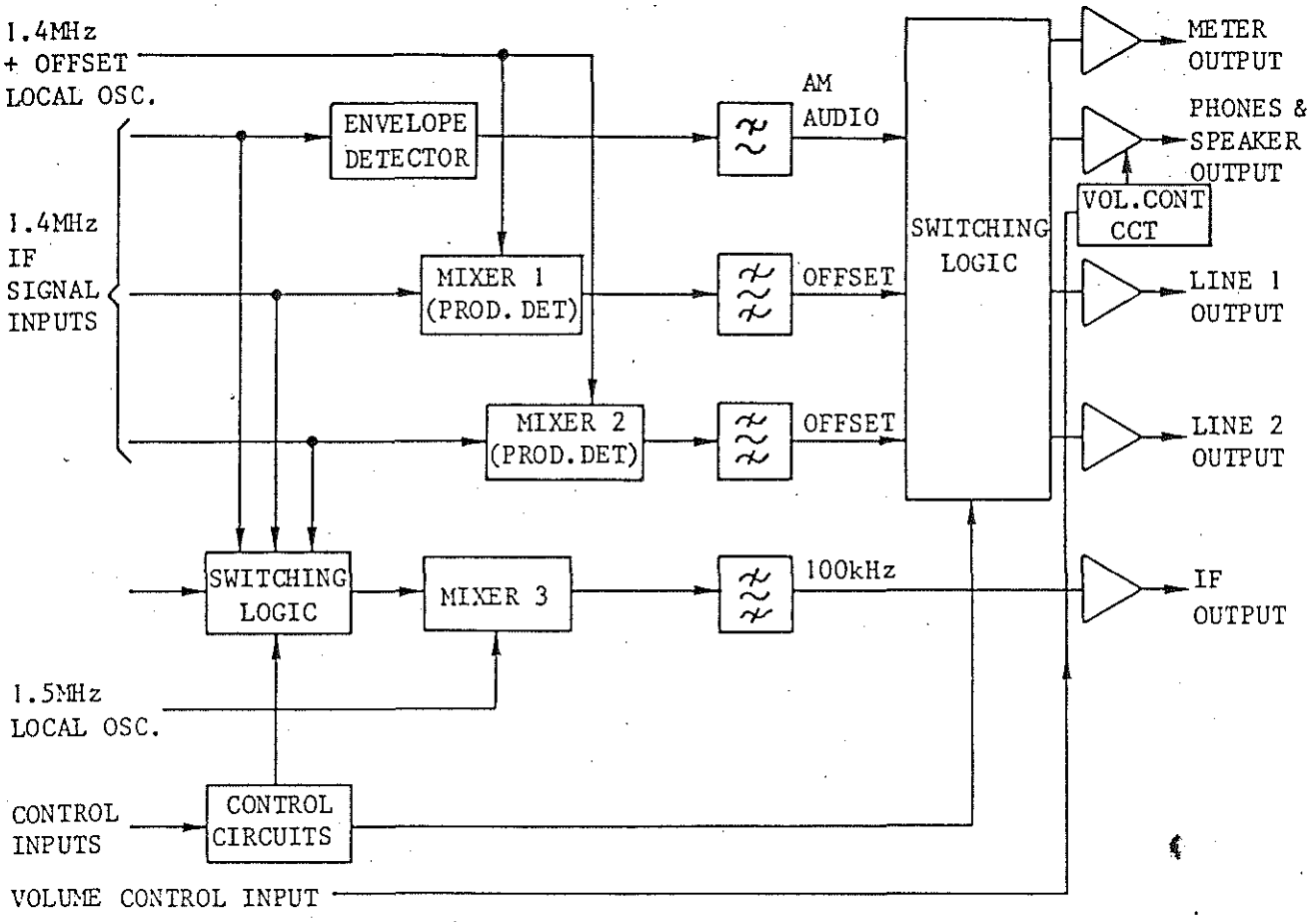


FIG (a) MODULE 5 FUNCTIONAL BLOCK DIAGRAM

1.2 The detection circuits consist of an envelope detector and three mixers. Two of the mixers function as produce detectors; these two share a common 1.4MHz+OFFSET local oscillator input. The third mixer receives a 1.5MHz local oscillator input. Three 1.4MHz IF input signals from Module 4 are applied to Module 5. In ISB mode, two are present simultaneously: in all other modes, only one is present at any given time. The applied input (or inputs, i.e. both sidebands on ISB) is always connected to the input of the third mixer. As this mixer receives a 1.5MHz local oscillator input, any signal input to Module 5 is continuously down-converted to 100kHz to produce the IF OUTPUT.

1.3 An amplitude-modulated input signal applied to the envelope detector produces an audio output; this is used in AM mode. An input signal applied to either product detector produces an output at whatever offset frequency has been set on the local oscillator; this is employed in all modes except AM. When working ISB, the incoming signal is split in Module 4: the upper sideband is fed to Mixer 1, while the lower sideband is fed to Mixer 2.

1.4 Three output amplifiers and a meter amplifier are used in addition to that in the IF OUTPUT circuit already described. One provides the phones and speaker outputs. The second provides one LINE output. The third provides the second LINE output. The inputs to the three output amplifiers are connected as appropriate to the detector outputs by the switching logic, controlled from Module 10.

1.5 Except when working ISB, all detected signals are fed to all output amplifiers. When working ISB, one line amplifier receives USB and one receives LSB: the inputs to the meter amplifier and to the phones and speaker amplifier are then either LSB or USB as determined by the setting of the front-panel MONITOR toggle switch.

2. CIRCUIT DESCRIPTION

2.1 Detectors

2.1.1 Envelope Detector

The AM input from SKA is applied to the inverting amplifier stage formed by TR2 and TR3. The amplifier has two negative feedback paths, D2-R11 for positive half-cycles, and D1-R10 for negative half-cycles. Neither conducts until the signal at TR3 collector is approximately 1.2V peak-to-peak. A small input signal therefore experiences open-loop gain amplification. When amplitude increases sufficiently to cause D1 and D2 to conduct, gain is set by R10 (or R11) and R4. The half-wave rectified output from D2-R11 junction forms the envelope output, and is fed via 1.4MHz rejector circuit L2-C10 and a second-order low-pass active filter (see Appendix 1) to output stage TR7.

2.1.2 Product Detectors

IC2 and IC3 are each double balanced modulators which function similarly to ring modulators but without using transformers. The signal input is applied to pin 7 and the local oscillator input is applied to pin 3. Two in-phase outputs are produced, one from pin 5 and one from pin 6. The pin 6 output is via an open-emitter stage, and uses a 1k ohm resistor between pin 6 and 0V as emitter load. A capacitor connected between pin 5 and 0V provides a degree of high-frequency roll-off. Internal decoupling is provided by capacity between pin 2 and 0V. Each product detector output is taken via an amplifier stage and level presetting control, and applied to a second-order low-pass active filter (see Appendix 1). The filter outputs are fed to the transfer gate switching described in paragraph 2.3.2. As the i.f. inputs are 1.4MHz, and the local oscillator frequency is 1.4MHz plus an offset determined in Module 6, the outputs are at offset frequency.

2.1.3 100kHz Mixer and Output Circuit

The 100kHz mixer circuit of IC1 is identical with that of IC2 and IC3, except that local oscillator frequency is 1.5MHz. Output frequency is therefore 100kHz, selected by a passive band-pass filter circuit. The filtered 100kHz output is amplified by TR11, 12, 13, and 15 to produce two unbalanced 50 ohm outputs, on SKG and SKF.

2.2 Switching Logic

The switching logic controls the signal input switching to IC1, and the output switching between the three detectors and the output amplifiers.

Control is exercised by ten input lines, one (LS) from the USB/LSB MONITOR toggle switch on the front-panel and the remainder from the control logic in Module 10. The switching logic is made up from the elements contained in IC14, IC15, and IC16. The action is shown in table 1 in terms of input '1' and '0' levels necessary to produce a logic '1' level on each output line.

TABLE 1 : SWITCHING LOGIC

INPUTS	LS	$\overline{LS}$	L	L+I	$\overline{I}$	F+C+U	I+U+C+F	AM+I	AM	$\overline{M+RM}$
SYNTH. MUTE LS (MON. LSB)	0 AND 1	0 AND 1								
L (LSB)			1	1	1					
I (ISB)				1	OR		1 OR	1		
F (F)					1 OR	1 OR	1 OR			
C (CW)					1 OR	1 OR	1 OR	OR		
U (USB)					1 OR	1	1			
AM (AM)					1			1	1	
MUTE										0 AND 0
REM. MUTE										

2.3 Switching

2.3.1 Input Switching

The inputs to the envelope detector (TR2 base), and the two product detectors (IC2 and IC3 pin 7) receive i.f. input signals directly from SKA, SKB, and SKD. These three input lines are also connected via transfer gates to a common point on R85, and from this common point via transfer gate IC11D to 100kHz mixer IC1. IC11A conducts an AM+I logic output. IC11B conducts on I+U+C+F logic output. IC11C conducts on L logic output. IC11D conducts on $\overline{M+RM}$ logic output. Input connections to IC1 are therefore made as shown in table 2.

TABLE 2 : INPUT CONNECTIONS TO IC1

MODE	CONDUCTING GATES	INPUT TO IC1 FROM:
LSB	IC11C, IC11D	SKD
ISB	IC11A, IC11B, IC11D	SKA and SKB
F	IC11B, IC11D	SKB
CW	IC11B, IC11D	SKB
USB	IC11B, IC11D	SKB
AM	IC11A, IC11D	SKA
MUTE (M+RM)	not IC11D	NONE

2.3.2 Output Switching

The outputs from the envelope detector and the two product detectors are switched by transfer gates to feed four amplifiers as shown in Figure (b), wherein the transfer gates are shown as switched. Alongside each is a 'flag' indicating the operating modes in which the various gates conduct under control of the switching logic. Each transfer gate is fed by a 0.1 d.c. blocking capacitor to avoid switching clicks in the output.

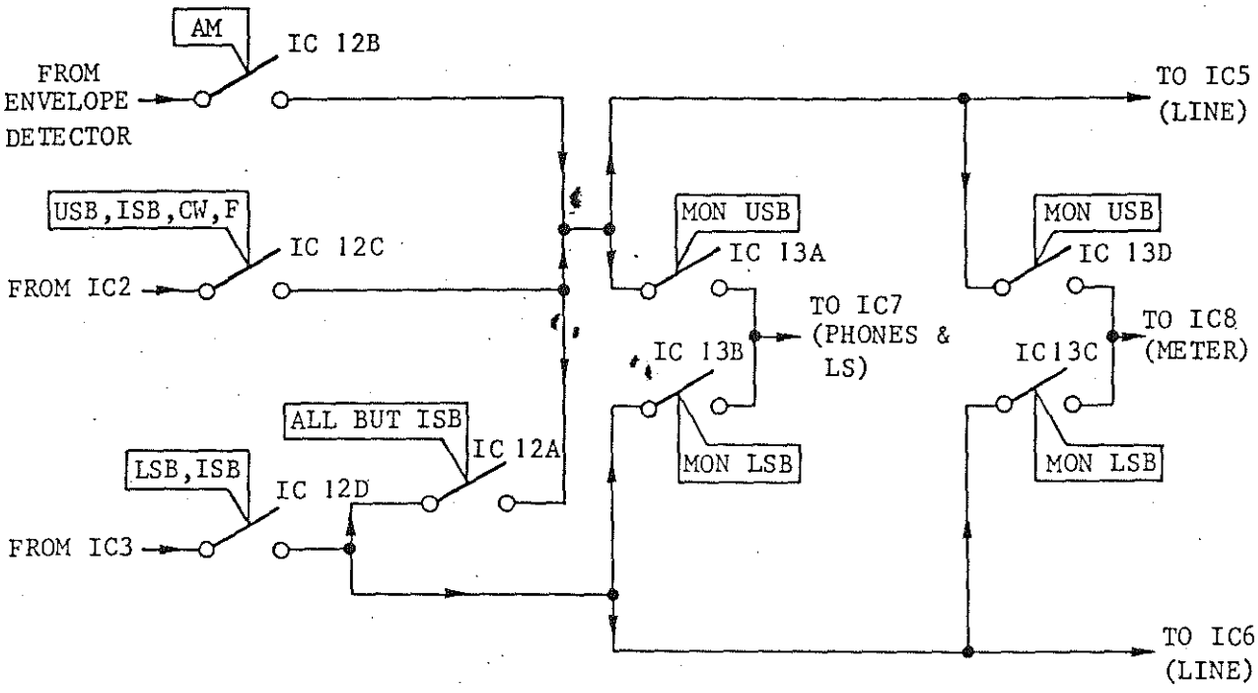


FIG. (b) OUTPUT SWITCHING ACTION

2.3.3 The signal paths produced are as follows:

(1) LSB : IC3 to all four outputs, irrespective of MONITOR switch position.

(2) ISB : IC2 to IC5, and IC3 to IC6. Both IC7 and IC8 inputs controlled by MONITOR switch position.

(3) F : IC2 to all four outputs, irrespective of MONITOR switch position.

(4) CW : exactly as (3).

(5) USB : exactly as (3).

(6) AM : Envelope detector to all four outputs, irrespective of MONITOR switch position.

2.4 Output Amplifiers

2.4.1 Phones and Speaker Output

The common output from transfer gates IC13A and IC13B is applied via emitter-follower TR16 to volume control stage IC4. The volume control integrated circuit consists of a differential amplifier fed by a current source. The current source is controlled by the input signal applied to

pin 2, while the d.c. volume-controlling level is applied to pin 1. The output from pin 6 is therefore of whatever waveform is applied to pin 2, and controlled in amplitude by the d.c. level applied to pin 1.

2.4.2 The output from pin 6 of IC4 is capacitively coupled to pin 8 of IC power amplifier IC7. Pin 8 is the non-inverting input of the amplifier. The inverting input on pin 6 is internally connected to the output (pin 12) by a feedback resistor. Gain is therefore controlled by the values of C65 and R63, the amplifier being connected as a voltage follower. A 2 Watt output is produced in this application. C67 aids ripple rejection as part of the internal decoupling circuit. The CR circuit between pin 5, 12, and 0V produces gain/frequency compensation. Pin 4 is a 'bootstrap' connection.

2.4.3 Line Amplifiers

Both line amplifiers (IC5 and IC6) are identical. IC5 is fed via emitter-follower TR17 from the junction of transfer gates IC12A, IC12B and IC12C. IC6 is fed via emitter-follower TR18 from the junction of transfer gates IC12A and IC12D. In each IC, signal input is applied to pin 5, and output is taken from pin 1: the amplifier operates in class AB, producing a maximum output of 10mW. Pin 6 is an unused input, grounded via 1.5n. The capacitors between pins 3 and 4 and ground determine frequency response, in conjunction with the series CR circuit from pin 1 to ground. Gain is set by the voltage applied to pin 8 from a pre-set gain control potentiometer.

2.4.4 Meter Amplifier

Meter amplifier IC8 is an integrated-circuit operational amplifier, and is fed directly from the junction of transfer gates IC13C and IC13D. In conjunction with TR14 it acts as a peak detector, producing a d.c. output level proportional to the amplitude of the input signal applied to IC8 pin 3. The device is essentially a voltage follower of unity gain, referred to +6V. The rectification occurs in TR14. Input swings falling below +6V produce collector current in TR14: input swings rising above +6V do not, as TR14 base is returned via R66 to +6V.

2.5 Muting

Three muting inputs are applied to Module 5. The LINE MUTE input is applied to pin 7 of both IC5 and IC6: when set to '0' level, both amplifiers produce no output, i.e. both LINE OUTPUTS are controlled by the LINE MUTE input. If the SYNTHESISER MUTE input level becomes '1', the LS and $\overline{LS}$ outputs from the switching logic become '0'. Transfer gates IC13A, B, C, and D become non-conducting, removing inputs from IC4 and IC8; i.e. LOUDSPEAKER, HEADPHONES, and AF METER outputs are controlled by the SYNTHESISER MUTE input. If either the MUTE or REMOTE MUTE input level becomes '1', the $\overline{M+RM}$ output from the switching logic becomes '0'. Transfer gate IC11D becomes non-conducting, removing the input from IC1; i.e.the 100kHz IF OUTPUT is controlled by the MUTE and REMOTE MUTE inputs.

APPENDIX 1 - ACTIVE FILTERS

Active filters consist of a number of resistive and capacitive passive elements working in conjunction with an amplifier. The circuit originated in the work of Sallen and Key, first published in 1954. The usual circuit has a second-order high-pass or low-pass characteristic; input impedance is high, and output impedance is low.

Figure (c) shows a simple first-order low-pass RC filter followed by a non-inverting unity gain buffer stage. The characteristic is asymptotic to 'A' and 'B' Frequency fc is a function of the values of R1 and C1. The output level at fc is 3dB below input level.

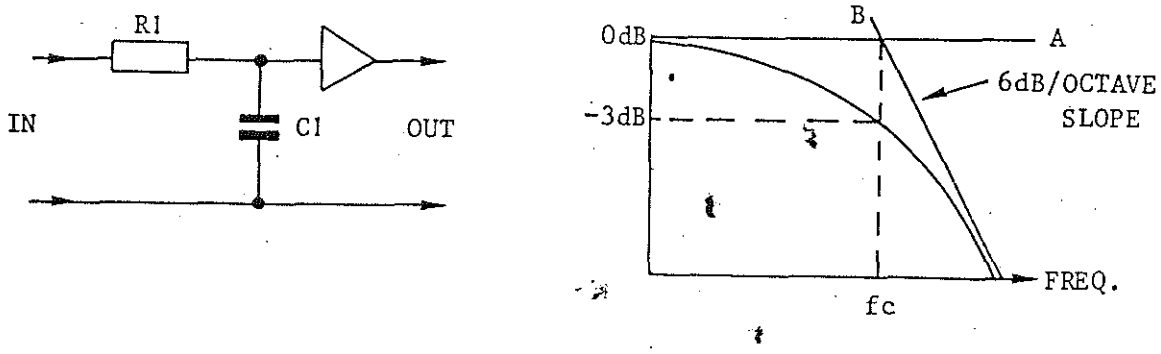


FIG (c) SIMPLE 1ST-ORDER LOW-PASS FILTER

If R1 in Figure (c) is split into two, and a further capacitor C2 is connected between the buffer output and the junction of the two parts of R1, then we have the second-order active filter circuit shown in Figure (d). Theoretically, the amplifier should have infinite input impedance and zero output impedance. The feedback introduced by C2 produces a characteristic which is asymptotic to 0dB and to a line of 12dB/octave slope. The shape of the curve (especially at frequencies near fc) is governed by the Q of the circuit, which can by any desired value up to about 1000. Typical characteristics are shown in Figure (d). A high-pass filter is produced by interchanging the positions of the resistive and capacitive elements in Figure (d).

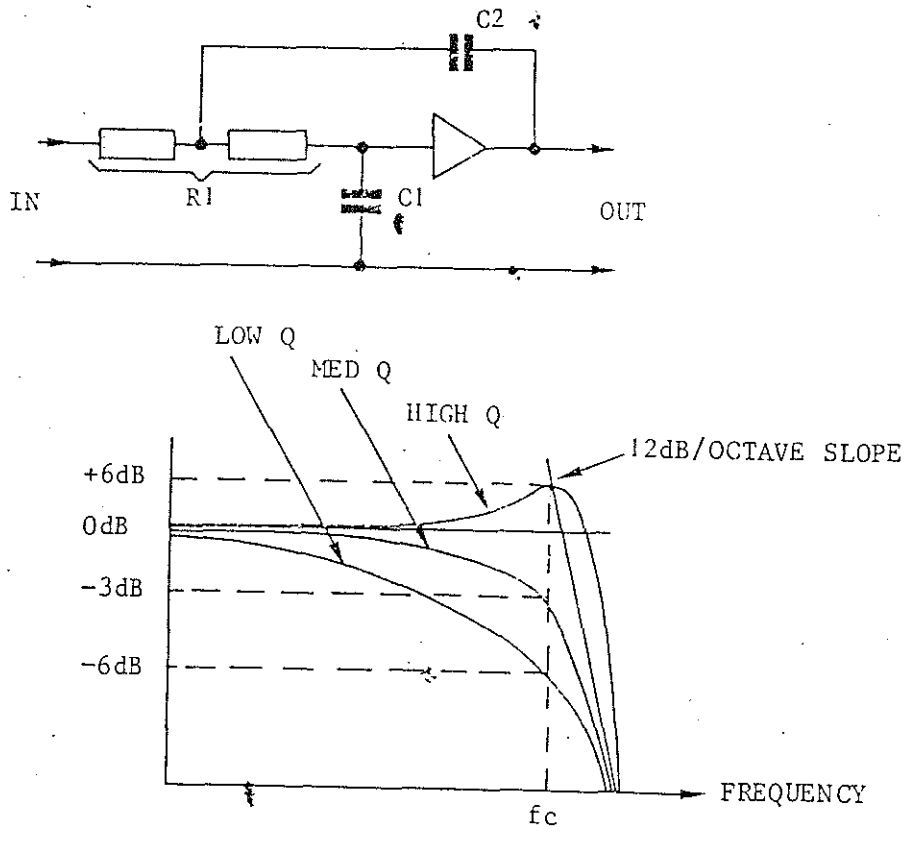


FIG (d) 2ND-ORDER LOW-PASS ACTIVE FILTER

A further reference on the subject is 'Active Filters' (Girley and Good), Wireless World, January 1970.

3. - TEST DATA

3.1 General

The procedure outlined in the following paragraphs forms a complete test procedure and need not be used to locate individual faults.

3.2 Test Equipment

The following items of test equipment are required:

Signal generator 1, 1.4MHz, 10mV r.m.s. output into 50 ohms. Capable of Amplitude modulation.

Signal Generator 2, 1.5MHz, 100mV output.

Oscilloscope.

Avometer.

50 ohm load (2 off) 50 ohm, 0.25W resistors mounted across meeting plugs for module sockets.

Distortion Factor Meter, type Hewlett Packard 8640B.

1k linear Potentiometer, 250 ohm 0.25 watt resistor for AUDIO VOLUME CONTROL.

3.3 Power Supplies

Separate +15V and +9V DC power supplies are required.

3.4 Alignment and Functional Tests

3.4.1 Connect the +15V supply to edge-pin 22, +9V supply to edge-pin 20 and 0V to edge-pin 2. Check the current consumption of the supplies as follows:

+15V : 200 $\pm$ 30mA
+9V : 80 $\pm$ 20mA

Using the Avometer check the d.c. voltage level at IC10 pin 2 (12 $\pm$ 0.6V) and at IC9 pin 2 (6 $\pm$ 0.3V).

3.4.2 100kHz Line Output

Select the 'AM' mode by applying a logic '1' to edge-pin 11, and connect the 1k potentiometer and 250 ohm resistor to the +15V supply (pin 22) to give a 0 to 12V variable supply to edge-pin 4 (Audio volume control). Set the volume control to minimum. Connect the signal generator set to 1.5MHz 100mV output, to SKTE. Connect signal generator (1) set to 1.4MHz 10mV output, to SKTA. Connect the two 50 ohm load resistors to SKT's F and G and the oscilloscope across pins 12 and 11 (SKTF). Adjust R42 to give a 300mV peak to peak 100kHz signal on the oscilloscope and check that the waveform is sinusoidal. Connect the oscilloscope across pins 13 and 14 (14 to 0V) SKTG and check that the signal displayed is 300 $\pm$ 30mV

peak-to-peak, sinusoidal. Select in turn modes CW, USB, LSB, LSB and F by applying a logic 1 to the appropriate edge-pins. A 100kHz signal should be present on ISB and absent in all other modes. Select AM mode and check that a waveform is present. Set, in turn, 'MUTE' and 'REMOTE MUTE' (logic 1 on pins 12 and 13) to the 'ON' position and check that the signal disappears in both cases. Reset both MUTES to the 'OFF' position. Connect the signal generator output to SKTB. Select each mode in turn and check the waveform is present on modes CW, USB and F only. Connect the signal generator output to SKTD. Select each mode in turn and check that the waveform is present in mode 'LSB' only.

3.4.3 Envelope Detector

Select 'AM' mode by applying a logic '1' to edge-pin 11, and connect the Distortion Factor Meter (DFM), set to 600 ohms, to line output 1, pins S and T. Set the signal generator to 1.4MHz 10mV r.m.s., 30% modulation at 1kHz and connect to SKTA. Set the 'AUDIO VOLUME' control fully clockwise. Set R68 and R69 fully clockwise and adjust R28 to give +10dBm on line output 1. Connect the DFM to line output 2, pins E and D and ensure that the output is +10dBm $\pm$ 0.5dB. Select all modes in turn (logic '1' on appropriate pins) and ensure that a line output is present on 'AM' mode only. Readjust R68 and R69 to give their respective lines of 0 $\pm$ 0.2dBm. Connect a microammeter to edge-pin 7 (AF METER) and check that the reading is 27 to 34uA.

3.4.4 CW/USB Product Detector

Set the signal generator to 1.39MHz 10mV r.m.s. (no modulation) and connect to SKTB. Set the second signal generator to 1.4MHz 100mV r.m.s. (reinserted carrier) and connect the SKTC. Select the CW mode by applying a logic '1' to edge-pin 17. Connect the DFM set to 600 ohms to line output 1 pins S and T and the oscilloscope between edge-pin 5 and 0V. Adjust R22 to give a reading on the DFM of 0 $\pm$ 2dBm. Measure the 1kHz waveform amplitude on the oscilloscope and check that the amplitude is not less than 7V peak to peak and that the waveform is sinusoidal. Select all modes in turn (logic '1' on appropriate pins) and ensure the oscilloscope waveform is present only on CW, F, USB and ISB. Set the volume control for 7V peak to peak, select ISB and ensure that the waveform amplitude is 7V $\pm$ 0.5V peak to peak.

3.4.5 LSB Product Detector

Connect signal generator to SKTD(LSB INPUT) and select mode LSB by applying a logic '1' (+12V) to edge-pin 15. Connect the DFM to line output 2 pins E and D and adjust R24 to give a reading on the DFM of 0 $\pm$ 0.2dBm. Select all modes in turn and check that the oscilloscope waveform is only present on LSB and ISB.

3.4.6 Audio Power Stage

Select mode ISB (logic '1' to edge-pin 14) and connect the oscilloscope between edge connector 5 and 0V. Adjust the 1k audio volume control, connected to edge-pin 4, for a reading on the oscilloscope of 7V peak to peak. Connect the oscilloscope between edge connector 8 and 0V and check that the waveform displayed is 5.65V $\pm$ 0.5V peak to peak. Reconnect the oscilloscope between pin 5 and 0V. Set the 1k audio volume control fully counterclockwise and check for a reading of between 20 and 50mV peak to peak. Adjust R55 as necessary to obtain this reading. Set the audio

volume control to approximately half way. Select USB mode (logic '1' on edge-pin 16) and check that the waveform disappears. Connect a signal generator to SKTB (CW, F, USB INPUT) and check that the waveform re-appears. Select LSB mode and check that the waveform disappears.

3.5 The modules should be inspected to ensure that no damage has been caused during testing.

4. COMPONENT LISTS.

Main Assembly (630/1/32985)
Panel Electronic Circuit (419/1/18015)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Panel Printed Circuit	Plessey	419/2/18016
-	Socket Semi-Conductor	Texas 8L DIL C930802	508/4/22096/001
-	Socket Semi-Conductor	Texas 14L DILC931402	508/4/22096/002
	Lead Assembly	Plessey	400/4/20672/010
C10	Capacitor 82pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/024
C23,55,56, 68	Capacitor 100pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/011
C54,57,71	Capacitor 1nF ± 5% 400V	Siemens B32560	435/4/90317/023
C22,32,33, 46,48	Capacitor 1.5nF ± 5% 400V	Siemens B32560	435/4/90317/024
C51,52	Capacitor 2.2nF ± 5% 400V	Siemens B32560	435/4/90317/025
C19,30,31	Capacitor 4.7nF ± 5% 400V	Siemens B32560	435/4/90317/027
C24,25,72	Capacitor 10nF ± 5% 400V	Siemens B32560	435/4/90317/029
C1,2,4-8, 11-17,26, 37-39,44, 45,62,66, 77,80,81, 84,85,87-92	Capacitor 100nF ± 5% 250V	Siemens B32560	435/4/90317/014
C63	Capacitor 220nF ± 5% 100V	Siemens B32560	435/4/90317/017
C9,34	Capacitor 330nF ± 20% 35V	ITT TAG	402/4/57057/002
C76	Capacitor 560pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/028
C27-29,41, 43,53,58, 75	Capacitor 10uF ± 20% 16V	ITT TAG	402/4/57057/008
C82	Capacitor 22uF ± 20% 16V	ITT TAG	402/4/57057/009
C35,36	Capacitor 3900pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/080
C18,20,21, 61,83	Capacitor 47uF ± 20% 16V	ITT TAG	402/4/57057/011
C47,49,62, 69	Capacitor 100uF ± 20% 16V	ITT TAP	402/4/55746/019
C64	Capacitor 68uF ± 20% 25V	ITT TAP	402/4/55747/018
C70	Capacitor 15nF ± 5% 400V	Siemens B32560	435/4/90317/030
C59,60,65, 73,74	Capacitor 220uF ± 20% 16V	ITT TAP	402/4/55746/021
L1	Inductor 22uH ± 10%	Sigma SC10	406/4/31749/002
L2	Inductor 150uH ± 10%	Sigma SC10	406/4/31749/003
IC14	Integrated Circuit	Motorola MC14001CP	445/4/02383/001
IC11,12,13	Integrated Circuit	Motorola MC14006CP	445/4/02383/066
IC15	Integrated Circuit	Motorola MC14071CP	445/4/02383/071
IC16	Integrated Circuit	Motorola MC14075CP	445/4/02383/075
IC9	Integrated Circuit	Motorola MC7806CT	445/9/03051/002
IC10	Integrated Circuit	Motorola MC7812CT	445/4/03051/004
IC5,6	Integrated Circuit	Plessey SL630C	445/4/02366
IC1,2,3	Integrated Circuit	Plessey SL640C	445/4/02386
IC4	Integrated Circuit	RCA CA3053	445/4/03058
IC8	Integrated Circuit	RCA CA3130E	445/4/03049/002
IC7	Integrated Circuit	TBA 8109	445/4/03057
R92,93	Resistor 180R ± 2%	Electrosil TR4	403/4/05522/180
R52,53,65	Resistor 10R ± 2%	Electrosil TR4	403/4/05521/100

Panel Electronic Circuit (Cont'd)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
R57,58	Resistor 15R ± 2%	Electrosil TR4	403/4/05521/150
R4,46,47	Resistor 47R ± 2%	Electrosil TR4	403/4/05521/470
R12,13	Resistor 56R ± 2%	Electrosil TR4	403/4/05521/560
R67	Resistor 82R ± 2%	Electrosil TR4	403/4/05521/820
R6,59,63,64	Resistor 100R ± 2%	Electrosil TR4	403/4/05522/100
R8	Resistor 270R ± 2%	Electrosil TR4	403/4/05522/270
R9,21,23	Resistor 330R ± 2%	Electrosil TR4	403/4/05522/330
R44,45	Resistor 390R ± 2%	Electrosil TR4	403/4/05522/390
R10,11	Resistor 470R ± 2%	Electrosil TR4	403/4/05522/470
R60	Resistor 820R ± 2%	Electrosil TR4	403/4/05522/820
R1,3,18-20, 25,26,36, 37,39,77-84,91,94, 95	Resistor 1k ± 2%	Electrosil TR4	403/4/05523/100
R56	Resistor 1.2k ± 2%	Electrosil TR4	403/4/05523/120
R88,89	Resistor 1.5k ± 2%	Electrosil TR4	403/4/05523/150
R7	Resistor 1.8k ± 2%	Electrosil TR4	403/4/05523/180
R5	Resistor 3.3k ± 2%	Electrosil TR4	403/4/05523/330
R43,51,90	Resistor 4.7k ± 2%	Electrosil TR4	403/4/05523/470
R17,40,41, 48,49	Resistor 5.6k ± 2%	Electrosil TR4	403/4/05523/560
R15,16,31-34	Resistor 15k ± 2%	Electrosil TR4	403/4/05524/150
R14,29,30	Resistor 18k ± 2%	Electrosil TR4	403/4/05524/180
R62	Resistor 22k ± 2%	Electrosil TR4	403/4/05524/220
R50	Resistor 33k ± 2%	Electrosil TR4	403/4/05524/330
R2,61,68-76,85,96-98	Resistor 100k ± 2%	Electrosil TR4	403/4/05525/100
R54	Resistor 120R ± 2%	Electrosil TR4	403/4/05522/120
R27	Resistor 560R ± 2%	Electrosil TR4	403/4/05522/560
R66	Resistor 3.9k ± 2%	Electrosil TR4	403/4/05523/390
R22,24,28, 42	Resistor Variable 1k ± 20%	Allen Bradley Type 90H	404/9/05047/003
R55	Resistor Variable 100k ± 20%	Allen Bradley Type 90H	404/9/05047/009
D1,2	Diode	Hewlett Packard HP5082-2800	415/9/98532
D3,4	Diode	Mullard OA90	415/9/98090
D5	Diode	Texas 1N4148	415/4/05720
T1,2	Transformer		406/9/29690
TR2,3,7,8, 9,11,13,15	Transistor	Mullard BC107	417/4/01777
TR4,16-18	Transistor	Mullard BC109	417/4/01776
TR5,6,12,14	Transistor	Mullard BC177	417/4/01859

Connector Assembly (720/1/20093/002)

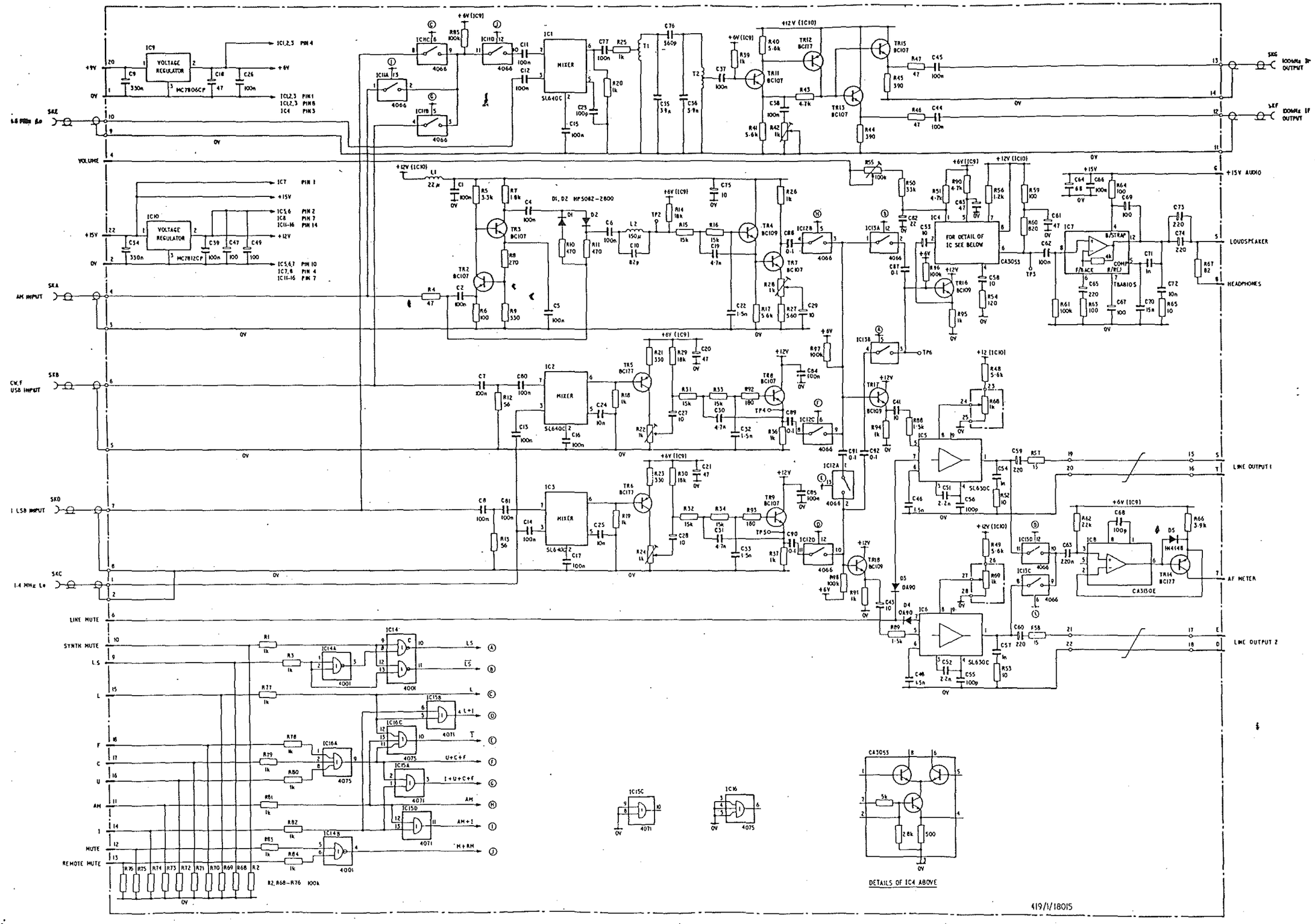
Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
SKC	Socket Electrical R.F.	Belling Lee L1465/K/BS	508/4/22059
-	Cable R.F.	Suhner R.G. 174/U 150mm	998/4/70537/001

Connector Assembly (720/1/20093/003)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
SKA,B, D,E	Socket Electrical R.F.	Belling Lee L1465/K/BS	508/4/22059
-	Cable R.F.	Suhner R.G. 174/U 170mm	998/4/70537/001

Connector Assembly (702/1/20093/005)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
SKF,G	Socket Electrical R.F.	Belling Lee L1465/K/BS	508/4/22059
-	Cable R.F.	Suhner R.G. 174/U 210mm	998/4/70537/001
R68,69	Resistor Variable 1k ± 20%	Plessey Type L Mk5	404/4/07647/001



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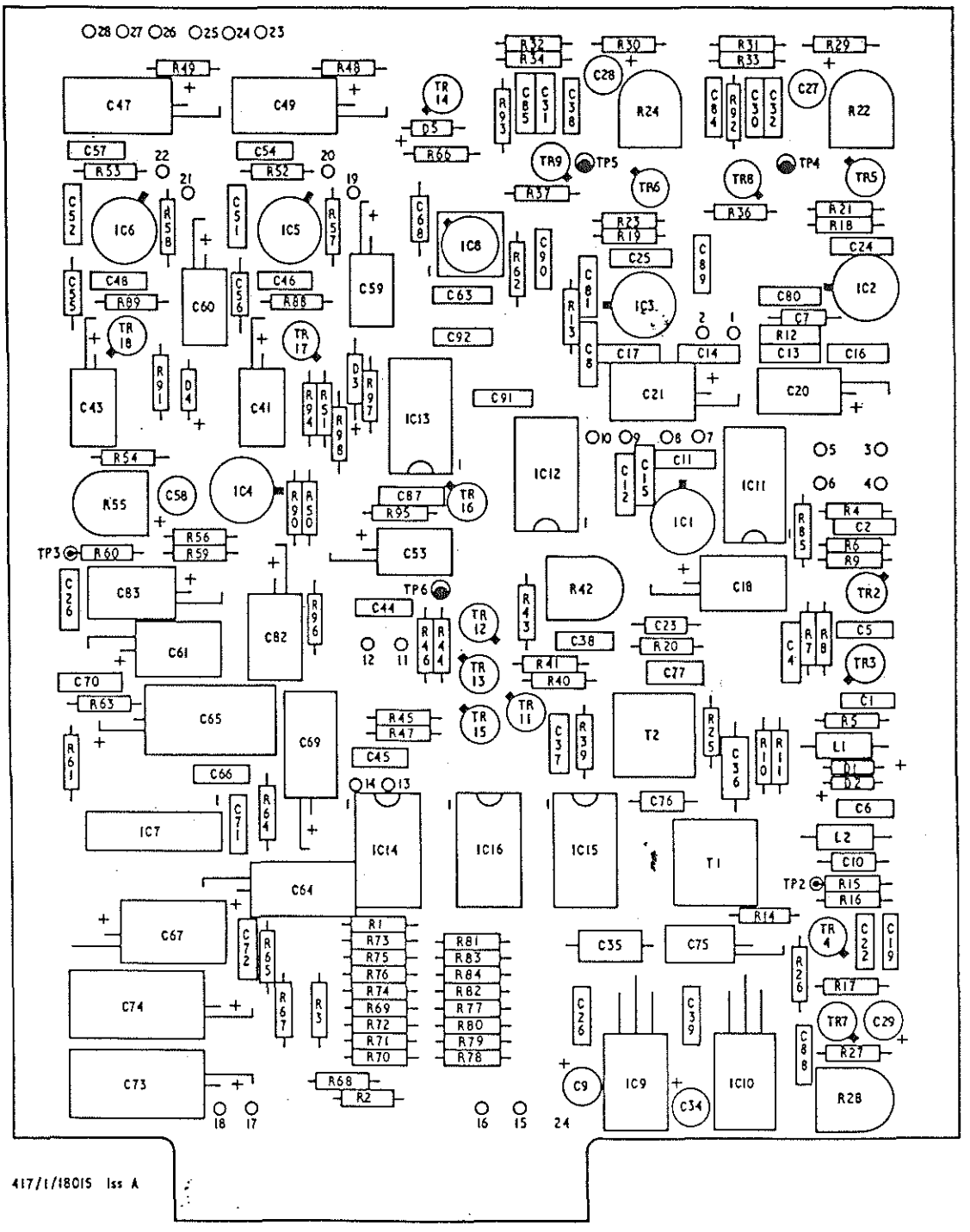
MODULE 5 : DETECTORS AND OUTPUT AMPLIFIERS CIRCUIT DIAGRAM

FIG 1



MODULE 5 PANEL- COMPONENT LAYOUT

FIG 2

CHAPTER 6

MODULE 6 BFO

CONTENTS

TABLES

ILLUSTRATIONS

APPENDICES

INTEGRATED CIRCUIT DEFINITIONS

This information forms a supplement to the circuit diagrams in respect of complex integrated circuits which are shown diagrammatically by a rectangular outline only.

MC 14518

Dual BCD counter

CL	BNC	R	ACTION
	1	R	) Count
0		0	) incremented
	X	0	)
X		0	) no
	0	0	) change
1		0	)
X	X	1	All outputs '0'

MC 14046

A Phase-lock loop controlled VCO. The centre frequency is set by value of R to pin 12 and C across pins 6 and 7. Input signal is applied to SIG IN, and frequency standard is applied to COMP IN. Oscillator output is obtained on VCO OUT. The device is made operational by applying a '0' level to the INH input.

1. BASIC DESCRIPTION

1.1 Module 6 is used in all PR2250 series receivers. It contains the oscillators and associated control circuits which produce the 1.5MHz and 1.4MHz inputs to the detector circuits in Module 5. The essentials of Module 6 can be seen in Figure (a).

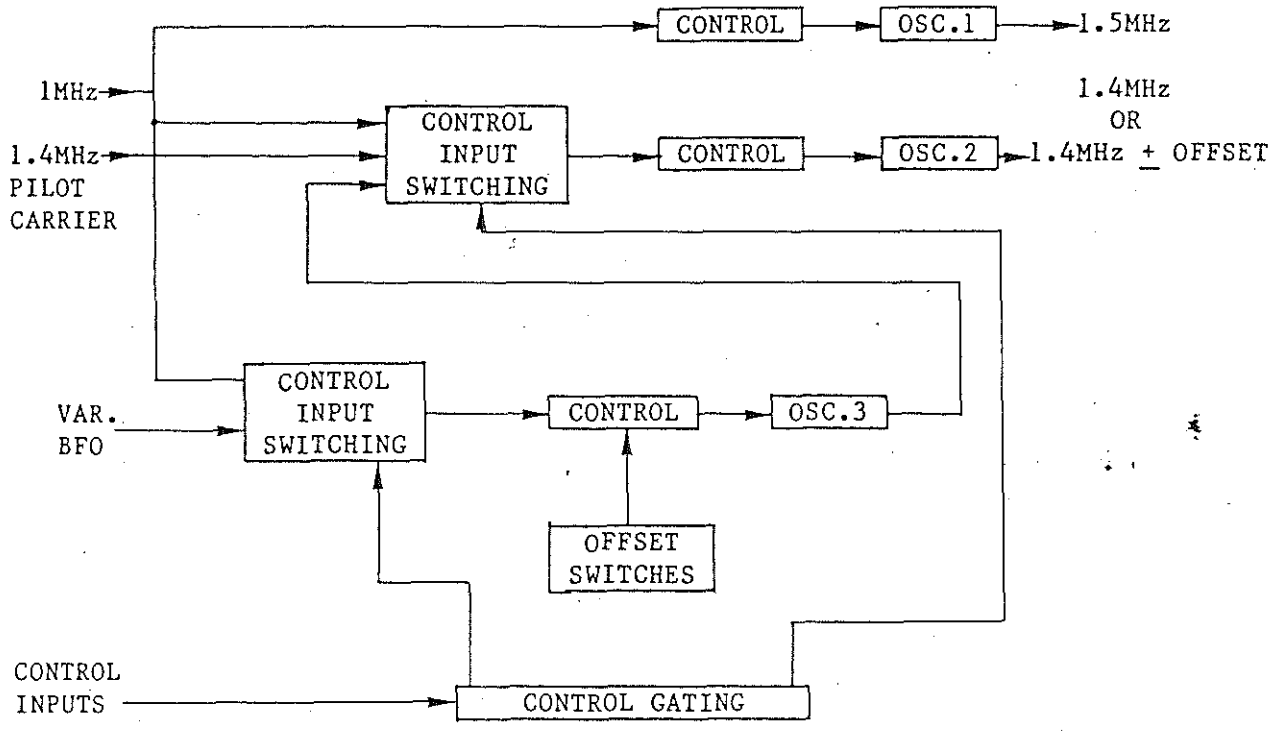


FIG (a) MODULE 6 BASIC BLOCK DIAGRAM

1.2 Oscillator 1 and Oscillator 2 provide the two outputs from Module 6. Oscillator 1 is permanently phase-locked to the 1MHz reference input. Oscillator 2 can be phase-locked to the 1MHz input, the 1.4MHz carrier input, or the output from Oscillator 3. Oscillator 3 can be locked to the 1MHz reference input (in which case its frequency can be set in 100Hz steps by the OFFSET switches) or controlled directly by the variable d.c. BFO input from the front-panel BFO control.

2. FUNCTIONAL DESCRIPTION

2.1 General

This description is intended to be read in conjunction with the Functional Block Diagram shown in Figure 1. Component references given in Figure 1 allow it to be related to the full circuit diagram used in the circuit description.

2.2 Oscillator 1

Oscillator 1 is controlled in frequency by the output from a phase detector receiving two 50kHz inputs. One is the oscillator output taken via a division ratio of 30 and the other is the 1MHz reference input taken via a division ratio of 20. The 1.5MHz output from Oscillator 1 is therefore phase-locked to the 1MHz reference input.

2.3 Oscillator 2

Oscillator 2 is controlled in frequency by a selected phase detector, either IC11 or IC13. When controlled by IC13, it is phase-locked to the 1.4MHz CARRIER input. When controlled by IC11, the output from Oscillator 2 is fed back at 100kHz via mixer IC17: control is exercised either by 1MHz reference input via a division ratio of 10 or by the output from Oscillator 3.

2.4 Oscillator 3

2.4.1 Oscillator 3 is controlled in frequency either by the output from phase detector IC5 or by the variable d.c. BFO control input. When controlled by the output from IC5, it is phase-locked to the 1MHz reference input taken via a division ratio of 10,000. The oscillator output is applied to the phase detector via a division ratio which can be set by switches. As the reference input (1MHz - 10,000) is 100Hz, Oscillator 3 will lock at whatever frequency produces a 100Hz output from the variable (-n) divider. The offset frequency produced in this way can be set in 100Hz steps above and below the nominal 100kHz frequency of Oscillator 3. When directly controlled by the BFO control input, Oscillator 3 does not form part of a phase-lock loop.

2.4.2 To set the offset switches inside the module, subtract the required offset in hundreds of Hz from 1000, and convert the answer to binary. Set the switches to this binary number, the ON position of a switch representing '1'.

Example: Required offset is 1500Hz

1000 - 15 = 985
985 = 1111011001

this has only ten digits, so add '0's to bring to 12 digits.

001111011001

The binary number is 12 digits, LSB on the right. The switches have toggles which are visible through their top hinged covers when ON.

Switch setting are given in Table 1.

TABLE 1 : SWITCH SETTINGS

DIGIT	SWITCH	BINARY VALUE	EXAMPLE 1500Hz
12 LSB	(1	1	1
11	S10 (3	2	0
10	(4	4	0
9	(2	8	1
8	(6	16	1
7	(7	32	0
6	(8	64	1
5	S9 (5	128	1
4	(2	256	1
3	(3	512	1
2	(4	1024	0
1	(1	2048	0

2.3 Oscillator 2

Oscillator 2 is controlled in frequency by a selected phase detector, either IC11 or IC13. When controlled by IC13, it is phase-locked to the 1.4MHz CARRIER input. When controlled by IC11, the output from Oscillator 2 is fed back at 100kHz via mixer IC17: control is exercised either by 1MHz reference input via a division ratio of 10 or by the output from Oscillator 3.

2.4 Oscillator 3

2.4.1 Oscillator 3 is controlled in frequency either by the output from phase detector IC5 or by the variable d.c. BFO control input. When controlled by the output from IC5, it phase-locked to the 1MHz reference input taken via a division ratio of 10,000. The oscillator output is applied to the phase detector via a division ratio which can be set by switches. As the reference input (1MHz - 10,000) is 100Hz, Oscillator 3 will lock at whatever frequency produces a 100Hz output from the variable (-n) divider. The offset frequency produced in this way can be set in 100Hz steps above and below the nominal 100kHz frequency of Oscillator 3. When directly controlled by the BFO control input, Oscillator 3 does not form part of a phase-lock loop.

2.4.2 To set the offset switches inside the module, subtract the required offset in hundreds of Hz from 1000, and convert the answer to binary. Set the switches to this binary number, the ON position of a switch representing '1'.

Example: Required offset is 1500Hz

1000 - 15 = 985
985 = 1111011001

this has only ten digits, so add '0's to bring to 12 digits.

001111011001

The binary number is 12 digits, LSB on the right. The switches have toggles which are visible through their top hinged covers when ON.

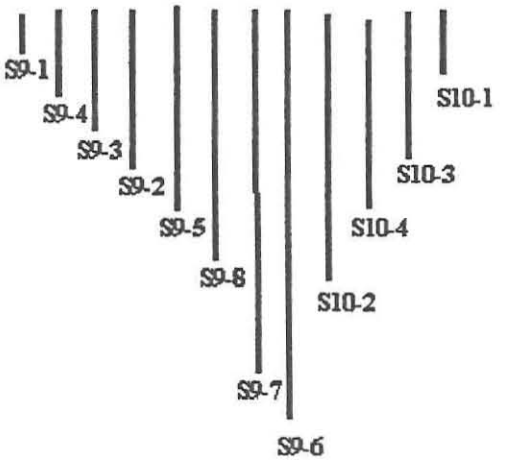
Switch setting are given in Table 1.

TABLE 1 : SWITCH SETTINGS

DIGIT	SWITCH	BINARY VALUE	EXAMPLE 1500Hz
12 LSB	(1	1	1
11	S10 (3	2	0
10	(4	4	0
9	(2	8	1
8	(6	16	1
7	(7	32	0
6	(8	64	1
5	S9 (5	128	1
4	(2	256	1
3	(3	512	1
2	(4	1024	0
1	(1	2048	0

COMBINAZIONI
PER
FSR

001111010111



1500 Hz

1700 Hz

31/05/00

2.5 Switching

The switching which sets up the desired phase-lock loop arrangement is controlled by front-panel settings which produce logic level control inputs to Module 6. These control inputs operate a number of transfer gates and one switching transistor according to the table given in Figure 1.

2.6 Meter Outputs

The output from phase detector IC13 is taken to provide two monitor ZERO BEAT outputs, both of which indicate phase-locking of Oscillator 2 to the 1.4MHz CARRIER input.

3. CIRCUIT DESCRIPTION

3.1 Phase-Lock Loops

All three oscillators in Module 6 are controlled in frequency by phase-lock loops employing 4046 Integrated Circuits as phase detectors controlling oscillator frequency by means of varactor diodes. The capacity of the varactor diodes decreases as control voltage increases, and increases as control voltage decreases: oscillator frequency therefore increases with an increase in control voltage, and decreases with a decrease in control voltage. The control voltage is produced at the output of the 4046 phase-detector.

3.2 Only part of the circuitry contained in a 4046 is used in this application. Two input signals of equal frequency are applied, one to pin 3 and one to pin 14. If both are exactly in phase, the output from pin 13 is 'open-circuit'. If the input to pin 14 increases in frequency, positive pulses from pin 13 rise. If the input to pin 3 increases in frequency, the positive pulses from pin 13 fall.

3.3 To produce a phase-lock loop, the 4046 IC is connected as shown in Figure (b). Divider circuits may be used in either or both 4046 input lines, depending on the frequencies of the reference input and the oscillator.

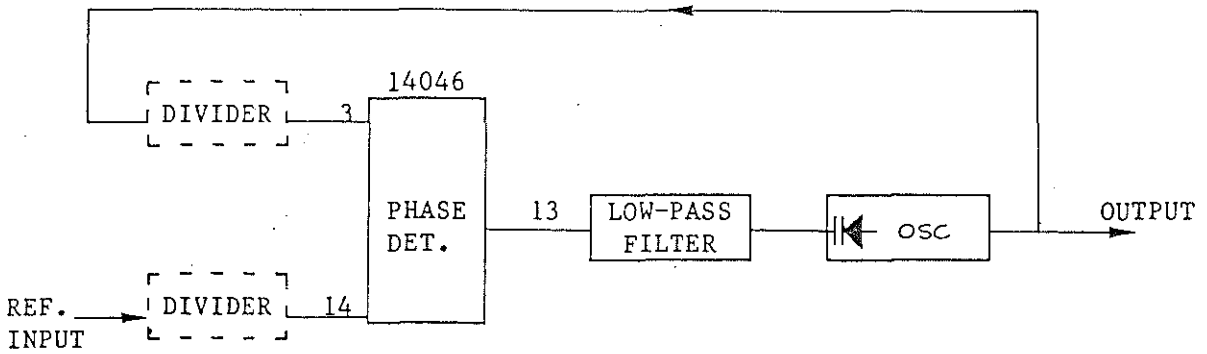


FIG (b) BASIC 14046 PHASE-LOCK LOOP

3.4 If the oscillator frequency increases relative to the reference frequency, the voltage at pin 13 of the 4046 falls; this decreases oscillator frequency. Similarly, if oscillator frequency decreases, the voltage at pin 13 rises to increase frequency. The oscillator frequency is therefore locked to the reference input frequency. If a variable reference frequency is applied, the oscillator will follow its variations.

3.5 Oscillator 1

Oscillator 1 is of the basic form shown in Figure (c); frequency control is exercised by varactor diode D5. The oscillator output is taken from TR8 base via paraphase amplifier TR9 to two output stages, TR10 and TR11. Nominal frequency of oscillation is 1.5MHz, the exact frequency being determined by the positive potential at pin 13 of IC14 applied to D5 via low-pass filter R66, R67, C32. R68 provides a high series impedance between the filter and the oscillator tuned circuit.

3.6 The reference input to pin 14 of IC14 is derived from the 1MHz INPUT applied to SKF. The output from buffer stage TR14 is divided by ten in IC19 (pin 1 input, pin 6 output)and further divided by two in IC16B, producing a 50kHz square-wave input to IC14 pin 14. The 1.5MHz output from TR11 collector is divided by two in IC16A and further divided by fifteen in IC15 pin 6 input, pin 1 output, producing a 50kHz square-wave input to IC14 pin 3. Both inputs to IC14 are in phase when the loop is locked: the oscillator output frequency is then 1.5000MHz.

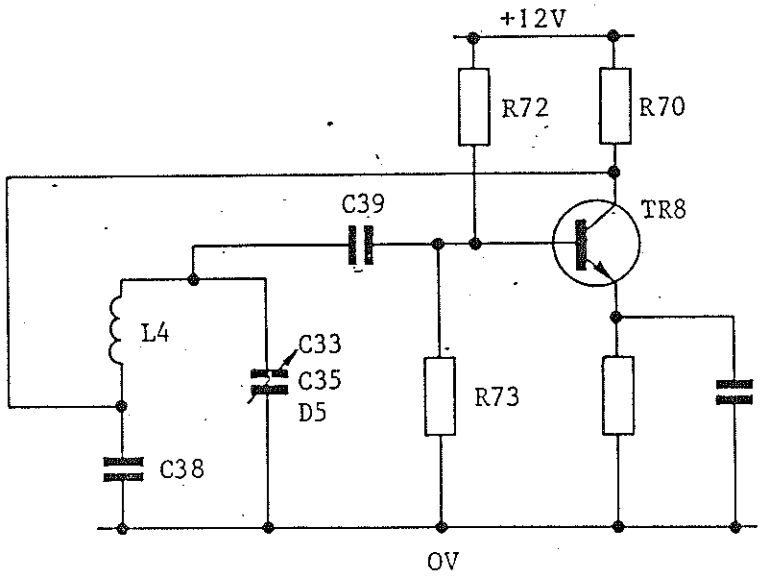


FIG (c) OSCILLATOR 1

3.7 Oscillator 2

Oscillator 2 is the same circuit as that of Oscillator 1; TR4 is the oscillator, controlled by D4. TR5, 6, and 7 are the amplifier stages. The output from TR6 collector to SKA can be switched off or on as requisite by the logic level applied to pin 13 of transfer gate IC12A, controlling transfer gate IC12B connected between TR6 collector and SKA. The nominal frequency of oscillation of Oscillator 2 is 1.4MHz, the exact frequency being determined by the positive potential at the junction of pin 9 of IC12C with pin 10 of IC12D. IC12C, when conducting, connects D4 to the output from phase detector IC13: IC12D, when conducting, connects D4 to the output from phase detector IC11. Oscillator 2 can therefore be controlled by either IC11 or IC13, each of which must receive an input from Oscillator 2.

3.8 The two inputs to phase detector IC13 are pin 14 and pin 9: the output is taken from pin 8. IC13 is (in this application) similar in action to the 4046 IC described in paragraph 3.2, except that it contains a limiter on the input applied to pin 14. The output contains ripple at the input frequency, which is removed by C29.

3.9 When transfer gate IC12C is conducting, Oscillator 2 and IC13 form a phase-lock loop which is locked to the 1.4MHz CARRIER input applied to SKE. SKE is connected to IC13 pin 14, and TR7 collector is connected to IC13 pin 9. The oscillator output frequency is identical with the frequency applied to SKE (nominally 1.4MHz).

3.10 When IC12D is conducting, the oscillator is controlled by the output from IC11. The oscillator output to IC11 pin 14 is taken from TR13 collector, which is fed via TR12 from the output of mixer IC17. The two inputs to IC17 are the 1.5MHz output from TR10 in Oscillator 1, and the output of Oscillator 2 from TR6 collector. The input to IC11 pin 14 is therefore at 100kHz.

3.11 The 100kHz reference input to IC11 pin 3 is taken from the junction of IC20B pin 3 and IC20A pin 2. If IC20A is conducting, the reference input is taken from the nominal 100kHz output of Oscillator 3, at TR3 collector: under these conditions, the output frequency of Oscillator 2 is locked to the output frequency of Oscillator 3. If IC20B is conducting, the reference input is derived from the 1MHz INPUT applied to SKF. The output from buffer stage TR14 is divided by 10 in IC19 (pin 1 input, pin 6 output) to produce a 100kHz reference via IC20B to IC11 pin 3: under these conditions, the output frequency of Oscillator 2 is 1.4000MHz.

3.12 Oscillator 3

Oscillator 3 consists of TR2 and associated components, and is controlled in frequency by two varactor diodes in parallel. The output is taken via amplifier stage TR3. Nominal frequency of oscillation is 100kHz. The oscillator can be switched on or off by the level applied to TR15 base. Note that C60 is not fitted in every receiver; its presence or omission is a factory 'select on test' decision.

3.13 Frequency control is exercised either by a phase-lock loop or directly by inputs applied to edge-pins 10 and 18 (REMOTE BFO and LOCAL BFO). With IC4B conducting, a variable d.c. level applied to either of these edge-pins (with either IC20D or IC4D conducting) will directly control the frequency of Oscillator 3.

3.14 With IC4A conducting, Oscillator 3 is connected in a phase-lock loop controlled by the output from IC5. The reference input to pin 14 of IC5 is derived from the 1MHz INPUT applied to SKF. The output from buffer stage TR14 is divided by 100 in IC19 (pin 1 input - pin 6 output, then pin 10 input - pin 14 output) and further divided by 100 in IC18 (pin 2 input - pin 6 output, then pin 10 input - pin 14 output) to produce a 100Hz input to IC5 pin 14. The output from Oscillator 3 is applied to IC5 pin 3 via a variable-ratio divider formed by IC6, IC7, and IC8. This can be considered as having a nominal division ratio of 1000, variable by the settings of switch banks IC/S9A, IC/S9B, and IC/S10. Assuming the division ratio is 1000, then a 100kHz output from TR3 will be applied to IC5 pin 3 as a 100Hz input: the loop will lock. If, however, the division ratio is set to be other than 1000, the loop will lock with the oscillator frequency at whatever value produces a 100Hz output from the variable divider. The frequency of Oscillator 3 can therefore be set by IC/S9A, IC/S9B, and IC/S10 in steps of 100Hz. The three switch banks are set to a coded version of the required frequency as laid down in paragraph 2.4.2. IC/S9A sets the most significant digit, and IC/S10 sets the least significant digit.

3.15 Variable Divider

3.15.1 Basic Concept

The divider consists of three integrated-circuit devices which each receive an input number smaller than 16. These numbers are hexa-decimal, i.e., the count is in 16s. The input number 342, therefore, is (3 x 16 x 16) + (4 x 16) + 2 = 834. On application of clockpulses, each of the three devices counts down to 0 from the applied input number, and produces one output pulse: thereafter, each device produces one output pulse for every 16 applied input pulses. This action continues until a presetting input pulse is applied. The presetting input is obtained from the output of the third stage, i.e. the third stage never counts to 16. The basic form of the circuit can be seen in Fig.(d).

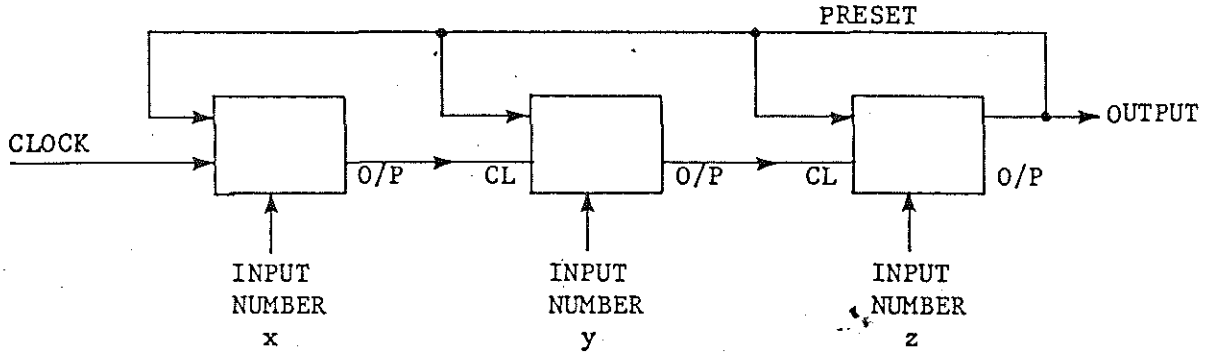


FIG (d) BASIC CIRCUIT

Note that this description covers the basic concept: the practical circuit is not connected exactly as shown in Fig.(d), but that in no way invalidates this description.

3.15.2 Consider the situation wherein the first and second stages are both counting 16, and the third stage is counting z. To produce one output pulse from the third stage, 16 x 16 x z clock pulses must be applied to the first stage (256z clock pulses).

3.15.3 Call 256z the 'basic count' of the circuit. Next, consider the situation wherein the first two stages have been preset to count down from an input number to 0. The first stage must therefore receive x clockpulses before producing an output pulse, and this output pulse will be the first clockpulse applied to the second stage. The second stage must receive y input pulses before producing an output pulse, and y input pulses to the second stage require x + 16y clockpulses to be applied to the first stage. Before the basic count of 256z commences, therefore, x + 16y clockpulses must be applied. The total number of clockpulses required to produce one output pulse from the third stage can be seen to be x + 16y + 256z. The output pulse from the third stage then presets all three stages, and the cycle repeats.

Numerical Example

Input number = 342 (x = 2, y = 4, z = 3)

Value = $(3 \times 16^2) + (4 \times 16^1) + (2 \times 16^0) = 834$

From the example given, with preset enabled an x = 2, y = 4 and z = 3, after two input clockpulses a 'carry' will be applied to the second

stage. After 16 further clockpulses, and thereafter every 16 input clockpulses, a carry will be applied to the second stage.

Similarly after four clockpulses applied to the second stage one output clockpulse will be produced, and applied to the third stage. Thereafter every sixteenth input clockpulse to the second stage will produce an output clockpulse.

The third stage requires three input pulses before it produces an output pulse. This pulse resets the circuit to the original condition set by the input numbers 342.

Hence total count is $2 + (4 \times 16) + (3 \times 16^2) = 834$

3.16 Circuit

3.16.1 Each of the three type 4526 4-bit binary programmable down-counter integrated circuits (IC6, IC7, IC8) in the variable divider has a maximum count of 16. Initially, a Preset Enable (PE) input '1' level to pin 3 presets the count start to whatever binary number is applied in 4-bit parallel form to the four Preset (P) input lines (pins 5, 11, 14, and 2). On application of clockpulses to the Clock (CL) input (pin 6), the device counts down from the preset number to 0, and thereafter counts repeatedly down from 15 to 0. A 0-1-0 output pulse is produced on the Q3 output (pin 1) on each 0 to 15 transition. If the Cascade (CF) input (pin 13) level is '1', a 0-1-0 output pulse is also produced on the '0' output (pin 12) at count zero. The count changes on positive-going clockpulse transitions.

3.16.2 IC6, IC7, and IC8 form the three stages of a counter of the form shown in Fig.(d). Terms 'x', 'y', and 'z' (ref.para.3.15) are generated by the settings of switches IC/S10, IC/S9B, and IC/S9A respectively. Presetting is initiated by the '0' output from pin 12 of IC8: this occurs on every count of 'z' in IC8, as pin 13 (CF) is connected to a permanent logic '1' (+12V). An '0' output pulse from IC8 applied to the CF input of IC7 allows IC7 to produce one '0' output pulse at the end of a 15 0 count cycle: this '0' pulse from IC7 is applied to the CF input of IC6 to produce one '0' pulse at the end of an IC6 15 0 count cycle. This "ripple-back" action occurs once at the end of each complete 'x + 16y + 256z' count cycle. The '0' output pulse from IC6 is fed to the PE inputs of all 3 ICs to initiate a new count cycle, and is also taken as the output pulse from the whole variable divider.

3.16.3 The variable divider does not start a programmed count cycle immediately on switch-on, as the Q levels of the four bistables in each IC will initially be a random combination. The first count, therefore, will start from a random set of numbers and will be meaningless. This is unimportant, as the maximum theoretical duration is 16^3 clockpulses at 10uS intervals, i.e. 41mSec.

3.17 Switching

The various transfer gates are controlled by ten input control lines. The active level is '1' in positive logic on all control lines. The action of the control is defined in Table 2.

TABLE 2 : SWITCHING CONTROL

INPUT AT LOGIC '1'	TRANSFER GATES CONDUCTING
C	IC4B, IC20A, TR15
C	IC4A, IC20A, TR15
L	) IC20B
U	) IC20B
I	) IC20B
AM	) IC20B, IC12A, IC12B
RECON	IC12C
XTAL	IC12D
REMOTE	IC20D
LOCAL	IC4D

4. TEST DATA

4.1 General

The procedure outlined in the following paragraphs forms a complete test procedure and need not be used to locate individual faults.

4.2 Test Equipment

The following items of test equipment are required:

Oscilloscope (general purpose).

1k ohm load resistors (2 of).

Signal Generator (1.4MHz carrier input signal).

Avometer.

Frequency Counter (1.5MHz max.) with 1MHz Output.

Potentiometer network shown in Figure (e), to produce a variable BFO Control.

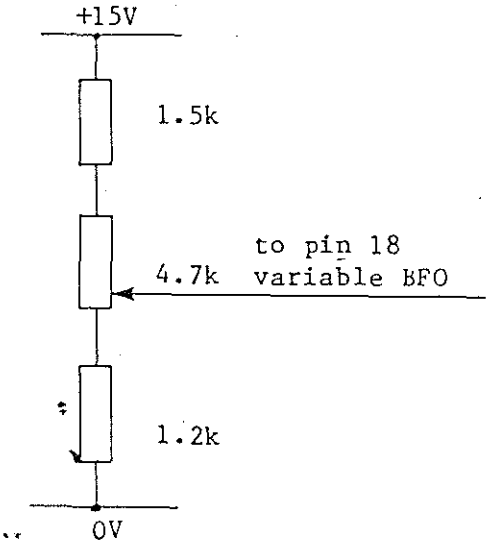


FIG (e) VARIABLE BFO CONTROL

4.3 Power Supplies

Separate +15V and +9V supplies are required.

4.4 Alignment and Functional Tests

4.4.1 Connect the +15V supply to edge-pin 22, the +9V supply to edge-pin 20 and 0V to edge pin 1. Using the Avometer check the current consumption of the supplies; +15V supply not more than 110mA, the +9V supply not more than 30mA. Check the d.c. voltage levels at the following points:

IC3 pin 2 - 12.0 $\pm$ 0.5V
IC2 pin 2 - 6.0 $\pm$ 0.3V

Select the following control signals by applying a logic '1' to the appropriate pins:

LOCAL - edge-pin 17
LOCAL BFO - edge-pin 18
XTAL - edge-pin 8
'L' MODE - edge-pin 13

4.4.2 1.5MHz Loop

Connect the 1MHz reference output from the frequency counter to SKTG (1MHz INPUT) and the input of the frequency counter to SKTC. Set the oscilloscope controls to DC, 0.2V/cm (assuming X10 probe) and connect the probe to TP1. Adjust L4 to give a constant d.c. display on the oscilloscope of 6.0V $\pm$ 0.5V. Check that the frequency counter reading is 1.50000MHz. Lock $\overline{\text{L4}}$.

4.4.3 1.4MHz Loop

Connect the frequency counter input to SKTA and the oscilloscope probe to TP2. Adjust L3 to give a constant d.c. display on the oscilloscope of 7 $\pm$ 0.25V. Check that the frequency counter reading is 1.40000MHz. Lock $\overline{\text{L3}}$.

4.4.4 BFO

Select the following control signals (logic '1' on appropriate pins):

LOCAL - edge-pin 17
CW - edge-pin 14

Connect the oscilloscope probe to TP3. Connect the potentiometer network to 0V, 15V and edge-pin 18 (LOCAL BFO) as shown in Figure (e). Adjust the 4.7k potentiometer (var. BFO) fully clockwise and note the DC reading on the oscilloscope. Readjust the potentiometer fully counter clockwise until the DC reading on the oscilloscope is half the value noted above. (NOTE: there will be a standing DC of approximately 2 Volts). Adjust C57 to give a frequency counter reading of 1.40000MHz $\pm$ 100Hz, and note reading. Adjust the Var. BFO potentiometer fully clockwise and note the change in frequency from that noted above. The frequency change should be not less than 8kHz. Adjust the Var. BFO potentiometer fully counter clockwise and again note the change in frequency, which should be not less than 8kHz. Select the 'REMOTE' control signal (logic '1' to edge-pin 16) and check that the frequency reading remains unchanged.

4.4.5 Fixed BFO

Select mode 'F' by applying a logic '1' to edge-pin 15. Set switches IC/S9 and 1C/S10 on the printed circuit panel as follows:

IC/S9 '4' ON, 1-3, 5-8 'OFF'
IC/S10 1-4 'OFF'

The frequency reading should be 1.39760MHz.
Set the switches IC/S9, IC/S10 as follows:

IC/S9 1 and 4 - 'OFF', 2, 3, 5, 8 - 'ON'
IC/S10 1 to 4 - 'ON'

Check that the frequency is 1.39770MHz.

Set the switches IC/S9, IC/S10 as follows (2.5kHz):

IC/S9 1, 4, 6, 7 - 'OFF', 2, 3, 5, 8 - 'ON'
IC/S10 1-4 'ON'

Check that the frequency is 1.40250MHz.

4.4.6 Reconstituted Carrier

Select mode 'USB' (logic '1' on edge-pin 12) and connect the signal generator, set to 1.4MHz, to SKTE. Connect a 100uA F.S.D. meter to the ZERO BEAT, METER DRIVE output pin 6. Connect the oscilloscope probe to TP4. Adjust the signal generator frequency to give a slow beat on the meter (less than 5 beats/second). Check that the needle slewing is reasonably centralised. Select the control signal 'RECON CARRIER' (logic '1' on edge-pin 7) and check that the frequency reading on the counter is 1.400000 $\pm$ 5Hz. Check that the constant d.c. reading on the oscilloscope is 6.0 $\pm$ 0.5V. Slowly vary the signal generator frequency and check that the reading on the frequency counter varies with the signal generator.

4.4.7 Output Levels

Connect a 1k load resistor to SKTC and the oscilloscope probe to edge-pin 3. Check that the amplitude of the 1.5MHz output is 300mV $\pm$ 100mV peak-to-peak. Connect a 1k load resistor to SKTA and the oscilloscope probe to pin 5. Check that the 1.4MHz output is 300mV $\pm$ 100mV peak-to-peak.

4.5 The module should be inspected to ensure that no damage has been caused during testing.

4. COMPONENT LISTS

Main Assembly (630/1/32986)
Panel Electronic Circuit (419/1/18018)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Panel Printed Circuit	Plessey	419/2/18019
-	Socket Semi-Conductor	Texas 14L DIL C931402	508/4/22096/002
-	Socket Semi-Conductor	Texas 16L DIL C391602	508/4/22096/003
C60	Capacitor 22pF ± 1% 30V	Suflex HSC 22	437/4/30011/083
C9,36	Capacitor 100pF ± 2% 30V	Lemco MS80/M/R	438/4/25898/001
C17	Capacitor 150pF ± 2.5%	Lemco MS80/M/R	437/4/30011/025
C10	Capacitor 470pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/019
C38	Capacitor 850pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/109
C20	Capacitor 960pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/110
C16,33	Capacitor 1nF ± 5% 400V	Siemens B32560	435/4/90317/023
C48	Capacitor 2.2nF ± 5% 400V	Siemens B32560	435/4/90137/025
C19,35	Capacitor 4.7nF ± 5% 400V	Siemens B32560	435/4/90137/027
C29	Capacitor 6.8nF ± 5% 400V	Siemens B32560	435/4/90317/028
C11,28	Capacitor 10nF ± 5% 400V	Siemens B32560	435/4/90317/029
C2,4,7,12-14,18,22-27,39-47,49-51,53-56,58,59	Capacitor 100nF ± 5% 100V	Siemens B32560	435/4/90317/014
C1,3	Capacitor .33uF ± 20% 35V	ITT TAG	402/4/57057/002
C8,21,37	Capacitor 10uF ± 20% 16V	ITT TAG	402/4/57057/003
C32	Capacitor 22uF ± 20% 16V	ITT TAG	402/4/57057/009
C6,15,30,31	Capacitor 100uF ± 20% 16V	ITT TAG	402/4/57057/019
C34	Capacitor 1uF ± 20% 35V	ITT TAG	402/4/57057/003
C5	Capacitor 33uF ± 20% 16V	ITT TAG	402/4/57057/010
C57	Capacitor Variable 5-57pF	Mullard 809-08002	401/4/32131/002
L9	Inductor 22uH ± 10%	Sigma SC30	406/4/31753/028
L3,4	Inductor 68uH ± 10%	Cambion 558-1199-18	406/4/31751/018
L1,2,5,6,7	Inductor 100uH ± 10%	Sigma SC30/37	406/4/31753/036
L8	Inductor 10mH ± 10%	Sigma SC60/49	406/4/31754/025
IC16	Integrated Circuit	Motorola MC14013CP	445/4/02383/013
IC5,11,14	Integrated Circuit	Motorola MC14046CP	445/4/02383/046
IC4,12,20	Integrated Circuit	Motorola MC14066CP	445/4/02383/060
IC18,19	Integrated Circuit	Motorola MC14518CP	445/4/02383/518
IC6,7,8,15	Integrated Circuit	Motorola MC14526CP	445/4/02383/526
IC1	Integrated Circuit	RCA CD4075BE	445/4/02383/075
IC2	Integrated Circuit	Motorola MC7806CT	445/4/03051/002
IC3	Integrated Circuit	Motorola MC7812CT	445/4/03051/004
IC17	Integrated Circuit	Plessey	445/4/02386
IC13	Integrated Circuit	Texas SN 7666 ON	445/4/03052
IC/S9	Integrated Circuit Switch	Siemens C42315-A1341-A4	408/9/51492/007
IC/S10	Integrated Circuit Switch	Siemens C42315-A1341-A1	408/9/51492/003
R63	Resistor 56R ± 2%	Electrosil TR4	403/4/05521/560
R56,75,85	Resistor 330R ± 2%	Electrosil TR4	403/4/05522/330
R93	Resistor 560R ± 2%	Electrosil TR4	403/4/05522/560
R7-12,15-17,31,32,57,58,76,77,82-84,86	Resistor 1k ± 2%	Electrosil TR4	403/4/05523/100

Panel Electronic Circuit (Cont'd)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
R35,52,54, 55,59,62, 64,71,73, 74,78,81, 91,95	Resistor 2.2k ± 2%	Electrosil TR4	403/4/05523/220
R33	Resistor 3.3k ± 2%	Electrosil TR4	403/4/05523/330
R51,60,70,79	Resistor 4.7k ± 2%	Electrosil TR4	403/4/05523/470
R25,26,27,67	Resistor 10k ± 2%	Electrosil TR4	403/4/05524/100
R53,72	Resistor 12k ± 2%	Electrosil TR4	403/4/05524/120
R66	Resistor 33k ± 2%	Electrosil TR4	403/4/05524/330
R65	Resistor 68k ± 2%	Electrosil TR4	403/4/05524/680
R34,61,80,92	Resistor 82k ± 2%	Electrosil TR4	403/4/05524/820
R1-6,14,18, 19,22,23, 36-47,49, 50,68,69,87	Resistor 100k ± 2%	Electrosil TR4	403/4/05525/100
R89	Resistor 270k ± 2%	Electrosil TR4	403/4/05525/270
R30	Resistor 560k ± 5%	Allen Bradley Type CB	403/4/04361/001
R20,21,88,24, 29	Resistor 1M ± 5%	Allen Bradley Type CB	
R90	Resistor 6.8k ± 2%	Electrosil TR4	403/4/05523/680
R24,48	Resistor 18k ± 2%	Electrosil TR4	403/4/05524/180
R94	Resistor Variable	Allen Bradley Type 90H	404/9/05047/009
D2,3	Diode	Texas 1N4148	415/4/05720
D1,4,5,6	Diode	Motorola MV2115	415/9/98905/014
TR3,4,6,8,10, 15	Transistor	Mullard BC107	417/4/01777
TR12	Transistor	Mullard BC177	417/4/01859
TR11,13,14,7	Transistor	Texas 2N2369	417/4/01881
TR2	Transistor	Texas 2N5245	417/4/01882

Connector Assembly (702/1/20093/002)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
SKC,G	Socket Electrical R.F.	Belling Lee L1465/K/BS	508/4/22059
-	Cable R.F.	Suhner R.G. 174/U 150mm	998/4/70537/001

Connector Assembly (702/1/20093/003)

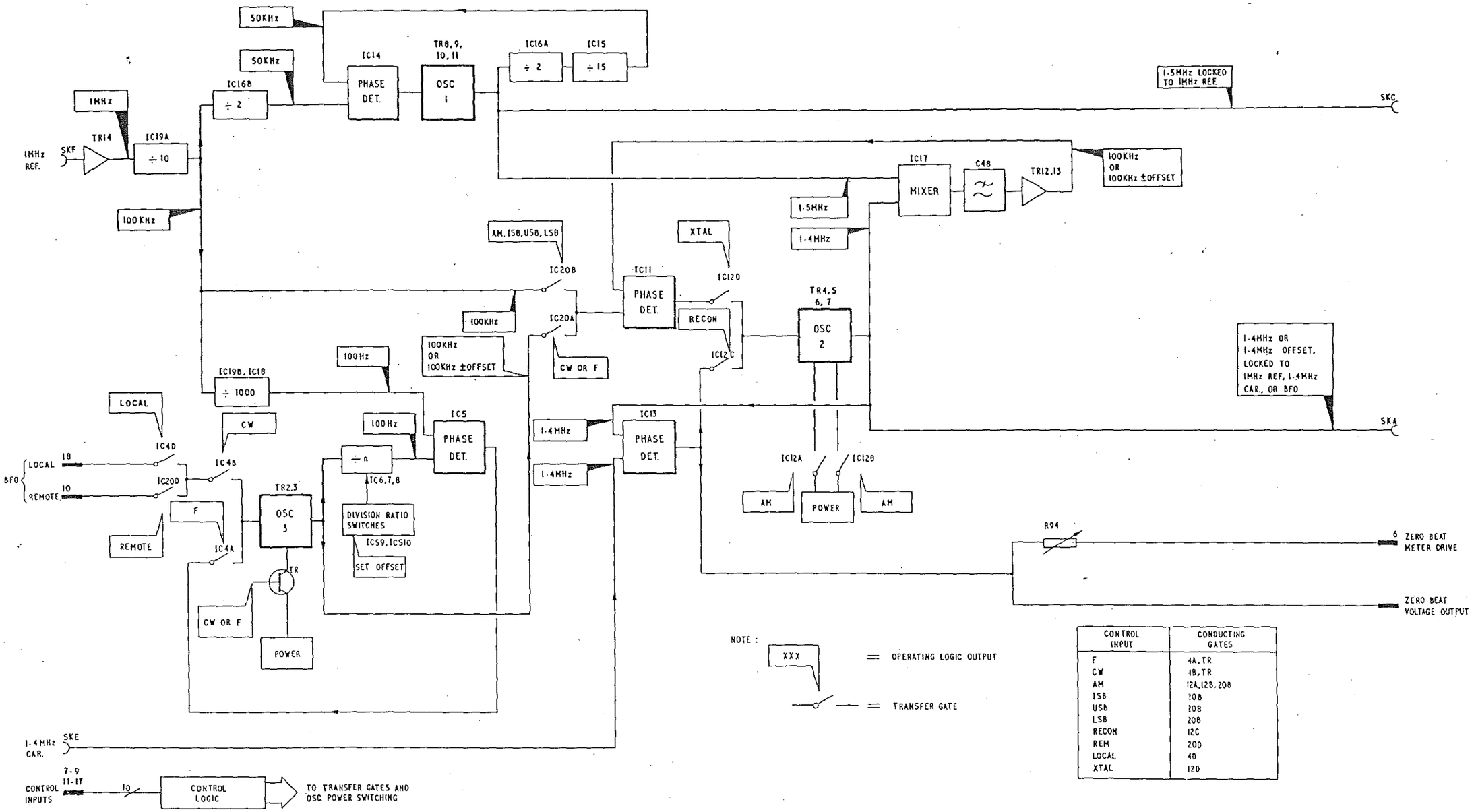
Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
SKF	Socket Electrical R.F.	Belling Lee L1465/K/BS	508/4/22059
-	Cable R.F.	Suhner R.G. 174/U 170mm	998/4/70537/001

Connector Assembly (702/1/20093/004)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
SKA -	Socket Electrical R.F. Cable R.F.	Belling Lee L1465/K/BS Suhner R.G. 174/U 190mm	508/4/22059 998/4/70537/001

Connector Assembly (702/1/20093/006)

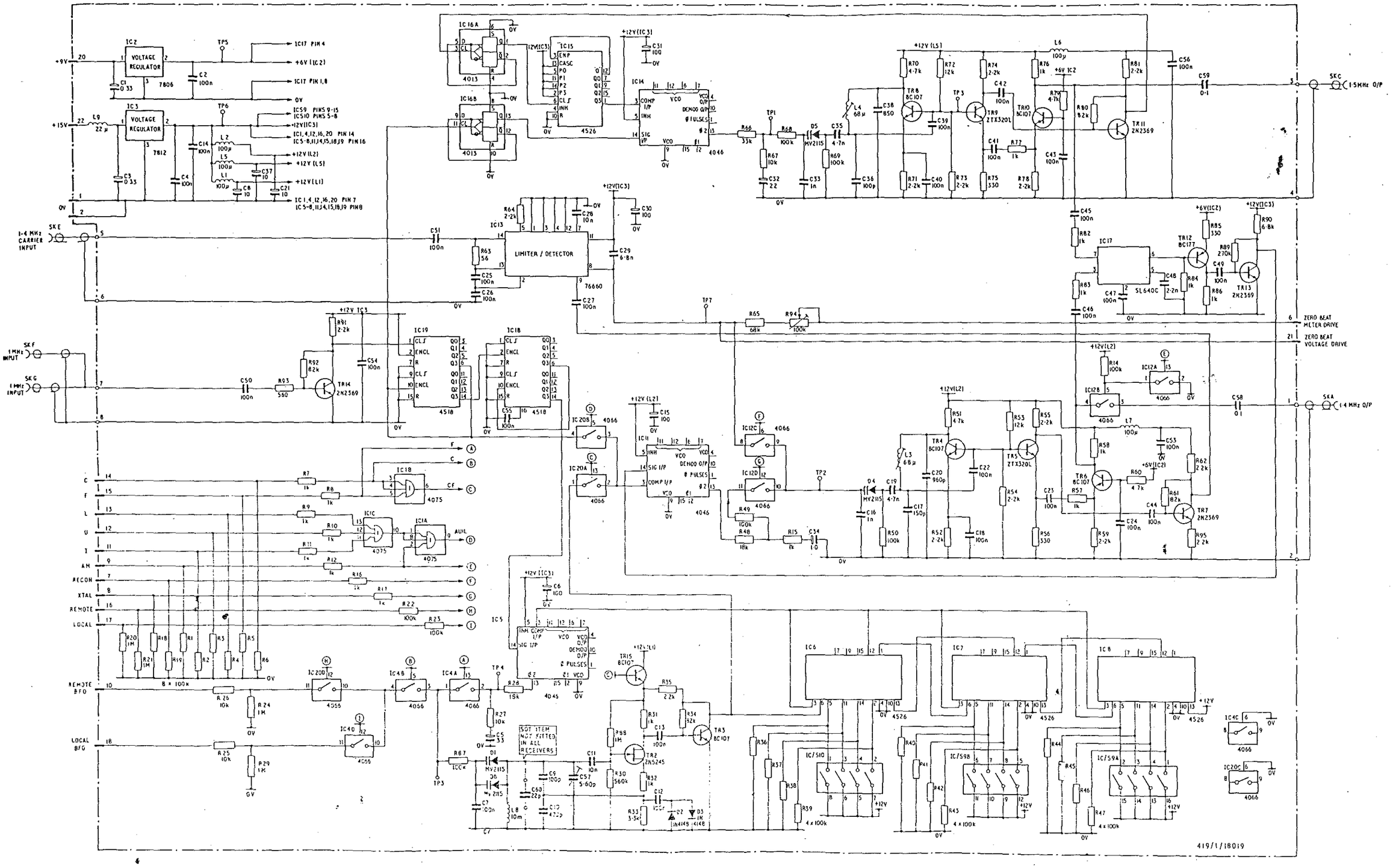
Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
SKE -	Socket Electrical R.F. Cable R.F.	Belling Lee L1465/K/BS Suhner R.G. 174/U 230mm	508/4/22059 998/4/70537/001



CONTROL INPUT	CONDUCTING GATES
F	4A, TR
CW	4B, TR
AM	12A, 12B, 20B
ISB	20B
USB	20B
LSB	20B
RECON	12C
REM	20D
LOCAL	4D
XTAL	12D

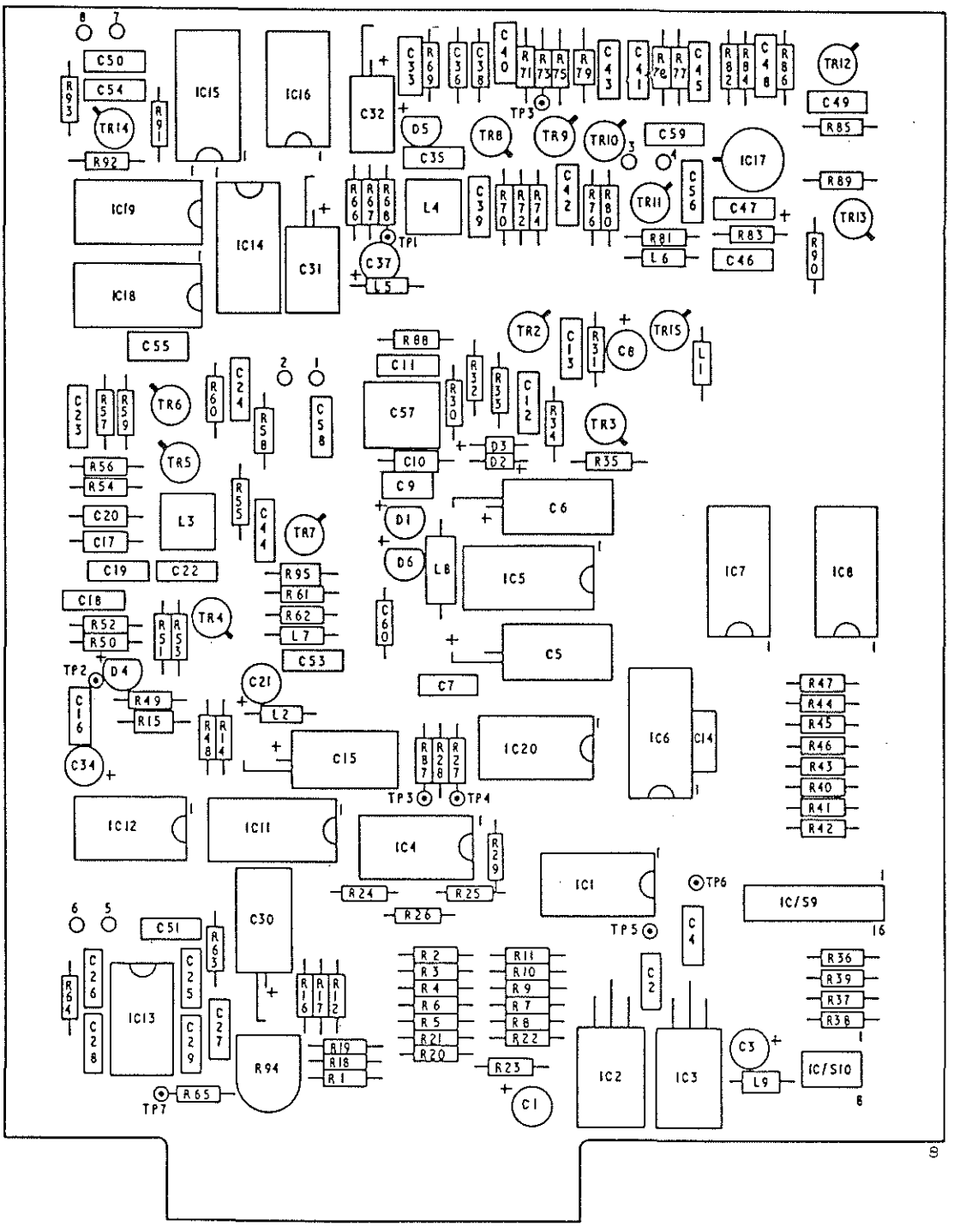
MODULE 6 FUNCTIONAL BLOCK DIAGRAM

FIG 1



MODULE 6 : BFO CIRCUIT DIAGRAM

FIG 2



MODULE 6 PANEL - COMPONENT LAYOUT

FIG. 3

CHAPTER 7

MODULE 7A, 1MHz REFERENCE OSCILLATOR

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ILLUSTRATIONS

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MODULE 7A, 1MHz REFERENCE OSCILLATOR

1. FUNCTIONAL DESCRIPTION

Module 7A is the frequency standard for the receiver. It is fitted in all PR2250 and PR2252 models, and consists of a high stability 10MHz crystal oscillator feeding an emitter-follower output stage via a divide-by-ten circuit. The block diagram can be seen in Figure (a).

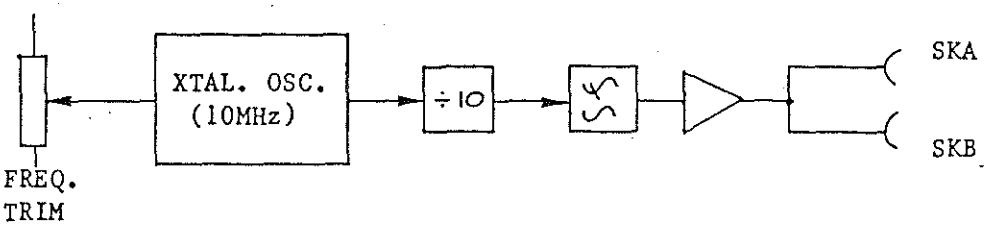


FIG (a) MODULE 7A FUNCTIONAL BLOCK DIAGRAM

2. CIRCUIT DESCRIPTION

2.1 Crystal Oscillator

An encapsulated crystal oscillator unit which includes the crystal oven is employed. A 9V supply to pin 4 supplies the oven heater, while the oscillator itself is supplied by 5V applied to pin 3. Pin 2 is the common 0V terminal. Frequency is trimmed by a variable d.c. potential applied to pin 5; this is derived from a 6.2V temperature-controlled zener reference diode, D1, and exercises control via an internal varactor diode. Output is taken from pin 1 at 10.0000MHz.

2.2 Divide-by-ten Circuit

The oscillator output is applied to IC2, which is a TTL Decade counter. A square-wave output is obtained from pin 12 at one-tenth the frequency of the input applied to pin 1 when pins 11 and 14 are strapped together.

2.3 Low-pass Filter and Output Stages

The 1MHz output from IC2 is applied to a 2 section LC low-pass filter formed by L2, L3, C6, and C7. An almost sinusoidal 1MHz output is obtained, and applied to emitter-follower TR1 to provide two identical outputs on SKA and SKB.

3. TEST DATA

The procedure outlined in the following paragraphs forms a complete test procedure and need not be used to locate individual faults.

3.1 Test Equipment

The following items of test equipment are required:

Avometer.
Oscilloscope (general purpose).

3.2 Power Supplies

A +9V supply is required.

3.3 Alignment and Functional Tests

3.3.1 Connect the +9V supply to edge-pins 11 and 12, and using the Avometer, check the current consumption (not more than 900mA). Measure the voltage at IC1 pin 2 (5V $\pm$ 0.3V).

3.3.2 Output Level

Connect the oscilloscope to SKTA and SKTB in turn and measure the amplitude of the output signal which should be the same in each case:

Not less than 1.2V peak-to-peak

Check that the waveform is approximately sinusoidal.

3.3.3 Frequency Setting

It is essential that the frequency setting is not disturbed unnecessarily as it forms the 1MHz reference signal. If the frequency is wrong check for adjustment by a 1:1 lissajous pattern test with a 1 part in 10^9 reference source.

3.4 The module should be inspected to ensure that no damage has been caused during testing.

4. COMPONENT LISTS

Main Assembly (630/1/32987/001)
Panel Electronic Circuit (419/1/18027)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Panel Printed Circuit	Plessey	419/2/18028
-	Socket Semi-Conductor	Texas 14L DIL C391602	508/4/22096/002
C6,7	Capacitor 470pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/019
C2-5,8-11	Capacitor 0.1uF ± 5% 100V	Siemens B32560	435/4/90317/014
C1	Capacitor 0.33uF ± 5% 100V	Siemens B32560	435/4/90317/018
L2	Inducator 47uH ± 10%	Sigma SC10	406/9/31741/001
L1	Inductor 100uH ± 10%	Sigma SC10	406/9/31741/002
L3	Inductor 100uH ± 10%	Sigma SC10	406/9/31741/003
IC1	Integrated Circuit	Motorola MC7805 UC	445/9/03051/001
IC2	Integrated Circuit	Texas SN5.190 AJ	445/4/03050
R8,9	Resistor 39R ± 2%	Electrosil TR4	403/4/05521/390
R7	Resistor 100R ± 2%	Electrosil TR4	403/4/05522/100
R4	Resistor 470R ± 2%	Electrosil TR4	403/4/05522/470
R5	Resistor 1.8k ± 2%	Electrosil TR4	403/4/05523/180
R2	Resistor 390R ± 2%	Electrosil TR4	403/4/05522/390
R6	Resistor 3.3k ± 2%	Electrosil TR4	403/4/05523/330
R3	Resistor 10k ± 2%	Electrosil TR4	403/4/05524/100
R1	Resistor Variable 5k	Morganite AB84	404/4/08057/009
TR1	Transistor	Mullard BC109	417/4/01776
D1	Diode	Semitron ZR823	415/9/05754/003

Panel Electronic Circuit (419/1/18051)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Panel Printed Circuit	Plessey	419/2/18052
OSC.1	Crystal Oscillator	Cathodeon FS5953.01 10MHz	428/1/05030
-	Spacer Threaded	Harwin R6076 M2.5 x 14LG	999/9/32544/006
PL7	Plug Electrical	Cannon DEF 9P	

Connector Assembly (702/1/20096/001)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
SKB	Socket Electrical R.F.	Belling Lee BLL004-0703-AC-C001V	508/4/22113
-	Cable R.F.	Suhner R.G. 174/U 150mm	998/4/70537/001

Connector Assembly (702/1/20096/002)

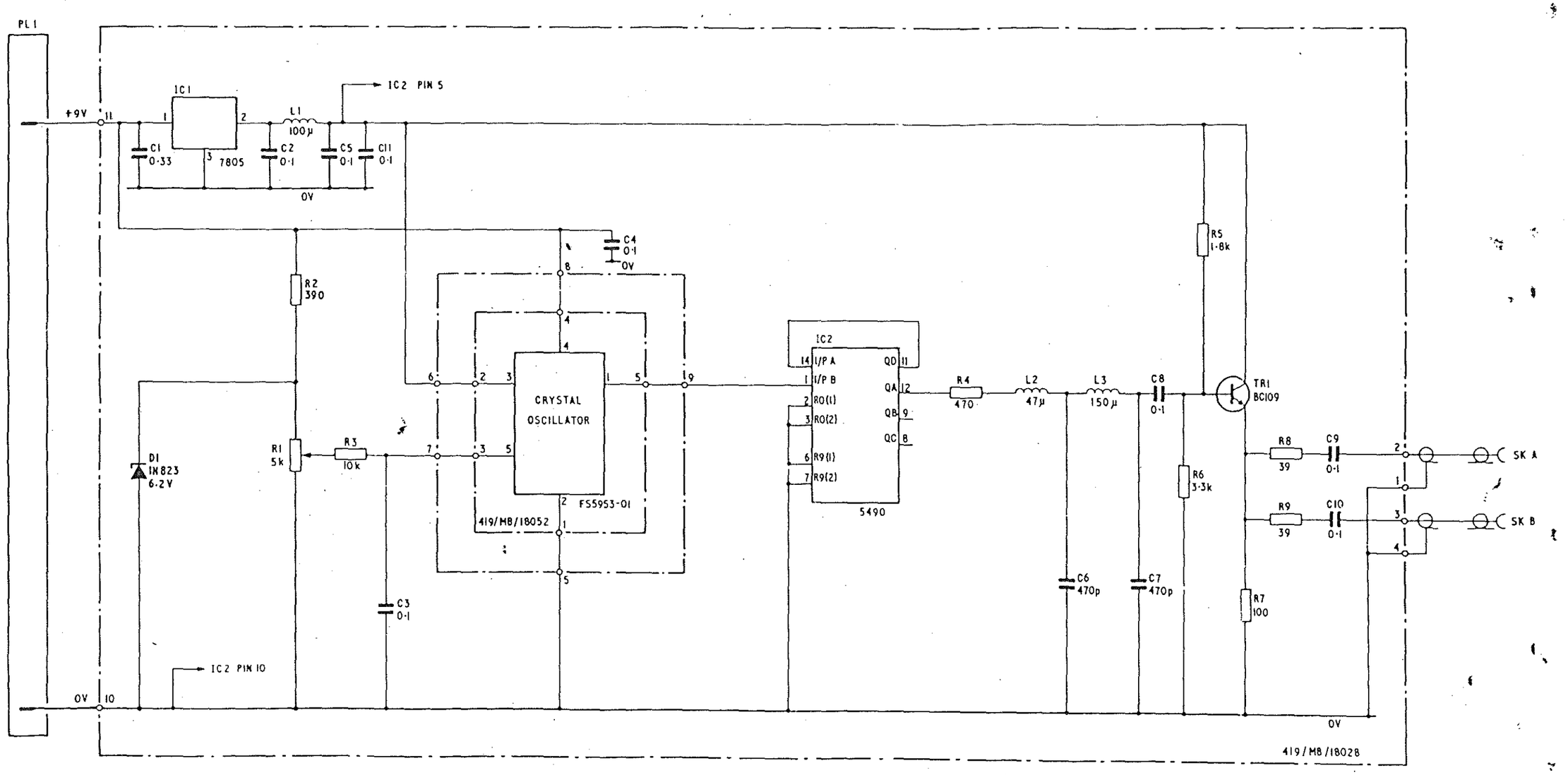
Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
SKA	Socket Electrical R.F.	Belling Lee BLL004-0703-AC-L00V	508/4/22113
-	Cable R.F.	Suhner R.G. 174/U 200mm	998/4/70537/001

INTEGRATED CIRCUIT DEFINITIONS

This information forms a supplement to the circuit diagrams in respect of complex integrated circuits which are shown diagrammatically by a rectangular outline only.

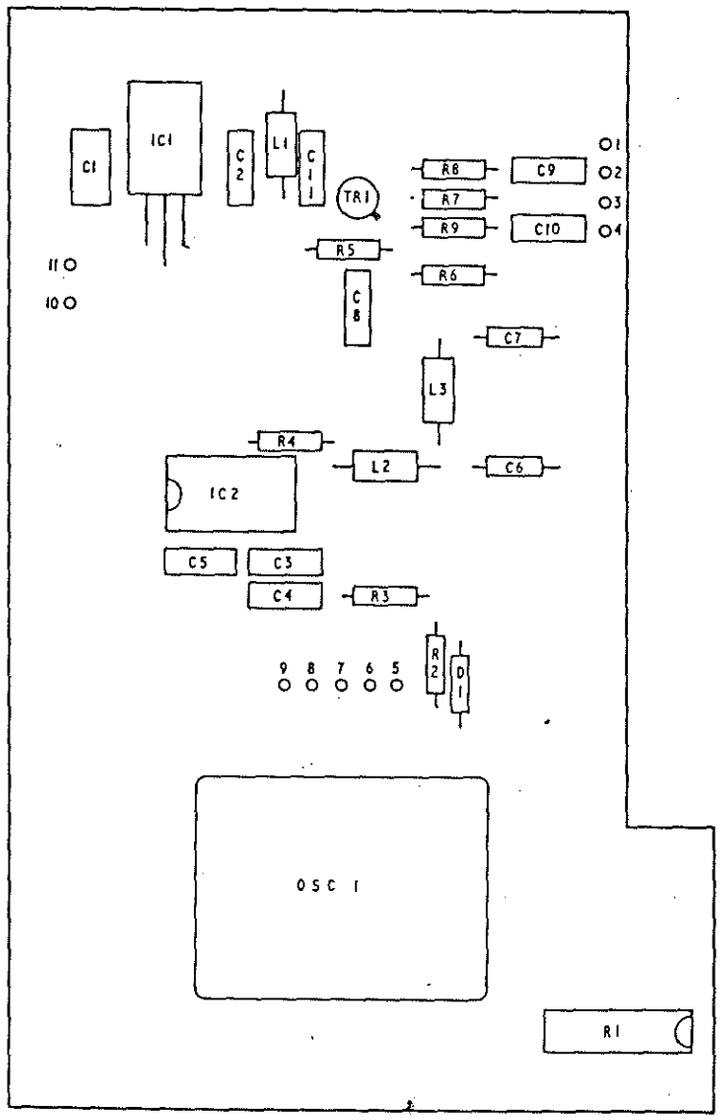
SN 5490

Decade counter. Produces a binary count of clockpulses on Q outputs. QA is LSB, QD is MSB.



MODULE 7A : 1 MHz REFERENCE OSCILLATOR CIRCUIT DIAGRAM

FIG 1



MODULE 7A PANEL - COMPONENT LAYOUT

FIG. 2

CHAPTER 8

MODULE 8A POWER SUPPLIES

CONTENTS

TABLES

ILLUSTRATIONS

MODULE 8 POWER SUPPLIES

1. FUNCTIONAL DESCRIPTION

1.1 Module 8A is the Power Supply Unit, and is fitted in all models of the PR2250 series receivers. D.C. power outputs at +9V, +12V, +15V, +24V, and +70V are produced from a 45 to 400Hz single-phase a.c. supply of either 100 to 125V or 200 to 250V. Power consumption is approximately 65VA. A functional block diagram can be seen in Figure (a).

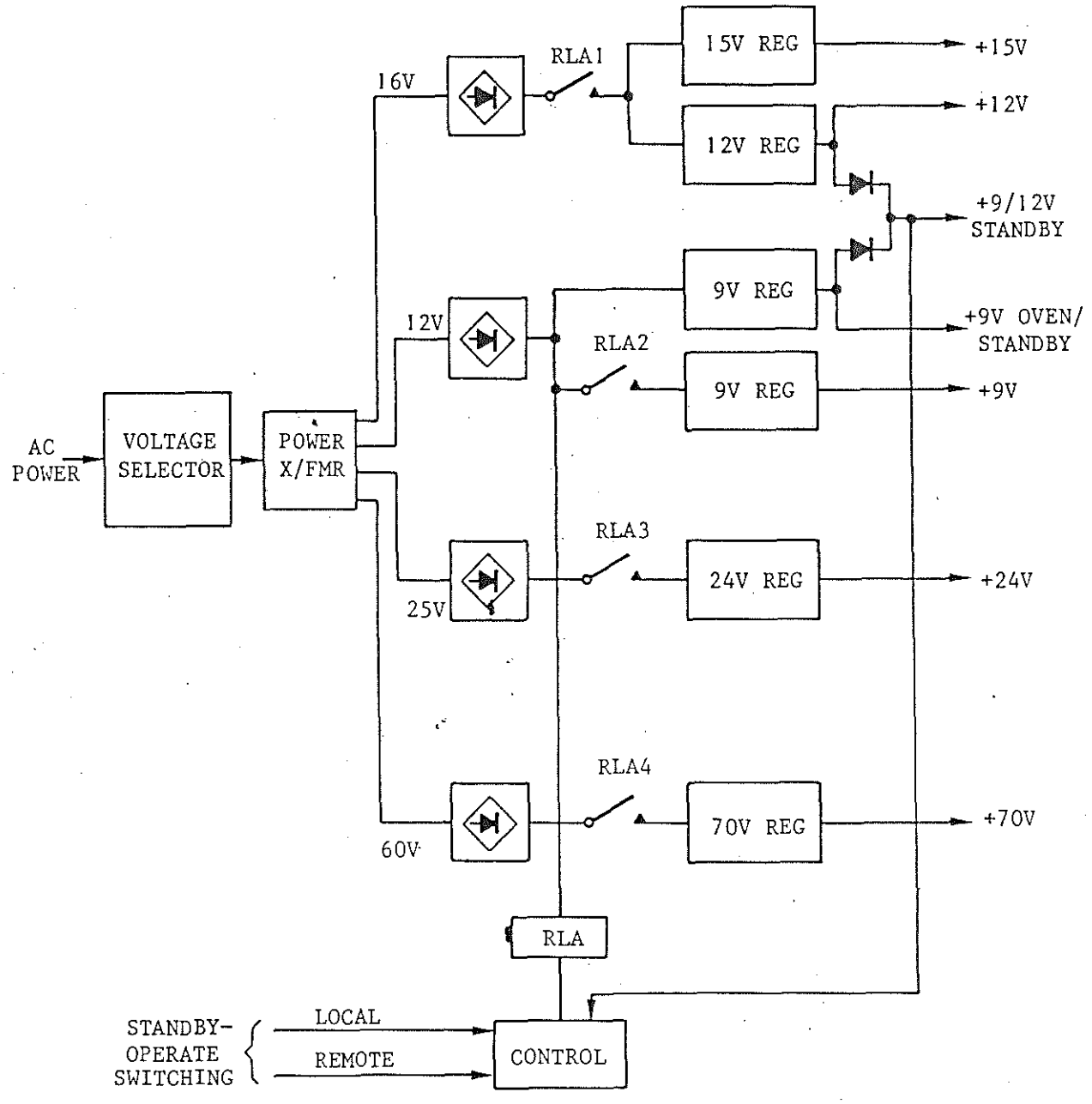


FIG (a) MODULE 8A FUNCTIONAL BLOCK DIAGRAM

1.2 Four bridge rectifiers are fed from the power transformer. Each bridge rectifier is followed by a reservoir capacitor and discharge resistor. In the receiver 'standby' state, a.c. power is applied, and therefore one

9V regulator produces an output (+9V/12V STANDBY) and also supplies the control logic. Switching relay RLA is operated by the control logic and is powered by the raw 12V rectifier output.

1.3 On switching the receiver from STANDBY to OPERATE, RLA is energised. Raw d.c. is applied to the remaining five regulator circuits, and all d.c. outputs are available. In addition, the +9V/+12V STANDBY output voltage rises from +9V to +12V. All voltage regulators incorporate over-current and thermal protection.

2. CIRCUIT DESCRIPTION

2.1 A.C. Circuits

The a.c. power supply to Module 8A is applied via 3-pin plug PL1 and fuse FS1. The pins of PL1 are coded L, N, and E in accordance with British standard practice. In Britain, public a.c. power supplies have one side earthed (grounded) at the generating station; this line is known as NEUTRAL (N). The other line is known as LIVE (L), and is the line in which fuses and single-pole on-off switches are inserted. A third pin is also used on all British power sockets (outlets); this is locally connected to earth (frequenctly via a copper water-supply pipe forming part of the public utility system) and is known as EARTH (E). Corresponding British power lead core colours are:

LIVE	: BROWN
NEUTRAL	: BLUE
EARTH	: GREEN/YELLOW

In places where two-pin a.c. sockets are accepted practice, the E pin of PL1 should be locally earthed via the green/yellow core of the supplied power lead. In places where neither side of the a.c. power supply is earthed at the generating station, the L and N markings have no significance.

2.2 The fuse-protected a.c. supply is applied to the power transformer via a voltage selector panel. To set the selector for a particular supply voltage, plug in the bar so that the arrow points to the appropriate voltage figure.

2.3 Four a.c. outputs are produced by the power transformer, all from separate windings. The outputs are 16V, 3.5A:10V, 3A:25V, 1.6A:60V, 0.1A. Each output is protected by a separate fuse.

2.4 Rectifiers

Each of the four outputs from the power transformer is rectified by a conventional bridge circuit. A reservoir capacitor and discharge resistor is connected across the output of each rectifier.

2.5 Control Switching

2.5.1 When set to LOCAL, the front-panel LOCAL/REMOTE switch applies a '0' level to SK1 pin 13; when set to REMOTE, a '1' level is applied. When the front-panel STANDBY/OPERATE switch is set to OPERATE, a '1' level is applied to SK1 pin 11. When the remote STANDBY/OPERATE switch is set to OPERATE, a '1' level is applied to SK1 pin 10. LOCAL and OPERATE therefore produces a '1' level output from IC5B, while REMOTE and OPERATE produces a '1' level output from IC5A: both of these states produce a '1'

level at IC5D output provided that the pull-up level applied to pin 12 is '1'. This pull-up is supplied via TR9, and is provided to avoid relay chatter at switch-on or any other power transient situation; at switch-on there is a slight delay in the application of the pull-up level while C18 charges via R39. Pull-up is also applied to IC5C.

2.5.2 A '1' level output from IC5D produces, via D34, a '1' output from IC5C; this is applied to TR7 base, causing RLA to energise. Positive feedback is applied via C17 and R28 to ensure a 'clean' start. An inverted control logic level output on SK1 pin 9 is taken from IC5D via TR8.

2.6 Voltage Regulators

2.6.1 Integrated Circuit Regulators

The outputs from Rectifier 1 and Rectifier 2 are regulated by IC regulators. Three types are employed, 15 volt, 12 volt, and 8 volt. In all cases, the raw d.c. is applied to pin 1, and the regulated output is taken from pin 2. If pin 3 is connected directly to 0V, the stated output voltage is obtained. If pin 3 is held at a potential above 0V, then that potential is added to the output voltage. This method is employed to produce a +9V output from IC3 and IC4; two conducting diodes in series between pin 3 and 0V raise pin 3 approximately +1.2V above 0V. All ICs incorporate overload protection.

2.6.2 Each IC regulator provides a separate regulated output from Module 8A. In addition, the outputs from IC1 and IC3 are combined via diodes D17 and D19 to provide the +9V/+12V STANDBY output (ref.paragraph 1.3).

2.6.3 24 Volt Regulator

The 24V regulator supplied by Rectifier 3 consists of TR1, 2, 3, 4, and associated components. The raw d.c. is connected via R15 and series regulator transistor TR2 to the load between SK1 pins 19 and 37 and 0V (SK1 pins 11 and 20). TR2 emitter current is controlled by TR1 base current, and TR1 base potential is held by D23 and D24 at 1.2V negative to raw d.c. voltage. If, therefore, load current via TR2 and R15 increases to approximately 3.6A, TR1 emitter potential moves negatively to 1.2V negative to raw d.c. voltage. TR1 then cuts off, providing over-current protection.

2.6.4 Under normal running conditions, TR1 base current is determined by the base and emitter potentials of TR3, which are in turn determined by the voltage across the load. Variations in load voltage will react on TR4 emitter current and therefore, via TR3 collector current, on TR1 base current.

2.6.5 70 Volt Regulator

The 70 volt regulator supplied by Rectifier 4 (D13-D16) consists of TR5, 10, 11 and associated components. The regulating action of TR10 and TR11 is identical with that of TR3 and TR4 as described in paragraph 2.6.3. Overload protection is only provided in respect of an output short-circuit: this condition holds TR10 base at 0V, and therefore shuts off TR5 base current.

3. TEST DATA

The procedure outlined in the following paragraphs forms a complete test procedure and need not be used to locate individual faults.

3.1 Test Equipment

The following items of test equipment are required:

Digital Voltmeter (DVM)

Mains power supply connector and lead

Resistance loads for the supplies and monitor points as shown in Table 1.

TABLE 1 : RESISTANCE LOADS

Supply (volts)	Resistance (ohms)	Wattage	SK1 pin (0V pin 1)
9V oven	23.5	4 watts	21
9V supply	10	3 watts	35
12V logic	10	15 watts	34
15V audio	50	4 watts	5
15V supply	34	7 watts	36
24V supply	25	25 watts	19
70V supply	2.2k	3 watts	2

3.2 Alignment and Functional Tests

WARNING: CARE MUST BE TAKEN WHEN WORKING ON MODULE 8A WITH THE COVERS REMOVED AND MAINS POWER CONNECTED AS THE 115/240V AC and +70V DC SUPPLY TERMINALS ARE LIVE AND EXPOSED.

3.2.1 Check that the mains tappings on the module are set correctly. Remove the four retaining screws from the top cover of the module, and fold the cover back to expose the printed circuit panel and the presets, R8 and R43. Connect the mains supply to the module but do not switch on the mains supply.

3.2.2 Standby/Operate

Set the module to "LOCAL" operation by connecting a logic '0' (0V) to SK1 pin 13 and switch the mains supply on. Check that the"STANDBY INDICATOR" supply is present on SK1 pin 28, and that no supply is present on SK1 pin 27 (OPERATE). Set the module to 'OPERATE' by applying a logic '1' (+12V) to SK1 pin 11 and check that the "STANDBY" and "OPERATE" indicator supply is present on SK1 pins 27 and 28. Set the module to 'REMOTE' operation by applying a logic '1' (+12V) to SK1 pin 13 and repeat the above tests (apply a logic '1' to SK1 pin 10 instead of SK1 pin 11).

3.2.3 Supply Levels

Switch the mains supply to the module off and connect the load resistors shown in Table 1 to the appropriate pins on SK1. Switch the mains supply on and set the module to 'LOCAL' and 'OPERATE' (logic '0' on SK1 pin 13 and logic '1' pin 11). Connect the digital voltmeter (DVM) across the +24V supply (SK1 pins 19 and 11), and adjust R8 on the printed circuit

panel to give 24V ± 0.2V. Connect the DVM across the +70V supply (SK pins 2 and 11), and adjust R43 to give +70V ± 0.5V. Using the DVM check the supply voltages shown in Table 2.

TABLE 2 : SUPPLY VOLTAGES

Supply	DVM reading	SK1 pins (0V pin 1)
+15V audio	14.3 ± 1V	23
+15V supply	15.0 ± 0.8V	17
+12V logic	12.0 ± 0.6V	15
+9V/12V standby	11.4 ± 0.8V	18
+9V supply	9 ± 1V	16
+9V oven	9 ± 1V	21
+24V supply	24 ± 1.5V	37
+70V supply	70 ± 4V	2

3.3 The module should be inspected to ensure that no damage has been caused during testing. Refit the top cover.

4. COMPONENT LISTS .

Main Assembly (630/1/32988)
Panel Electronic Circuit (419/1/17990)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Panel Printed Circuit	Plessey	419/1/17990
-	Socket Semi-Conductor	Texas C931402	508/4/22096/002
C15	Capacitor 1nF ± 5% 400V	Siemens B32560	435/4/90317/023
C17	Capacitor 220nF ± 5% 100V	Siemens B32560	435/4/90317/017
C19	Capacitor 470nF ± 5% 100V	Siemens B32560	435/4/90317/019
C18	Capacitor 2.2uF ± 20% 35V	ITT TAG	402/4/57057/004
C13	Capacitor 10uF ± 20% 35V	ITT TAG	402/4/57057/006
C4	Capacitor 470uF +50% -10% 100V	EN12-12 100/100	402/4/57056/004
C20	Capacitor 4.7nF ± 10% 100V	Erie 8111M-X7R	400/4/21280/001
IC5	Integrated Circuit	Motorola MC14081 BCP	445/4/02383/081
RL1	Relay	Thorn NF4 12V	507/4/05129/005
R15	Resistor 0.33R ± 5%	Welwyn Type W21	403/4/04276/033
R12	Resistor 100R ± 2%	Electrosil TR4	403/4/05522/100
R10	Resistor 560R ± 2%	Electrosil TR4	403/4/05522/560
R1,4,14,28	Resistor 1k ± 2%	Electrosil TR4	403/4/05523/100
R11,13	Resistor 2.2k ± 2%	Electrosil TR4	403/4/05523/220
R41	Resistor 2.7k ± 2%	Electrosil TR4	403/4/05523/270
R7,9,44	Resistor 5.6k ± 2%	Electrosil TR4	403/4/05523/560
R16	Resistor 6.8R ± 2%	Electrosil TR4	403/4/05523/680
R21	Resistor 82k ± 2%	Electrosil TR4	403/4/05524/820
R40	Resistor 15k ± 2%	Electrosil TR5	403/4/05524/150
R46	Resistor 18k ± 2%	Electrosil TR4	403/4/05524/180
R29,30	Resistor 47k ± 2%	Electrosil TR4	403/4/05524/470
R42	Resistor 56k ± 2%	Electrosil TR4	403/4/05524/560
R3,6,22, 27,31-35, 37-39	Resistor 100k ± 2%	Electrosil TR4	403/4/05525/100
R17	Resistor 150k ± 2%	Electrosil TR4	403/4/05525/150
R2	Resistor 180k ± 2%	Electrosil TR4	403/4/05525/180
R5	Resistor 300k ± 2%	Electrosil TR4	403/4/05525/300
R45	Resistor 820k ± 5%	Allen Bradley Type CB	403/4/04361/002
R36	Resistor 1M ± 5%	Allen Bradley Type CB	403/4/04361/003
R23	Resistor 4.7M ± 5%	Allen Bradley Type CB	403/4/04361/470
R8	Resistor Variable 1k	Allen Bradley Type 90H	404/9/05047/003
R43	Resistor Variable 2.2k	Allen Bradley Type 90H	404/9/05047/011
D13-16	Diode	1R Type 10D1	415/4/98088/001
D21-24,27, 28,30,32-34	Diode	Texas 1N4148	415/4/05720
D29,17,19	Diode	Texas 1N4001	415/9/98466/001
D26	Diode Zener	Mullard BZY88C6V8	415/4/02792/011
D25	Diode Zener	Mullard BZY88C12	415/4/02792/017
TR3,4,6,7	Transistor	Mullard BC107	417/4/01777
TR8,9	Transistor	Mullard BC179	417/4/01860
TR10,11	Transistor	Motorola MPSA43	417/4/01878
TR1,5	Transistor	Motorola MPSU60	417/4/01879

Heatsink Component Assembly (630/1/32958)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Heatsink Assembly	Redpoint Type 6Q	630/1/33024
-	Cover	Plessey	630/2/33025
-	Nut Caged Lug Double	Spire SM/G/03/0/71/44/6	991/4/11739/001
-	Terminal Lug	Tucker G369-4	703/9/98048/018
-	Terminal Lug	Tucker S88-6BA	703/9/98756/002
IC1	Integrated Circuit	Motorola MC7812CK	445/4/10366/004
IC2	Integrated Circuit	Motorola MC7815CK	445/4/10366/005
TR2	Transistor	Texas 2N3055	417/9/98431/001
C5,6,7,8	Capacitor 1uF ± 20% 35V	Siemens V32560	402/4/55748/001

Heatsink Assembly (630/1/33024)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Heatsink Electric	Redpoint Type 6Q	418/4/42252/004

Heatsink Component Assembly (630/1/32969)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Bush	Jermyn A1201	999/9/02931
-	Insulator Washer	Jermyn A26-3027	703/4/06562
REC1,2,3	Rectifier Bridge	Semtec SCAJ1	415/9/98914/007
IC3,4	Integrated Circuit	Motorola MC7808CP	445/9/01730/003

Heatsink Assembly (630/1/32968)

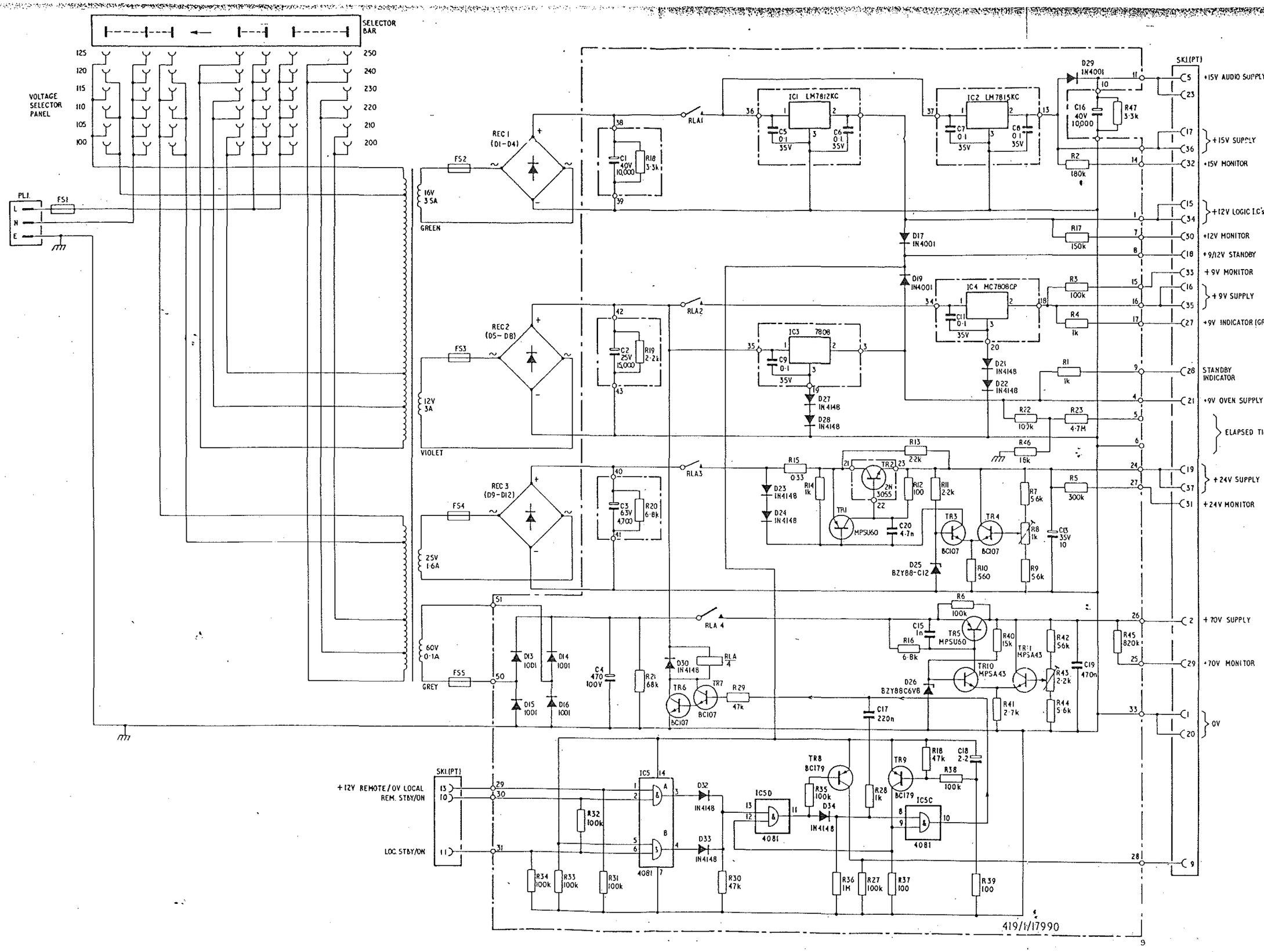
Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Heatsink Electric	Redpoint 6M-1 Natural	418/4/44460/008

Chassis Components

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Spacer Threaded	Plessey	630/2/31526/004
-	Clamp	Plessey	630/2/32963

Chassis Components (Cont'd)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Label	Plessey	630/2/34137
-	Nut Thumb	Plessey	630/2/32967
TB1,2	Terminal Block	Klippons Mk2-12	703/4/03801/001
-	Panel Voltage Selector	McMurdo Type V279002/2	508/9/20409
PL1	Plug Electrical Fixed	Belling Lee L2132C/L	508/4/22263
SK8	Socket Electrical Fixed	Cannon 7443 DCF-375	508/4/28180/002
FS1,2,3, 4,5	Fuseholder	Belling Lee L2006A	516/4/00452
-	Carrier Cartridge Fuse Link	Belling Lee	516/4/98084/001
FS5	Fuse Link (Slow Blow) 0.1 Amp	Belling Lee L2081/100	518/4/90461/001
FS4,1 (240V)	Fuse Link (Slow Blow) 1 Amp	Belling Lee L2081/1	518/4/90461/002
FS1 (110V)	Fuse Link (Slow Blow) 2 Amp	Belling Lee L2081/2	518/4/90461/003
FS2,3	Fuse Link 3 Amp	Belling Lee L1427/3.15	508/4/90462/001
T1	Transformer	Avel Lindberg Pt. No. 40/2611	405/9/14466
C1,16	Capacitor 10,000uF 40V DC	Erie Type 32107-100-0103-OT-04	402/4/57059/006
C2	Capacitor 15,000uF 25V DC	Erie Type 32107-100-0153-OT-0250	402/4/57060/006
C3	Capacitor 4,700uF 63V DC	Erie Type 32107-100-0472-OT-0630	402/4/57061/008
C9,11	Capacitor 100nF 35V DC	Siemens B32560	402/4/55748/001
R19	Resistor 2.2k ± 2% 0.25W	Electrosil TR4	403/4/05523/220
R18,47	Resistor 3.3k ± 2% 0.25W	Electrosil TR4	403/4/05523/330
R20	Resistor 6.8k ± 2% 0.25W	Electrosil TR4	403/4/05523/680
-	Cable Tie	Insulok Type T1812	915/4/98775/000
-	Sleeve Indent Black 0	Hellerman	915/4/04042/000
-	Sleeve Indent Brown 1	Hellerman	915/4/04042/001
-	Sleeve Indent Red 2	Hellerman	915/4/04042/002
-	Sleeve Indent Orange 3	Hellerman	915/4/04042/003
-	Sleeve Indent Yellow 4	Hellerman	915/4/04042/004
-	Sleeve Indent Green 5	Hellerman	915/4/04042/005
-	Sleeve Indent Blue 6	Hellerman	915/4/04042/006
-	Sleeve Indent Violet 7	Hellerman	915/4/04042/007
-	Sleeve Indent Grey 8	Hellerman	915/4/04042/008
-	Sleeve Indent White 9	Hellerman	915/4/04042/009
-	Sleeve Indent Black 0	Hellerman	915/4/04042/060
-	Sleeve Indent Brown 1	Hellerman	915/4/04042/061
-	Sleeve Indent Red 2	Hellerman	915/4/04042/062
-	Sleeve Indent Orange 3	Hellerman	915/4/04042/063
-	Sleeve Indent Yellow 4	Hellerman	915/4/04042/064
-	Sleeve Indent Green 5	Hellerman	915/4/04042/065
-	Sleeve Indent Blue 6	Hellerman	915/4/04042/066
-	Sleeve Indent Violet 7	Hellerman	915/4/04042/067
-	Sleeve Indent Grey 8	Hellerman	915/4/04042/068
-	Sleeve Indent White 9	Hellerman	915/4/04042/068



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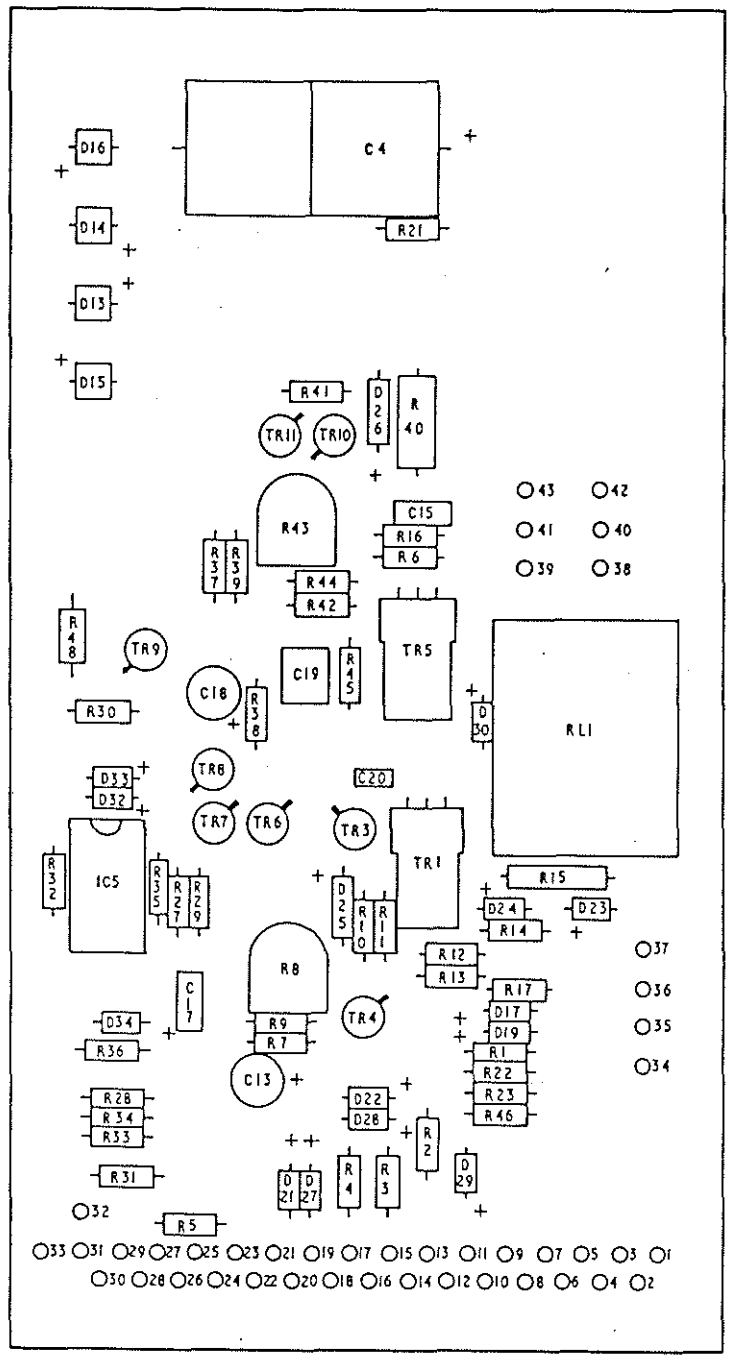
MODULE 8A : POWER SUPPLY CIRCUIT DIAGRAM

FIG 1



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MODULE 8A PANEL COMPONENT LAYOUT

FIG.2

CHAPTER 9

MODULE 9 - SYNTHESISER

CONTENTS

TABLES

ILLUSTRATIONS

ILLUSTRATIONS (Cont'd)

APPENDICES

MODULE 9 - SYNTHESISER

1. INTRODUCTION

Module 9 contains two phase-lock loop controlled oscillator circuits. One produces the fixed-frequency (63.6MHz) 2ND LOCAL OSCILLATOR output, while the other produces the variable-frequency (65 to 95MHz) 1ST LOCAL OSCILLATOR output; this output can be varied in steps of 10Hz.

2. BASIC PRINCIPLES

2.1 The basic phase-lock loop circuit employed is of the form shown in Figure (a). The VFO output frequency is x times the reference frequency, where x is the division ratio of the loop divider circuit. If this division ratio is variable, the output frequency is also variable. The output frequency variation step size is equal to the reference frequency applied to the comparator, and this limits the minimum step size. If, for example, a 10Hz reference frequency were employed then the output frequency could be varied in 10Hz steps. However, the time taken for the loop to 'lock' increases as the reference frequency decreases, so there is a limit to the fineness of the minimum output step from the circuit shown in Figure (a).

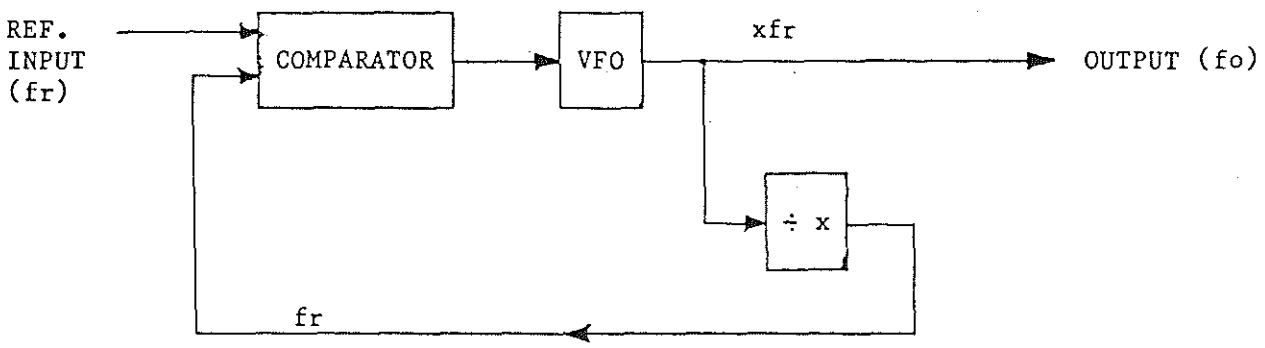


FIG (a) BASIC PHASE-LOCK LOOP

A divider is frequently inserted in the REF. INPUT line to produce a suitable reference input frequency to the comparator.

2.2 Consider the circuit shown in Figure (b), wherein a mixer and a variable divider precede the circuit of Figure (a). The upper side-band output from the mixer is applied to the 'reference' input of the comparator. In Figure (b), let REF.1 be of fixed frequency, and let REF.2 be of variable frequency. Also, let both variable dividers at all times produce identical division ratios.

If both dividers in Figure (b) have a division ratio of x, then the final output frequency (fo) is x times the USB filter output frequency. The USB filter output frequency is:-

$$\text{REF 1} + \frac{\text{REF 2}}{X}$$

therefore the final output frequency fo is

$$x\ (\text{REF 1} + \frac{\text{REF 2}}{X}),\ \text{or}\ x\ \text{REF 1} + \text{REF 2}$$

and can be varied in two ways. Either term x (the divider ratio) or REF. 2 frequency can be varied to change the value of fo.

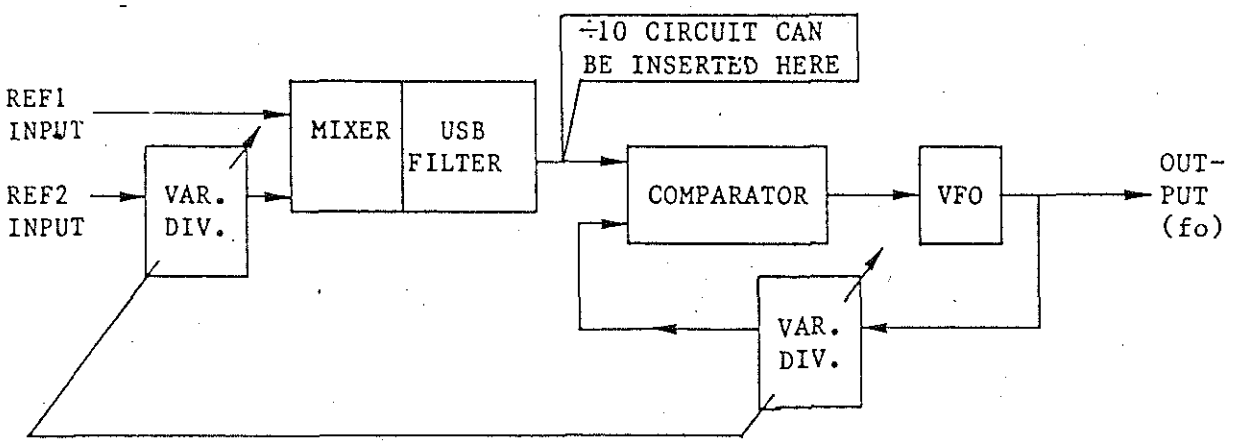


FIG (b) DEVELOPMENT OF FIG (a) CIRCUIT

The following numerical examples will illustrate the action:

(1) REF.1 = 1MHz; REF.2 = 1.1MHz; x = 50

$$fo = 50\ (1+\frac{1.1}{50}) = \underline{51.1MHz}$$

(2) REF.1 = 1MHz; REF.2 = 1.2MHz; x = 50

$$fo = 50\ (1+\frac{1.2}{50}) = \underline{51.2MHz}$$

(3) REF.1 = 1MHz; REF.2 = 1.1MHz; x = 76

$$fo = 76\ (1+\frac{1.1}{76}) = \underline{77.1MHz}$$

i.e. fo = x + REF.2 where REF.1 = 1MHz.

2.4 If the circuit shown in Figure (b) is further modified by the inclusion of a divide-by-ten circuit between the USB filter output and the comparator input, then the output frequency is given by fo = 0.1 (x + REF.2) where REF1 = 1MHz. This arrangement can be used in a cascade loop as shown in Figure (c). The first stage is as shown in Figure (a); the second and third are as shown in Figure (b) with 10 modification, and the fourth is as shown in Figure (b).

2.5 If terms w, x, y, and z of Figure (c) are given values of w = 40, x = 50, y = 60, and z = 70, then the frequencies at points A, B, C, and D in Figure (c) are as follows:-

A = (w x REF.1) = 40 x 1 = 40MHz

B = 0.1 (x + A) = 0.1 (50 + 40) = 9MHz

C = 0.1 (y + B) = 0.1 (60 + 9) = 6.9MHz

fo = D = (z + C) = 70 + 6.9 = 76.9MHz

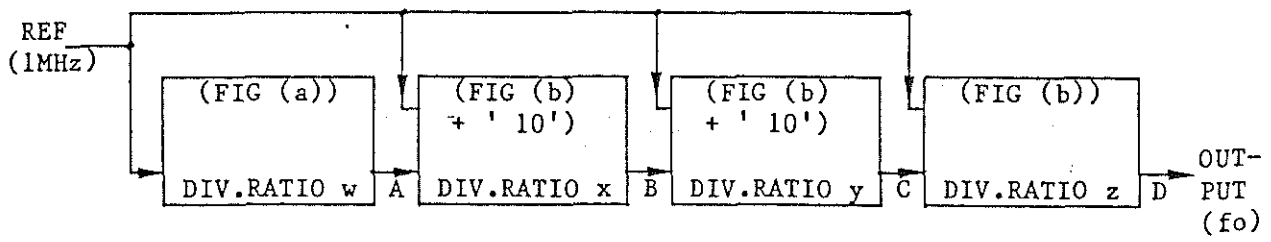


FIG (c) FOUR-TERM CASCADE PHASE-LOCK LOOP

2.6 Table 1 shows the effect of varying terms w, x, y, and z separately. By this method, four division ratio controls (one for each stage) can be calibrated in terms of digits of the output frequency fo. These controls can be further combined by external circuits into one single rotary knob.

TABLE 1 : VARIATIONS OF DIVIDER TERMS

DIVIDER TERM				fo								
				Varied by Term z		Varied by Term y		Varied by Term x	Varied by Term w	
w	x	y	z							
40	50	60	70	7	6	.	9	0	0	MHz
40	50	60	80	8	6	.	9	0	0	MHz
40	50	60	71	7	7	.	9	0	0	MHz
40	50	61	70	7	7	.	0	0	0	MHz
40	51	60	70	7	6	.	9	1	0	MHz
40.5	50	60	70	7	6	.	9	0	5	MHz

2.7 The range of variation of term z is decided by the desired frequency range. The variations of terms y and x are both over a range of ten. In the example given, the variation of term w is over a range of one in steps of 0.1 or less: in a practical circuit, term w is a division ratio of hundreds and therefore would vary over a larger range. The smallest step by which term w can be varied decides the smallest step by which output frequency can be varied, so producing a circuit (Figure (c)) in which fine variations of frequency can be made without incurring the penalty of long ' lock' time.

3. FUNCTIONAL DESCRIPTION

3.1 1st Local Oscillator

3.1.1 The four-term first local oscillator loop in Module 9 can be seen in detailed block diagram form in Figure 1. Term values are:

w : 900 to 999.9 (FINAL LOOP)

x : 81 to 90 (INTERPOLATION LOOP 1)

y : 81 to 90 (INTERPOLATION LOOP 2)

z : 56 to 85 (OUTPUT LOOP)

Variations of term values for given final output frequency shifts are as shown in Table 2.

TABLE 2 : VARIATIONS OF TERM VALUES

	10Hz	100Hz	1kHz	10kHz	100kHz	1MHz	10MHz
w	0.1	1	10	-	-	-	-
x	-	-	-	1	-	-	-
y	-	-	-	-	1	-	-
z	-	-	-	-	-	1	10

The first stage consists of the 'FINAL LOOP' circuit on printed-circuit panels B and C, and is of the form shown in Figure (a). The 1MHz REF input is divided down to 10kHz: this, in conjunction with a Term w division ratio variable between 900 and 999.9 produces a FINAL LOOP output frequency between 9 and 10MHz which can be varied in steps of 100kHz, 10Hz, or 1kHz (equivalent to output A in Figure (c)).

3.1.2 The output from the FINAL LOOP is applied to the second stage, known as INTERPOLATION LOOP 1: this is housed in panels D, E, and F. The circuit is of the form shown in Figure (b) with the addition of a 10 circuit as previously described. The 10 circuit is split into two parts, 2 and 5: the 2 circuit precedes the mixer to produce an input of 1 to 1 mark-space ratio to the mixer. A similar 2 circuit is placed in the divider to mixer input path for the same reason. Term x value is variable between 81 and 90: this, in conjunction with a 9 to 10MHz input from the FINAL LOOP produces an output frequency between 9 and 10MHz. A variation of one in Term x produces an INTERPOLATION LOOP 1 output frequency variation of 100kHz. Variations of FINAL LOOP output frequency are divided by ten and now appear as 10kHz, 1kHz, or 100Hz. The INTERPOLATION LOOP output frequency, therefore, is between 9 and 10MHz, and can be varied in steps of 100kHz, 10kHz, 1kHz, and 100Hz (equivalent to output B in Figure (c)).

3.1.3 The output from the INTERPOLATION LOOP 1 is applied to the third stage, known as INTERPOLATION LOOP 2; this is identical with INTERPOLATION LOOP 1, and is housed on the same three p.c. panels (D, E, and F). A variation of one in Term y produces an INTERPOLATION LOOP 2 output frequency variation of 100kHz. Variations of INTERPOLATION LOOP 1 output frequency are divided by ten, and now appear as 10kHz, 1kHz, 100Hz, and 10Hz. The INTERPOLATION LOOP 2 output frequency, therefore, is between 9 and 10MHz and can be varied in steps of 100kHz, 10kHz, 1kHz, 100Hz, and 10Hz (equivalent to output C in Figure (c)).

3.1.4 The output from INTERPOLATION LOOP 2 is applied to the fourth stage, known as the OUTPUT LOOP: the circuit is of the form shown in Figure (b), and no 10 action occurs. The circuit is housed on

panels G. H, and J. A second ÷10 circuit, placed between the variable divider in panel H and the Phase and Frequency comparator, nullifies the effect of the ÷10 function in the other input line to the comparator. The action therefore becomes the mathematical addition of Term z (MHz) to the output from INTERPOLATION LOOP 2 (MHz). A variation of one in Term z produced a 1MHz output frequency step. The OUTPUT LOOP output frequency, therefore, is between 9 and 10MHz plus the value of Term z, and can be varied in steps of 10MHz, 1MHz, 100kHz, 10kHz, 1kHz, 100Hz, and 10Hz.

3.2 2nd Local Oscillator

3.2.1 The fixed-frequency 2ND LOCAL OSCILLATOR is housed on panels K and L. It consists of a circuit of the form shown in Figure (a) with a divider in the reference input line. An output frequency of 63.6MHz is produced.

3.3 Monitoring

A monitor output is taken from the Phase and Frequency Comparator of each phase-lock loop. An LED indicator is provided for each of the five loops, indicating when it is in lock. When all are in lock, a further LED indicator indicates 'all in lock'. When tuning (i.e. frequency variation) is in progress lock is lost; under these conditions a muting output is produced which shuts down the receiver outputs until lock is acquired on the new tuning setting. The monitoring circuits are housed in panel A.

3.4 Power Regulation

ECL and RTL integrated circuits are used in the Synthesiser because of the high frequencies involved; CMOS circuits cannot operate at such frequencies. This, coupled with the fact that a high degree of decoupling is necessary to avoid spurious outputs from the synthesiser, requires the use of power regulators inside Module 9.

4. CIRCUIT DESCRIPTION - FINAL LOOP

4.1 Introduction

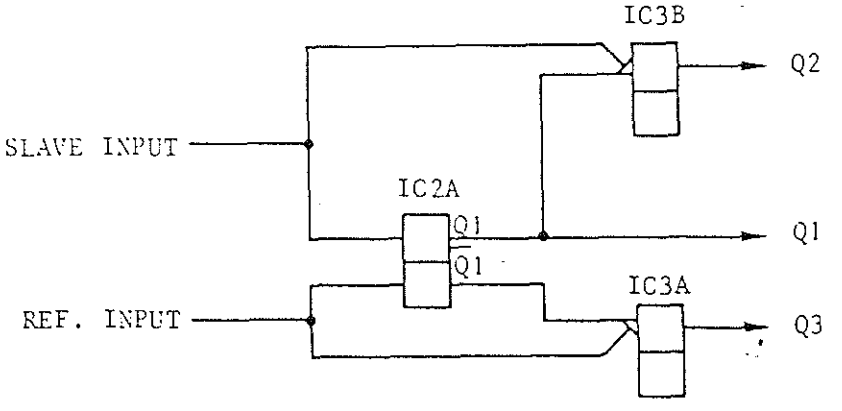
4.1.1 The final loop circuit is housed on printed-circuit panels B (419/1/18041) and C (419/1/18043). The Oscillator, Phase Filter, Phase and Frequency Comparator, and Lock Detector are on panel C, while the Dividers and Code Conversion circuits are on panel B.

4.2 Oscillator (Panel C, Figure 4)

4.2.1 The Oscillator is formed by TR8, TR9, and associated passive components. An output is produced between 9 and 10MHz at a level of 0dBm and at an impedance of 50 ohms, i.e. 2V peak-to-peak (0.67V r.m.s. or 10mW). The tuned circuit is formed by L3, C15, C16, and variable capacitance diode D3. Frequency control is exercised by the d.c. potential applied across D3; 6 volts produces a 9MHz output, while 14 volts produces a 10MHz output. D4 and D5 are connected across the tuned circuit as an amplitude limiter operating at ± 0.6V.

4.3 Phase and Frequency Comparator and Phase Filter (Panel C, Figure 4)

4.3.1 The Phase and Frequency Comparator consists of ICs 1A, 2A, 2B, 3A, and 3B with associated passive components. The basic principle of operation is shown in Figure (d). The fixed reference frequency and the variable slave frequency inputs are applied as trains of short pulses to a set-reset bistable and to the clock inputs of two D-type bistables. The set-reset bistable Q output (Q1 in Figure (d)) is set to '1' by each slave pulse and reset to '0' by the following reference pulse: this produces a variable mark-space ratio output in which the mark-space ratio is proportional to the phase difference between the two inputs. The Q1 output is smoothed and applied to the oscillator as fine frequency control.



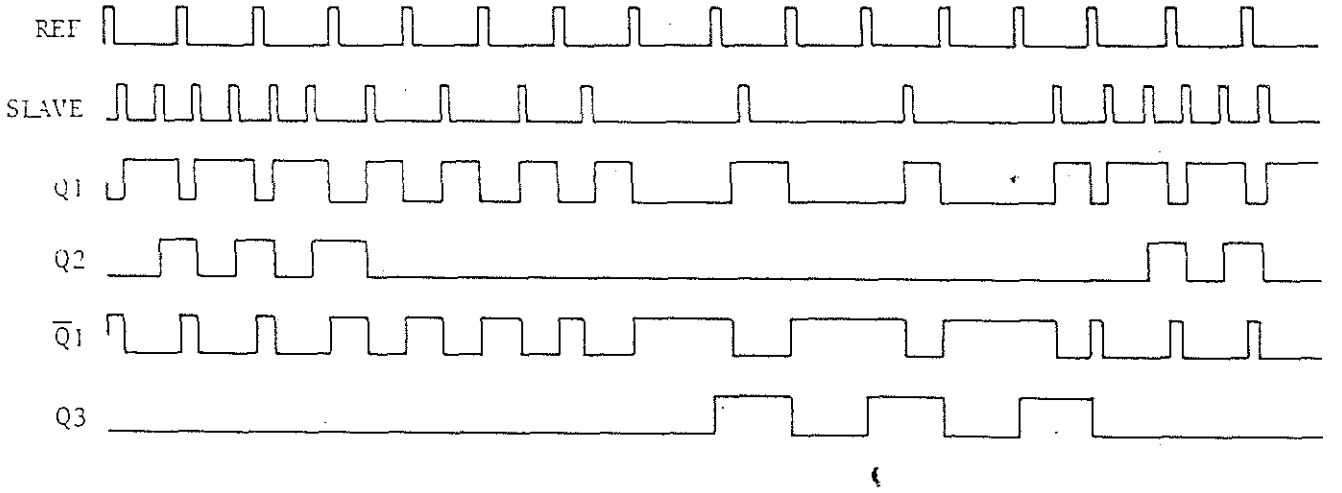


FIG (d) BASIC COMPARATOR ACTION

4.3.2 The Q1 and $\overline{Q1}$ outputs from the set-reset bistable are applied to the D inputs of two bistables which are clocked by the slave and reference inputs respectively. The Q2 (Figure (d)) output will only set to '1' when two or more slave pulses occur in one reference period: similarly, the Q3 (Figure (d)) output will only set to '1' when two or more reference pulses occur in one slave period. The Q2 output, therefore, is only present when the slave frequency rises above about 140% of reference frequency, and the Q3 output is only present when the slave frequency drops below about 70% of reference frequency. Q2 and Q3 outputs provide the coarse control of the associated oscillator.

4.3.3 The inputs to SK1(H) and SK1(15) are not both of the previously described short-pulse form, and are therefore fed to IC2 and IC3 via shaping circuits. IC1A produces CMOS levels and rise times, leaving pulse length unchanged: IC2B is connected as a monostable, and produces CMOS output pulses of 150 nanosec in length. The shaped SLAVE and REF signals form the two inputs to the comparator proper, which comprises IC2 and IC3. The action of the comparator is as shown in Figure (a), with the addition of minimum pulse-length producing circuits (C2, R4: C3, R5) to the outputs of IC3A and IC3B. These ensure that a '1' level at IC3A-Q is maintained for a minimum of 300usec, and that a '1' level at IC3B-Q is maintained for a minimum of 100usec. The two periods are unequal to avoid the possibility of the whole phase-lock loop oscillating in frequency; this point will be expanded later.

4.3.4 The Q outputs from IC3A and IC3B form the coarse tuning control signals. A '1' level at IC3B-Q causes TR5 to conduct (via TR2), so taking current from C14. A '1' level at IC3A-Q causes TR4 to conduct (via TR3), so charging C14. The potential across C14 is fed via R25 and R26 to appear across variable capacity diode D3 in the oscillator tuned circuit.

The variable mark-space ratio output from IC2A-Q is applied to TR6 base. The output from TR6 collector is smoothed by the circuit between TR6 collector and C15, providing a smooth variation of C15 potential which is proportional to fine slave/reference phase variations. The resistor network at TR6 collector produces a non-linear transfer characteristic between mark/space ratio and voltage: this compensates for the non-linear frequency/voltage response of the controlled oscillator. The first part of the smoothing circuit (L1, C9) forms a tuned circuit resonant at 10kHz, rejecting ripple at the frequency of the reference input to the comparator. The second part of the smoothing circuit (L2, C11) is resonant at 1kHz, rejecting ripple at the variable divider sidestep programme frequency: this term will be explained later. Diodes D1 and D2 prevent L2 and C11 from ringing when C14 is suddenly charged by TR4 or discharged by TR5.

4.3.6 As has been explained, if slave and reference frequencies differ widely then either TR4 or TR5 conducts, causing the potential across C14 to rise or fall rapidly. If these rise and fall steps were equal, a loop oscillatory state could commence, as frequency overshoot is inevitable with coarse control. To prevent this, the two minimum pulse-length circuits which control IC3A and IC3B outputs are of unequal time-constants. The coarse control ceases when the oscillator frequency below about 140% of reference frequency and above about 70% of reference frequency: inside these limits, control is exercised by the smoothed output from TR6.

4.4 Power Regulation (Panel C, Figure 4)

4.4.1 Any noise or other transients on the d.c. power supply to TR4, TR5, and TR6 would cause variations in the potential across C15 and would therefore affect oscillator frequency. Inductance-capacity decoupling is therefore fitted on the printed-circuit panel, consisting of L4, C17, C19, and C13. C13 is connected via TR7 so as to multiply its capacity by the gain ( ) of the transistor.

4.5 Lock Indication (Panel C, Figure 4)

4.5.1 The 'loop locked' state is taken as being that in which neither IC3A-Q nor IC3B-Q level is '1'. Under these conditions, both inputs to IC1B are '1' causing TR1 to conduct to illuminate a LED indicator, and also setting IC1D output level to '1'.

4.6 Fixed Divider (Panel B, Figure 3)

4.6.1 The fixed divider circuit consists of IC1, and is clocked by the 1MHz reference signal applied from SK1 (15) via TR1. In this context, IC1 forms a 'divide-by-100' circuit. The input frequency (1MHz) is applied to pin 1, and appears at 100kHz on pin 6. Pin 6 is linked to pin 9, which is the input to the second half of the circuit. An output at 10kHz is produced on pin 14, and is fed via SK1(13) to SK1(15) of panel C as REF.INPUT.

4.7 Variable Divider - Principle of Operation

4.7.1 Consider three counter stages connected in cascade as shown in Figure (e). One output pulse is produced for each 100z pulses applied at the input, giving a division ratio of 100z.

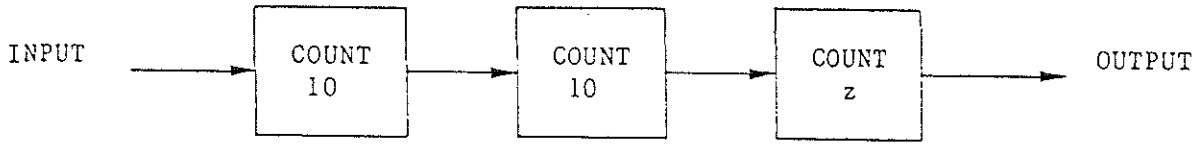


FIG (e) 3-STAGE BASIC COUNTER

The count (or division ratio) of the circuit shown in Figure (e) can be extended if, on production of each output pulse, the first two stages each carry out one extended count. Let these counts be 10+x for the first stage and 10+y for the second stage. The circuit now becomes of the form shown in Figure (f), and produces a count of 100z + 10y + x.

4.7.2 Referring to Figure (f), assume that an output pulse has been produced at point D. This pulse marks the end of a complete count cycle, and acts as an 'extended count' command input to the first two stages. In the next count cycle, the first count of the first stage will be 10+x and the first count of the second stage will be 10+y. Thereafter, the first and second stages will both count in tens until z pulses have been produced at pint C: at this moment another pulse will occur at point D and the complete count cycle will re-commence.

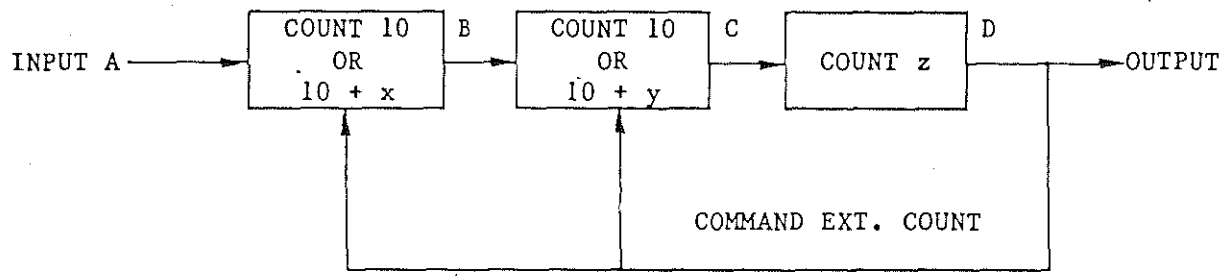


FIG (f) BASIC VARIABLE COUNTER

The action can best be followed from a numerical example, based upon Figure (f), in which x = 5, y = 2, z = 3.

Example

(1) 3 pulses at C produce 1 pulse at D.

(2) 3 pulses at C are produced by 12+10(3-1)=32 pulses at B: extended count = 10+y = 10+2 = 12

(3) 32 pulses at B are produced by 15+10(32-1)=325 pulses at A: extended count = 10+x = 10+5 = 15

(4) If x = 5, y = 2 and z = 3, then 100z+10y+x = 300+20+5 = 325

4.7.3 If terms x, y, and z are made variable, then the device will produce counts of any desired number greater than 100z. Where a fine degree of control is required, a technique known as 'sidestep programme control' is used. Here (referring again to Figure (f)) the value of term x is changed by a small amount for a selected number of complete count cycles in a total of ten, and the mean of the ten counts is taken. If, for example, seven counts of 325 were followed by three counts of 326 (x=6), then the mean count over the ten cycles is:

$$0.1 \quad (325 \times 7) + (326 \times 3) \quad = 325.3$$

The increase of 1.0 in Term x has effectively become an increase of 0.1: the value of 0.3 has been obtained by 'sidestepping' three counts.

4.7.4 In a practical circuit, the output pulse-length is too great to allow it to be directly fed back as command. Two controls, 'Recognition' and 'Reset' are employed. The arrangement can be seen in Figure (g).

4.7.5 When the final stage of the circuit shown in Figure (g) produces an output pulse (which is not used) it also produces a 'Recognition' pulse which is fed back to the second stage; the second stage accepts it as a command to produce one extended count. During the extended count, the second stage applies a 'Recognition' pulse to the first stage and also produces a 'Reset' pulse which terminates the 'Recognition' output from the third stage. The first stage responds in similar fashion to the 'Recognition' output from the second stage,

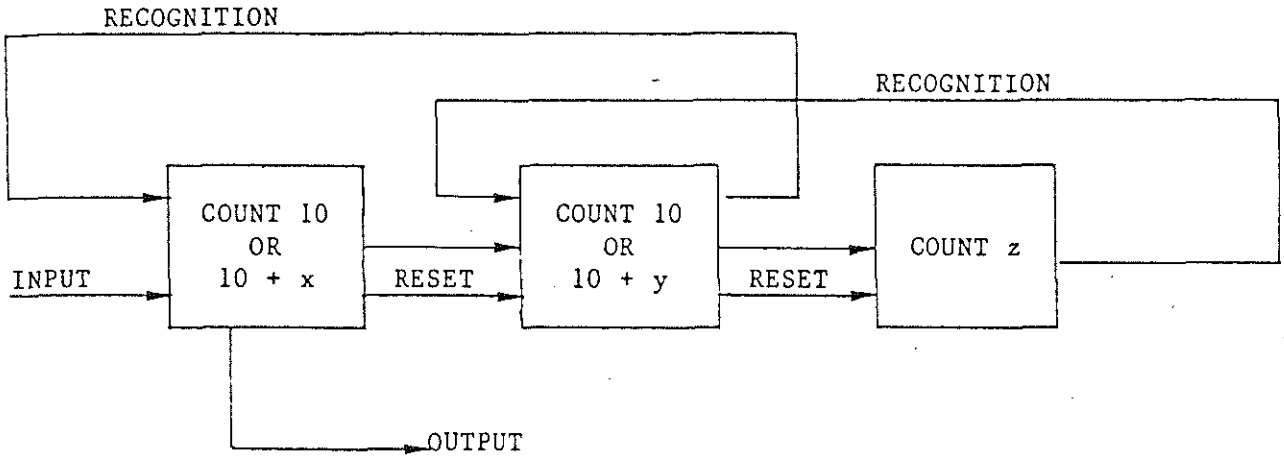


FIG (g) PRACTICAL CIRCUIT

producing an extended count and terminating the second stage 'Recognition' output. A narrow 'Output' pulse is produced once per complete count cycle by the first stage each time a 'Recognition' input is applied to it: this pulse is taken as the final output from the circuit.

4.8 Variable Divider Circuit (Panel B, Figure 3)

4.8.1 The Variable Divider is housed on Panel B, and is made up of IC3, IC4, and IC7. Counts (division ratios) from 900 to 999.9 can be obtained. Term x is generated in IC2 and is applied to IC3. Term y is generated in IC6 and is applied to IC4. Term z is fixed. Term x can be further varied by the sidestep programme generated in IC5, which permits variation of the mean count over ten cycles is steps of 0.1. Essential operating waveforms can be seen in Figure (h).

4.8.2 First Stage.

4.8.2.1 The output from the 9-10MHz oscillator on Panel C is applied from SK2 (3) via TR2 and TR3 to clock IC3. When the 'REC' input to IC3 pin 6 is '0', one '1-0-1' 'CARRY' pulse is produced at IC3 pin 5 for every tenth applied 'REC' pulse. 'CARRY' pulses are two clock periods in length. No other outputs are produced by IC3, and the inputs to pins 11, 10, 2, and 3 which determine the value of term x have no effect. This sequence is known as the 'divide-by-ten' phase of operation.

4.8.2.2 A 'recognition and reset' phase of operation occurs each time a '1' level is applied to the 'REC' input, provided that at least one divide-by-ten operation occurs between successive 'REC' input '1' levels. A '0-1-0' 'COUNT' output pulse of one clock-period duration is generated four clock-periods after the REC input level is set to '1'. A '0-1-0' RESET output pulse of one clock-period duration is generated SIX clock-periods after the REC input is set to '1'.

The extended count occurs during the 'recognition and reset' phase of operation: the value of the extension (term x) is set by the levels of the inputs to IC3 pins 11, 10, 2, and 3, as shown in Table 3.

TABLE 3 : IC3 INPUT LEVELS

TERM x VALUE	Pin 11	Pin 10	Pin 2	Pin 3
0	1	1	1	1
1	0	0	0	0
2	1	0	0	0
3	0	0	0	1
4	1	0	0	1
5	0	1	0	1
6	1	1	0	1
7	0	0	1	1
8	1	0	1	1
9	0	1	1	1

4.8.2.3 'Sidestep' variations of the value of Term x are produced by the levels of the inputs to IC3 pins 7, 12, and 13. In this mode of operation, the CARRY pulse produced during the 'recognition and reset' phase of operation can be displaced by +1 clock-period when pin 12 input level is '0'. Pin 12 level at '1' produces zero sidestep.

4.8.3 Second Stage.

The CARRY output from IC3 is applied as the clock input to IC4. The action of IC4 is very similar to that of IC3: the differences are:

(1) No COUNT output is produced.

(2) No 'sidestep' control is applied.

(3) CARRY output pulses are one clock-period in length.

(4) RESET output pulses are produced 7.5 clock-periods after REC input is set to '1', and are 0.5 clock-period in length.

(5) REC output pulses are produced 7 clock-periods after REC input is set to '1' and are 0.5 to 1 clock-period in length.

(6) The value of the count extension (Term y) is set by the levels applied to pins 12, 11, 2, 3, which correspond to pins 11, 10, 2, and 3 of IC3.

4.8.4 Third Stage.

The CARRY output from IC4 is applied as clock input to IC7, which is a fixed counter producing one REC output pulse for each ninth (z=9) input clockpulse. The REC output pulse is initiated by the '1-0' transition of a '0-1-0' input clockpulse, and is terminated by the '0-1' edge of the RESET input pulse: this pulse must be at least 80 nanosec. in length.

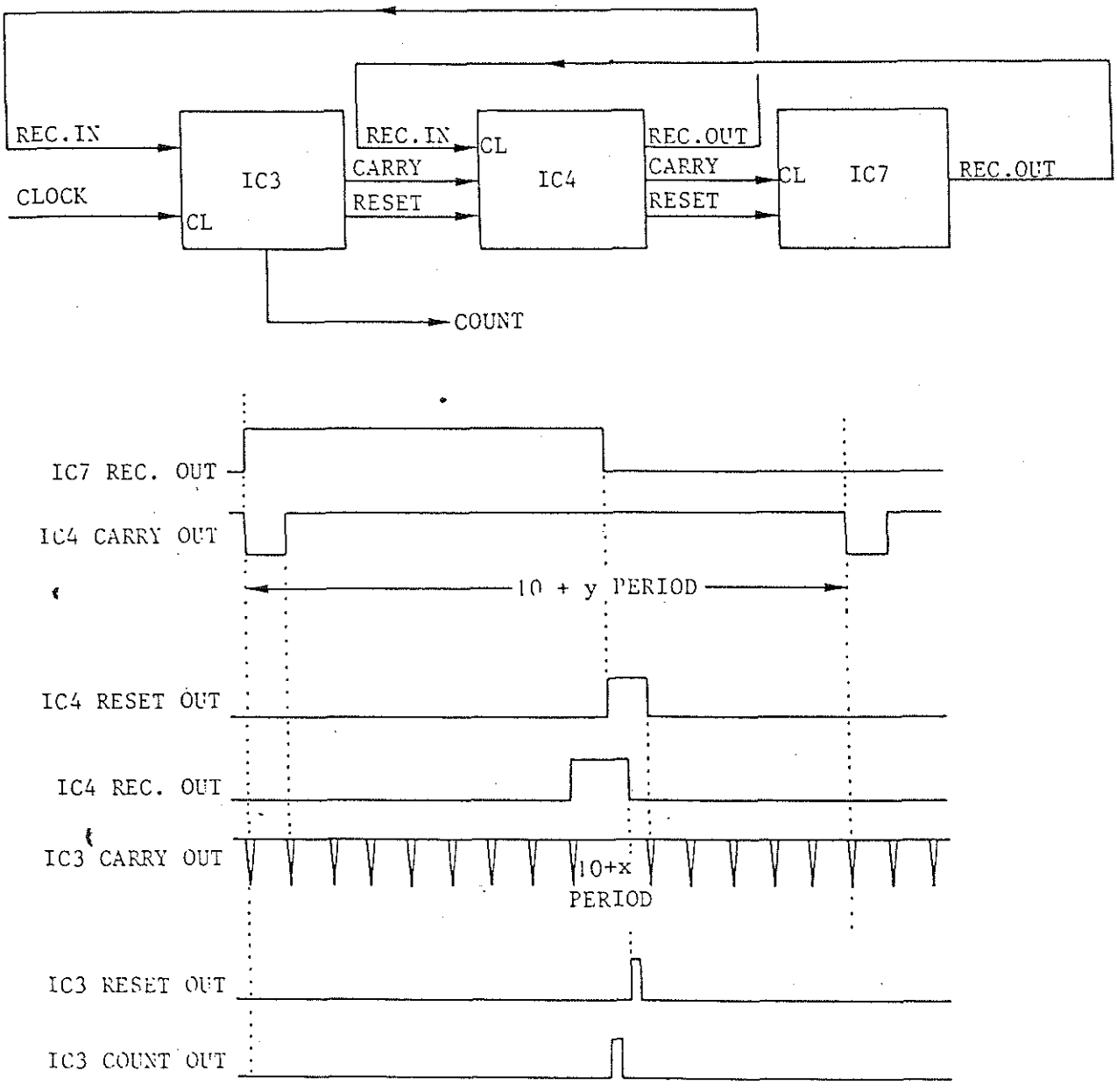


FIG (h) CONTROL OF EXTENDED COUNT BY 'RECOGNITION'

4.9 Control of Divider Term Values (Panel B, Figure 3)

4.9.1 Term Values.

The values of terms x and y are applied to panel B as parallel 4-bit binary numbers. Term x 'units' value is applied to SK1 (P, L, 9, and K). Term x 'tenths' value is applied to SK1 (J, 7, H, and G). Term y 'units' value is applied to SK1 (12, N, 11, and M). The control codes used by IC3 and IC4 are not binary numbers, and therefore modifying circuits are inserted between the inputs from SK1 and the two ICs. Also the 'tenths' value of term x is applied to IC3 by means of a 'sidestep' programme generated in IC5.

4.9.2 Terms x and y 'units' Values.

The circuits generating the x 'units' input to IC3 and the y 'units' input to IC4 are identical. The input binary numbers are fed directly to the A0, A1, A2, and A3 inputs of adders IC2 and IC6, and are also fed in modified form to the B1 and B3 inputs of IC2 and IC6. Mathematically each input from SK1 is a number between 0 and 9: if it is 0, 1, 2, or 3, it is added to 15. If it is 4 or greater, it is added to 5. The action can be seen in Table 4.

TABLE 4 : TERMS x AND y UNITS VALUES

INPUT VALUE	A0	A1	A2	A3	B0	B1	B2	B3	S0	S1	S2	S3
0	0	0	0	0	1	1	1	1	1	1	1	1
1	1	0	0	0	1	1	1	1	0	0	0	0
2	0	1	0	0	1	1	1	1	1	0	0	0
3	1	1	0	0	1	0	1	0	0	0	0	1
4	0	0	1	0	1	0	1	0	1	0	0	1
5	1	0	1	0	1	0	1	0	0	1	0	1
6	0	1	1	0	1	0	1	0	1	1	0	1
7	1	1	1	0	1	0	1	0	0	0	1	1
8	0	0	0	1	1	0	1	0	1	0	1	1
9	1	0	0	1	1	0	1	0	0	1	1	1

4.9.3 Term x 'tenths' Value.

4.9.3.1 As previously described, the 0.1 unit changes to term x are applied to IC3 by the 'sidestep programme' generated in IC5. The value required (in 0.1 unit steps) is applied as a parallel 4-bit binary number between 0 and 9 to IC8 from SK1 (J, 7, H, G): the decimal point is not applied, i.e. an input value of 7 indicates a required change in Term x of 0.7. IC8 is a binary-to-decimal decoder: the binary number applied to the D0, D1, D2, and D3 inputs appears as logic '1' level on the appropriate output, S0 to S9. The gating between the S outputs of IC8 and the A, B, C, and D inputs of IC5 is functionally as shown in Figure (j), and the action can be seen in Table 5.

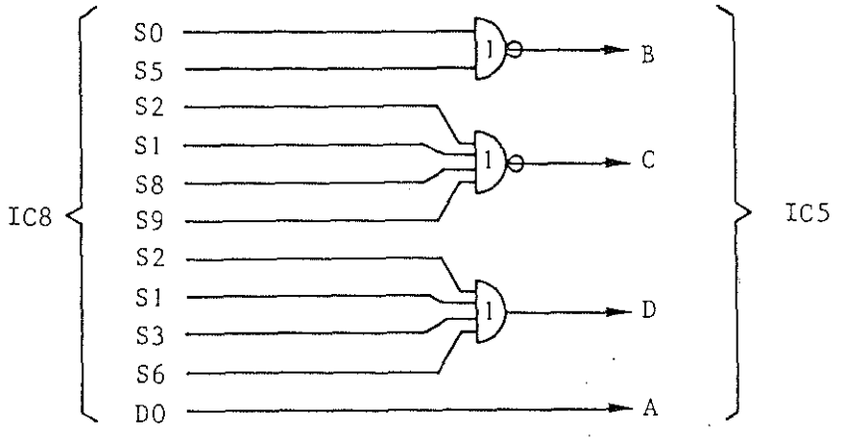


FIG. (j) IC8-IC5 GATING ACTION

TABLE 5 : IC8-IC5 GATING ACTION

D0	D1	D2	D3		A	B	C	D	SIDESTEP
0	0	0	0	S0=1	0	0	1	0	0
1	0	0	0	S1=1	1	1	0	1	1
0	1	0	0	S2=1	0	1	0	1	2
1	1	0	0	S3=1	1	1	1	1	3
0	0	1	0	S4=1	0	1	1	0	4
1	0	1	0	S5=1	1	0	1	0	5
0	1	1	0	S6=1	0	1	1	1	6
1	1	1	0	S7=1	1	1	1	0	7
0	0	0	1	S8=1	0	1	0	0	8
1	0	0	1	S9=1	1	1	0	0	9

4.9.3.2 The outputs corresponding to the values applied to the A, B, C, and D inputs of IC5 are serial ten-bit patterns on IC5 pin 10. Clock rate is one bit per complete count cycle, as IC5 is clocked by the REC output from IC7. The patterns produced are shown in Table 6. The inputs must not change during the pattern period.

TABLE 6 : IC5 PATTERNS

SIDESTEP	A	B	C	D	IC5 PIN 10 PATTERN									
0	0	0	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1	0
2	0	1	0	1	1	1	1	1	0	1	1	1	1	0
3	1	1	1	1	1	1	1	0	1	1	1	0	1	0
4	0	1	1	0	0	0	1	1	1	0	0	1	1	1
5	1	0	1	0	0	1	0	1	0	1	0	1	0	1
6	0	1	1	1	1	1	0	0	0	1	1	0	0	0
7	1	1	1	0	0	0	0	1	0	0	0	1	0	1
8	0	1	0	0	0	0	0	0	1	0	0	0	0	1
9	1	1	0	0	0	0	0	0	0	0	0	0	0	1

4.9.3.3 The number of complete count cycles in which IC5 pin 10 (and IC3 pin 12) level is '0' corresponds to the binary input number. Term x is increased by +1 on each of these cycles. The 'sidestepped' counts are distributed over the ten counts to reduce residual frequency-modulation of the oscillator output.

5. CIRCUIT DESCRIPTION - INTERPOLATION LOOP 1

5.1 Introduction

The Interpolation Loop 1 circuit is housed on printed-circuit panels D D(419/1/18039), E(419/1/18037), and F(419/1/18057). The Oscillator, Phase Filter, Phase and Frequency Comparator, and Lock Detector are on panel F: their action is identical with that of the corresponding Final Loop circuits on panel C and therefore will not be further described. The circuits providing the two inputs to the Phase and Frequency Comparator are on panels D and E.

5.2 First Variable Divider (Panel D, Figure 5)

5.2.1 The 9 to 10MHz output from the Final Loop oscillator is applied from SK2 (A) via buffer/shaper TR6-TR5 to clock the variable divider. The divider is formed by IC4 and IC3, and operates on the same principles as those of the variable divider in the Final Loop. IC3 produces a count of eight and therefore the basic count is 10 x 8 = 80. The extended count of IC4 (10 + x) can be varied between 11 and 20, so giving count values between 81 and 90. Values between 11 and 20 imply term x values between 1 and 10, and these are obtained by the permanent +1 sidestep value produced by the levels to which pins 7, 12, and 13 of IC4 are returned.

5.2.2 The count output is taken via buffer TR4 to clock IC5, which is connected as a divide-by-two circuit producing an output of 1 to 1 mark-space ratio. The Q output from IC5 is applied to driver stage TR2-TR3 to produced one input to the mixer circuit: this input is applied via a 90kHz low-pass filter to the transfer gates IC2A, B, C, and D which form the mixer.

5.3 2 Fixed Divider (Panel D, Figure 5)

The 1MHz REF input is applied via buffer TR1 to clock IC1B, which is connected as a divide-by-two stage producing a 1 to 1 mark-space ratio output. This divider forms the first part of the fixed divide-by-ten function of the loop: the second (5) portion is on panel E. The Q and $\overline{Q}$ outputs are applied to the mixer as anti-phase switching signals.

5.4 Mixer (Panel D, Figure 5)

A mixer circuit of the form shown in Figure (k) is formed by transfer gates IC2A, B, C, and D.

The two conducting elements are switched in anti-phase at 500kHz by IC1B, producing alternating current paths in T1 primary for the output from TR2-TR3. The resultant output from T1 secondary contains both sum and difference frequencies: the sum (USB) is selected by a 550 to 562kHz band-pass filter, and fed to SK3(3) as REF. OUT.

5.5 5 Fixed Divider (Panel E, Figure 6)

The selected upper sideband output from the mixer is taken from SK3(3) of panel D and applied via SK3(A) of panel E to FL1, a 550 to 562kHz band-pass filter. The filter output is fed via buffer/shaper TR5-TR4 to clock IC6, which is a decade counter connected to reset on every fifth applied clock pulse by connecting the Q5 output to the 'Reset' input. The output is taken from Q2 to SK1(13). This 5 divider forms

the second part of the fixed ÷10 function providing one input to the Comparator on panel F.

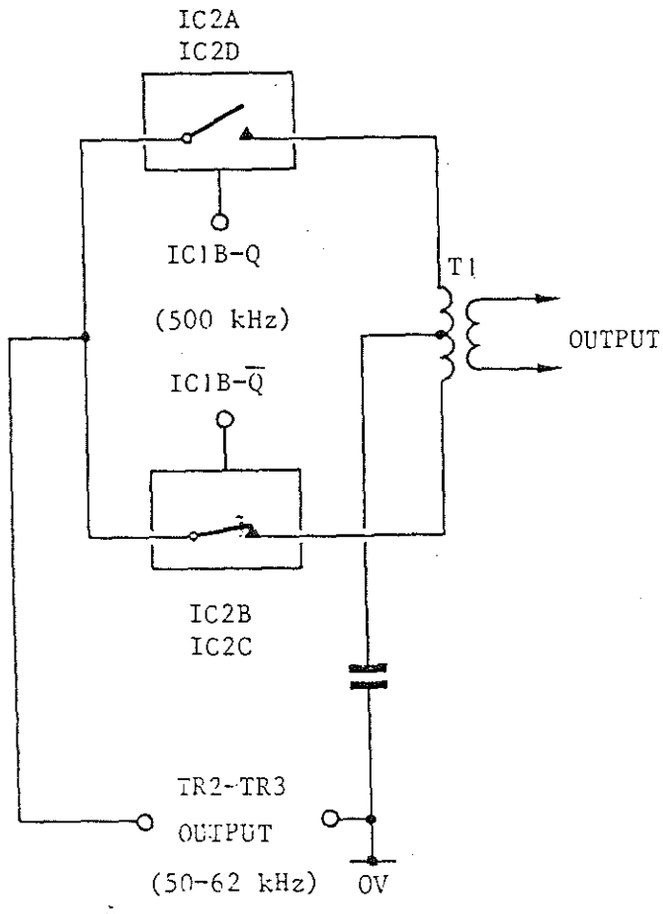


FIG (k) BASIC MIXER CIRCUIT

5.6 Second Variable Divider (Panel E, Figure 6)

The Second Variable Divider on panel E is identical with the First Variable Divider on panel D, and is therefore not further described. On panel E, the COUNT output is taken via TR3, IC1C, and IC1D to provide '1-0-1' SLAVE pulses to the Comparator on panel F.

5.7 Control of Divider Term Values (Panels E and D, Figures 6 and 5)

The control of term values applied to IC3 on panel E and, via SK1(L, K, J, H), to IC4 on panel D is identical with that employed to control the 'units' values applied to IC3 and IC4 on panel B (q.v.). However, a permanent +1 'sidestep' value is applied to IC3 on panel E and to IC4 on panel D by the levels to which pins 7, 12, and 13 of both ICs are returned.

6. CIRCUIT DESCRIPTION - INTERPOLATION LOOP 2

Interpolation Loop 2 is identical with Interpolation Loop 1. The same hardware is used. Loop 2 is therefore not separately described.

7. CIRCUIT DESCRIPTION - OUTPUT LOOP

7.1 Introduction

The Output Loop is housed on panels G(419/1/18055), H(419/1/18035), and J(419/1/18047). It is similar to the two Interpolation Loops and therefore does not require a full separate description. The differences are:

(1) The division ratios of the variable dividers.

(2) The widths of the band-pass filters.

(3) The oscillator circuit.

These parts of the circuit will be fully described.

7.2 Variable Dividers (Panel G, Figure 8 and Panel H, Figure 9)

7.2.1 The second variable divider (panel H) is fed from the oscillator output via a further ÷10 circuit formed by IC3. The input to pin 7 appears at the output of a ÷5 circuit on pin 2, which is connected to the input of a further ÷2 circuit at pin 12. An output at 1/10 input (pin 7) frequency is obtained from pin 15, and is applied via buffer TR4 to clock IC5 of the variable divider.

7.2.2 The divider circuits proper on panels G and H are identical with those of the Interpolation Loops, except that variable term values can be applied to both ICs.

The required count range is from 56 to 85, one unit change causing a 1MHz change in output frequency. A count of 56 indicates 0MHz, i.e. a receiver tuning frequency below 1MHz. Counts of 66 and 76 indicate receiver tuning frequencies of 10MHz and 20MHz respectively. The relationship between the two input 4-bit binary numbers defining (and corresponding to) 'units' and 'tens' of MHz and the count value is therefore not direct. In the 'units' circuit (IC5) the relationship shown in Table 7 applies.

TABLE 7 : IC5 UNITS RELATIONSHIP

INPUT NO(MHz)	0	1	2	3	4	5	6	7	8	9
COUNT VALUE	6	7	8	9	0	1	2	3	4	5

In the 'tens' circuit (IC6) the relationship shown in Table 8 applies.

TABLE 8 : IC6 TENS RELATIONSHIP

INPUT NO(MHzx10)	0	1	2
COUNT VALUE	5 up to 3MHz 6 from 3 to 9MHz	6 from 10 to 13MHz 7 from 14 to 19MHz	7 from 20 to 23MHz 8 from 24 to 29MHz

The parallel 4-bit binary number applied to panel H SK1(12, 19, 15, 7) defines the 'units' value, and the parallel two-bit binary number applied to panel H SK1(Q, 11) defines the 'tens' value. Both inputs must be modified to apply the correct code inputs to IC5 (units) and IC6 (tens) to produce the required count values.

7.2.3 The 'units' input is modified by ICs 8, 9, 7, and 4. The output from IC7, in conjunction with the levels on pins 3 and 7 of IC4, produce a 4-bit input to A0, A1, A2, A3, of IC4 of value 11 for input values to B0, B1, B2, B3, of IC4 of 0 to 6, and of value 1 for input values of 7 to 9.

7.2.4 The A and B inputs of IC4 are added, the sum appearing on S0, S1, S2, S3. These sum values are the required term-defining code input to IC5. The action can be seen in Table 9.

TABLE 9 : IC5 TERM-DEFINING CODES

INPUT	(LSB)			(MSB)	(LSB)			(MSB)	(LSB)			(MSB)	COUNT
VALUE	B0	B1	B2	B3	A0	A1	A2	A3	S0	S1	S2	S3	VALUE
0	0	0	0	0	1	1	0	1	1	1	0	1	6
1	1	0	0	0	1	1	0	1	0	0	1	1	7
2	0	1	0	0	1	1	0	1	1	1	1	1	8
3	1	1	0	0	1	1	0	1	0	1	1	1	9
4	0	0	1	0	1	1	0	1	1	1	1	1	0
5	1	0	1	0	1	1	0	1	0	0	0	0	1
6	0	1	1	0	1	1	0	1	1	0	0	0	2
7	1	1	1	0	1	0	0	0	0	0	0	1	3
8	0	0	0	1	1	0	0	0	1	0	0	1	4
9	1	0	0	1	1	0	0	0	0	1	0	1	5

$$(A1 = A3 = \overline{(B0.B1.B2) + B3})$$

7.2.5 From the input value/count relationships already defined, it can be seen that the 'tens' count produced by IC6 has two values for each value of input to SK1(Q, 11). The lower applies if the 'units' input value is 3 or less, and the higher applies if the 'units' input value is 4 or more. This is achieved by producing the SWA and SWB code inputs to IC6 from a combination of SK1(Q, 11) inputs and the two most significant bits (SK1 (7, 15)) of the 'units' input. When the units input is 3 or less, SK1(7, 15) levels are 0-0; otherwise, they are 1-0 or 0-1.

7.2.6 The term-defining code input to IC6 is produced, in conjunction with the levels to which IC6 pins 3 and 10 are returned, by IC7B, IC8A, IC8B, and IC9. These gates form the function shown in Figure (1).

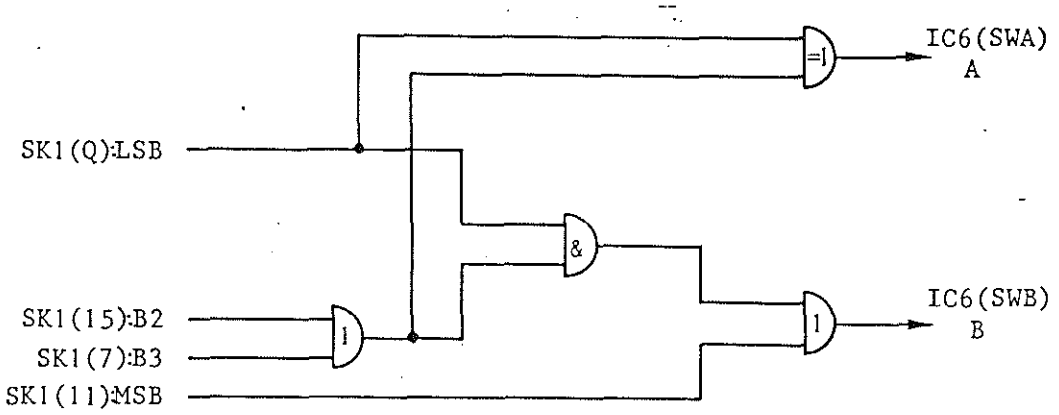


FIG (1) IC6 CODE PRODUCTION

The action over the range of counts can be seen from Table 10. In each 0 to 9 input units cycle, the tens count value is increased by 1 when the input units value is 4 or greater.

TABLE 10 : IC6 CODE RANGE

MHz	COUNT	UNITS TERM	B2	B3	LSB	MSB	A	B	TENS TERM VALUE
0 ⋮ 3	56 ⋮ 59	6 ⋮ 9	0 ⋮ 0	0 ⋮ 0	0 ⋮	0 ⋮	0 ⋮ 0	0 ⋮ 0	5
4 ⋮ 9	60 ⋮ 65	0 ⋮ 5	1 OR 0	0 OR 1	0 ⋮	0 ⋮	1 ⋮ 1	0 ⋮ 0	6
10 ⋮ 13	66 ⋮ 69	6 ⋮ 9	0 ⋮ 0	0 ⋮ 0	1 ⋮	0 ⋮			
14 ⋮ 19	70 ⋮ 75	0 ⋮ 5	1 OR 0	0 OR 1	1 ⋮	0 ⋮	0 ⋮ 0	1 ⋮ 1	7
20 ⋮ 23	76 ⋮ 79	6 ⋮ 9	0 ⋮ 0	0 ⋮ 0	0 ⋮	1 ⋮			
24 ⋮ 29	80 ⋮ 85	0 ⋮ 5	1 OR 0	0 OR 1	0 ⋮	1 ⋮	1 ⋮ 1	1 ⋮ 1	8

7.3 Band-Pass Filters (Panels G and H, Figures 8 and 9)

The bandwidths of FL1 on panel G and FL1 on panel H are 553 to 589kHz.

7.4 Oscillator (Panel J, Figure 10)

The 65-95MHz output loop oscillator is formed by TR7, TR8, and associated components. The tuned circuit is formed by L4, D2, D3, and C18. The basic oscillator is a long-tailed pair with the tuned circuit in one half, the output being taken from the other half: the basic configuration is shown in Figure (m).

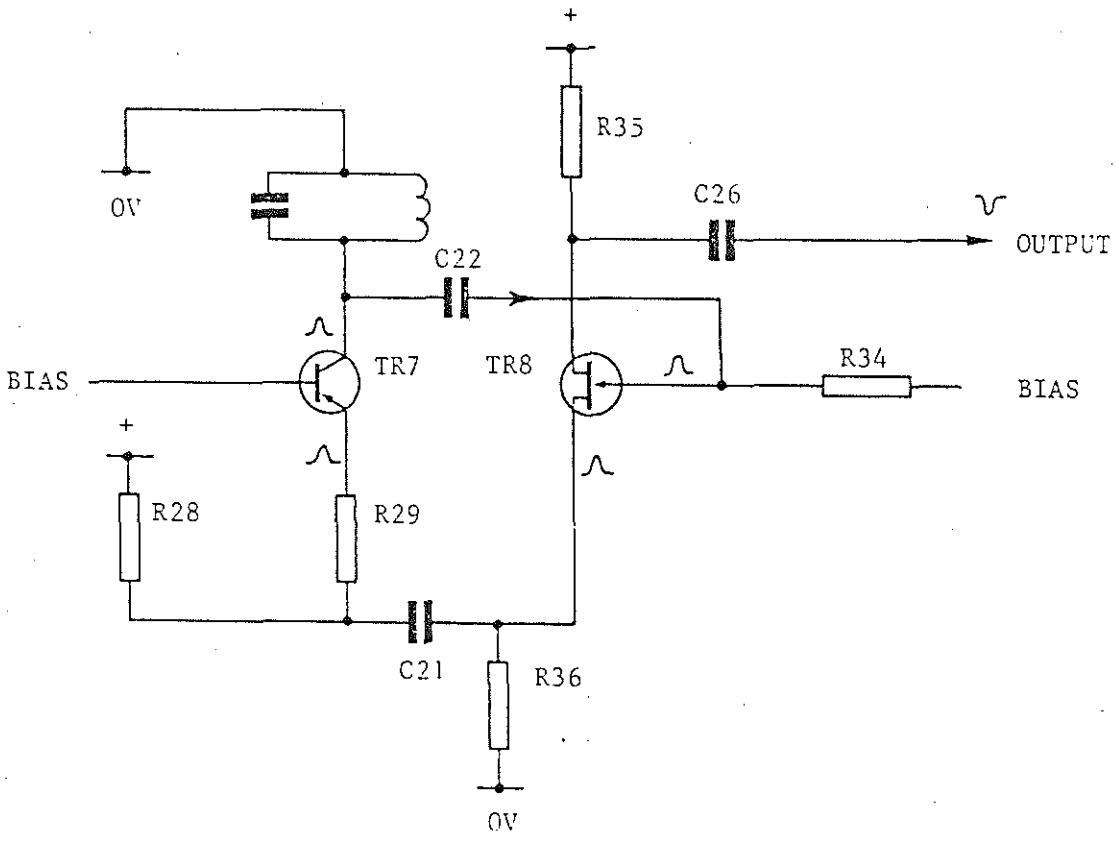


FIG (m) BASIC OSCILLATOR CONFIGURATION

Frequency control is exercised by variable capacitance diodes D2 and D3, as in the preceding oscillator circuits. Amplitude control is exercised by voltage clamp circuit D4-D5. The two diodes conduct only on the peaks of the tuned circuit waveform, and do not affect the level of bias applied to TR7. Output is taken from TR8 drain to provide a degree of isolation, and is fed via buffer stage TR9 to the output amplifiers formed by TR10, 11, 12, and 13.

8. CIRCUIT DESCRIPTION - SECOND LOCAL OSCILLATOR (Panels K and L, Figures 11 and 12)

8.1 Introduction

The Second Local Oscillator is housed on panels K(419/1/18049) and L(419/1/18059). The oscillator, phase filter, and Phase Frequency Comparator are on panel L, while the two fixed dividers are on panel K. An output frequency of 63.6MHz is produced. Panel L is almost identical with panel J of the Output Loop, and therefore will not be further described.

8.2 Fixed 40 Divider (Panel K, Figure 11)

The 1MHz REF. input is applied from SK1(15) via level-changer TR4 to a 4 circuit formed by IC4B and IC4A. The 250kHz output clocks 10 circuit IC5, the output from which is a 25kHz square-wave fed to SK1(N).

8.3 Fixed 2544 Divider (Panel K, Figure 11)

8.3.1 This circuit is made up of three dividers in series, having ratios of 16, 3, and 53. The SLAVE input from the oscillator on panel L is applied via SK2(A) and buffer/level changer circuits to clock IC2. The output from IC2 is a square-wave at 1/16th SLAVE frequency, and is applied via ECL-to-CMOS level-changer TR2-TR3 to a conventional 3 circuit formed by IC3B and IC3A. The Q output from IC3A, at 1/48th SLAVE frequency, clocks the 53 circuit formed by IC8, IC9B, IC9A, IC6B, and associated gates.

NOTE. The following text should be read in conjunction with waveform diagram Figure (n).

8.3.2 The 53 circuit produces one '1-0-1' output pulse from IC6B-Q for every 53 clockpulses applied to pin 6 of IC8. The output pulses are one clock period in length. The basic count of IC8 is sixteen; the 53 value is made up of three counts of sixteen and one count of five.

8.3.3 If the 'CASCADE' and 'ENP' inputs to IC8 are both '0', then the only used output produced by IC8 is Q3, a square-wave at 1/16th clock frequency. Q0, Q1, Q2, and Q3 together produce parallel 4-bit counts down from 15 to 0. If 'CASCADE' is '1', a '0-1-0' pulse is produced at '0' on each count of 0. Application of a '1' level to 'ENP' sets the four Q outputs to a value of 3 (Q0 = P0, Q1 = P1, Q2 = P2, Q3 = P3): when 'ENP' levels returns to '0' a count down from 3 to 0 takes place.

8.3.4 The 'CASCADE' and 'ENP' inputs to IC8 are produced from the '0' and 'Q3' outputs of IC8. 'ENP' is produced by IC6B, and 'CASCADE' is produced by IC9B and IC9A together with gates IC7C and IC7D.

8.3.5 IC9B and IC9A form a 4 circuit which is clocked by IC8 Q3 output and is reset by the 'ENP' output from IC6B-$\overline{Q}$. The 'CASCADE' output level from IC7D sets to '1' on the third 0-1 clock transition after application of 'ENP', and returns to '0' on application of the next 'ENP' pulse. The 'ENP' pulses are '0' output pulses from IC8 which have been retimed in IC6B.

8.3.6 Assume as a start point that 'CASCADE' (IC7D pin 11) level is '1' and that IC8 is at count 1 of a count from 15 to 0. At count 0 a '0' output is produced and is retimed to IC8 clock by IC6B. The retimed pulse, one clock period long, is applied to IC8 as 'ENP' and to IC9B and IC9A as reset. The reset input to IC9B and IC9A terminates the 'CASCADE' pulse by setting IC9A-Q level to '1'. The 'ENP' input to IC8 sets the Q outputs to a value of 3, from which the next count-down starts.

8.3.7 At the end of the count-down from 3 to 0, three count-downs from 15 to 0 take place: at the commencement of each, IC8-Q3 level sets to 1, returning to logic 0 on count 8. IC8-Q3 output clocks IC9B. On the third 0-1 transition from IC8-Q3, 'CASCADE' sets to '1'. At the end of the third 15-0 count a '0' output pulse is produced and the cycle recommences. The period between '0' pulses from IC8 is three times 16 plus the preset value of three plus the two clock periods occupied by the '0' and 'ENP' pulses, i.e. (3 x 16) + 5 = 53 clock periods.

The SLAVE OUT output to SK1(H), i.e. SLAVE IN ÷2544, is taken from IC6B-Q via monostable IC6A.

9. CIRCUIT DESCRIPTION - LOCK INDICATOR

9.1 Introduction

The Lock Indicator circuits are housed in panel A(419/1/18045). The lock states of all four synthesiser loops are sensed in conjunction with the state of the receiver manual tuning control. Two outputs are produced:

(a) Illumination of an LED when all loops are locked.

(b) Muting of Module 5 when out of lock.

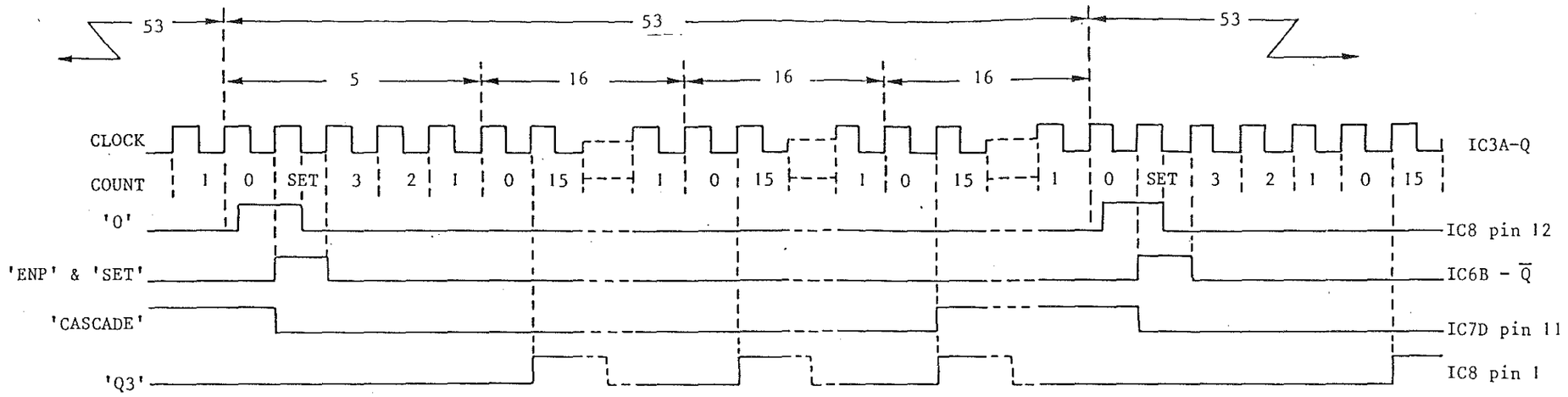
In addition to the circuits on panel A, the synthesiser power regulator panel carries five LED indicators, one for each loop. These indicate individual loop states, and are provided for servicing purposes.

9.2 Lock LED Circuit (Figure 2)

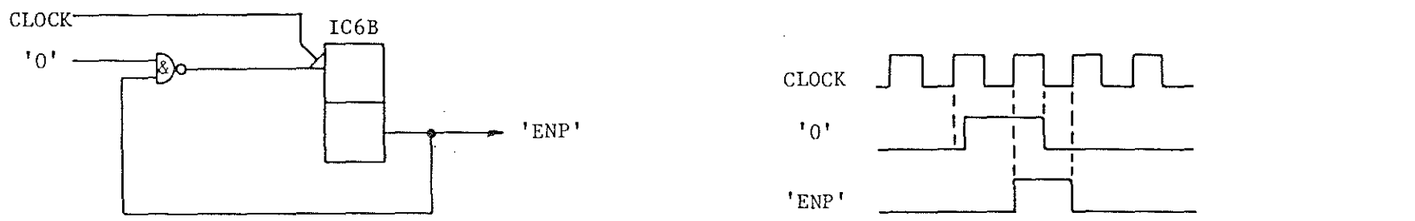
The lock LED circuit senses the states of all five synthesiser loops. These inputs are applied to SK1(N, M, 12, 13, and 9). A '1' level indicates 'in lock' in each case. IC1A, IC1B, and IC2A form a five-input AND function, the output of which is fed to IC4A and to the '1-0' trigger input of IC5B. When all loops are in lock, the '1' level at IC2A output in conjunction with the static $\overline{Q}$ '1' level from IC5B renders TR1 conducting, so illuminating the front-panel 'LOCK' LED connected to SK1(K). If one or more loops fall out of lock, IC2A output level changes to '0': a nominal 100mS '1-0-1' pulse is produced on IC5B-$\overline{Q}$, so holding IC4A output level at '1' for at least 100 mS. If the out of lock situation lasts for more than 100mS, IC2A '0' output level maintains IC4A output at '1' until lock is restored. A '1' level at IC4A output shuts down TR1, so extinguishing the 'LOCK' LED.

9.3 'Mute' Circuit (Figure 2)

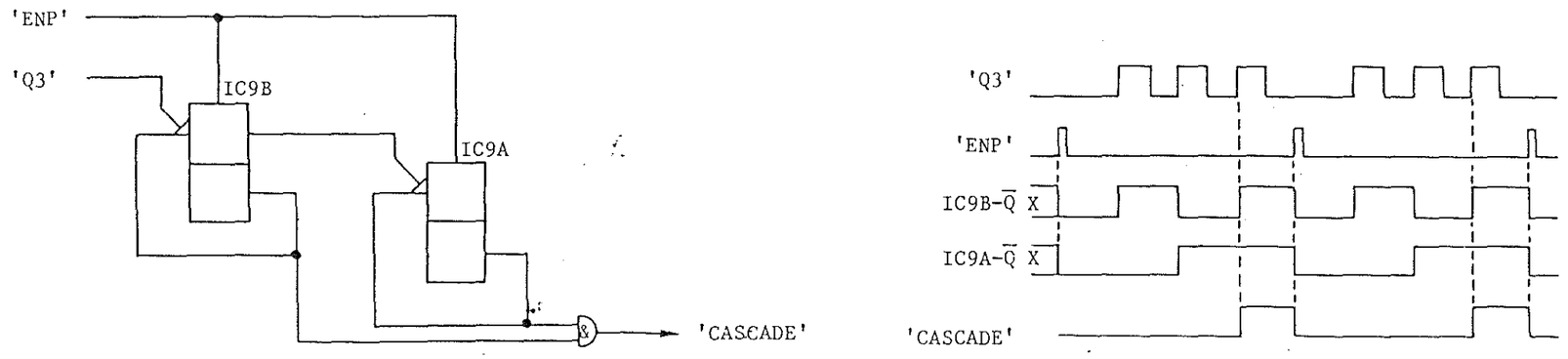
The 'mute' circuit senses the lock states of all five synthesiser loops and the state of the receiver manual tuning control. The 'Final' loop is sensed on two lines, $\overline{\text{UP}}$ FINAL and $\overline{\text{DOWN}}$ FINAL. These indicate



(a) ÷ 53 ACTION



(b) 'ENP' PULSE PRODUCTION



(c) 'CASCADE' PULSE PRODUCTION

FIG.(n) WAVEFORM DIAGRAM FOR 2544 DIVIDER

whether 'Final' loop frequency is high or low relative to the lock frequency. UP/DOWN indicates whether the receiver manual tuning control is rotating to increase or to decrease frequency. When rotation ceases, the UP/DOWN level remains unchanged until rotation in the opposite direction commences.

The sensing inputs are applied to SK1(N, M, 12, 13, 11, L, and 10). IC1A, IC2B, IC2D, IC2C, and IC3B form the logic function shown in Figure (p).

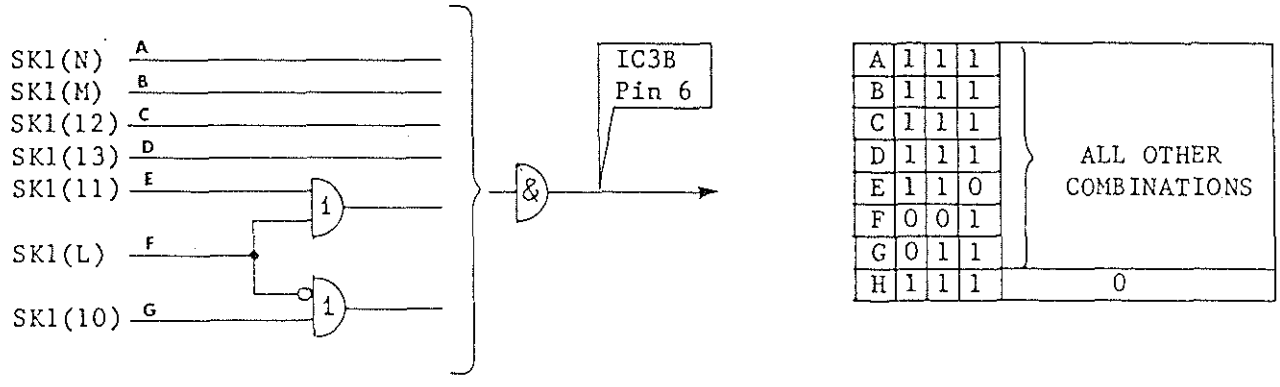


FIG (p) MUTING LOGIC

The combinations of input levels shown in Figure (p) are those which do not produce a muting output, i.e. SK1(H) level is '0' and SK1(J) level is '1'. Any other combination of input levels will produce a muting output, i.e. SK1(H) level is '1' and SK1(J) level is '0'. The action of IC5A is identical with that already described for IC5B, except that the 'minimum period' set by IC5A is nominally 20mS.

10. TEST DATA

The procedure outlined in the following paragraphs forms a complete test procedure and need not be used to locate individual faults. In order to carry out this procedure it is necessary to use the special Test Set supplied by the manufacturer. Do not attempt any adjustment or tests without this equipment.

10.1 Test Equipment

The following items of test equipment are required:

Test Set (special to type) Plessey part no.630/1/35049

Oscilloscope (general purpose)

Extender Card (special to type) Plessey part no.419/1/18069

Digital Voltmeter (DVM)

Counter, 100MHz e.g. Racal 9911

10.2 Alignment and Functional Tests

Remove all the slide in printed circuit panels (A to L) from the module and connect the counter to SKTB on the rear panel of the module. Connect the 1MHz output from the test set to SKTA on the rear panel of the module and also connect to the counter to act as an external reference.

10.2.1 Power Supplies

Connect the module to the Test Set and set the ON/OFF switch to the ON position. Monitor the 9V, 15V, 24V and 70V supplies on the Test Set meter to ensure that the supplies are present. Connect the DVM to pin 13 of the regulator board and adjust R2 to give a 3V $\pm$ 50mV reading on the DVM. Check the following voltages on the regulator board with respect to 0V:

Pin 24 - 6V $\pm$ .3V

Pin 19 - 12V $\pm$ .6V

Pin 7 - 20V $\pm$ .8V

10.2.2 Final Loop

Insert printed circuit panels A and B into the module and panel C via the extender card. Set the frequency on the Test Set to 29.99999MHz and connect the probe of the oscilloscope to the collector of TR6, panel C. Set the frequency on the Test Set to zero (using the FREQUENCY '0'/SETTING switch), C16 on panel C to mid-position and adjust L3 on panel C to give a 20% mark to space ratio display on the oscilloscope. Reset the frequency to 29.99999 (FREQUENCY '0'/SETTING switch to 'SETTING') and adjust C16 for a 80% mark to space ratio on the oscilloscope. Repeat the above test until both conditions are met to within $\pm$ 3%.

(NOTE: The pulse train is at a frequency of 10kHz and the pulse amplitude is approximately 10 and 15V).

Check that D1 on the regulator panel is illuminated. Connect the counter to SKT2 pin 'a' on the rear panel of the module. Set the FREQUENCY '0'/SETTING switch to '0' and check that the frequency is 9.000MHz. Set the switch to 'SETTING' and check that the frequency is 9.999MHz. Remove printed circuit panel C and the extender card from the module and refit panel C into the module.

10.2.3 Interpolation Loop 1

Insert printed circuit panels D, E and, via extender card, F into the first Interpolation Loop position in the module (positions 4D, 5E and 6F). Repeat the procedure in paragraph 10.2.2 adjusting L3 and C16 on panel F as before. Ensure that D2 on the regulator panel is illuminated. Check the frequencies as in paragraph 10.2.2 and note that the respective readings on the frequency counter are 9.0000MHz and 9.9999MHz.

(NOTE: The pulse train frequency is approximately 110kHz).

Remove printed circuit panel F and the extender card from the module and refit panel F into the correct position in the module.

10.2.4 Interpolation Loop 2

Insert the second set of D, E and, via extender card, F into the 2nd Interpolation Loop positions in the module (positions 7D, 8E and 9F). Repeat the procedure in paragraph 10.2.2 adjusting L3 and C16 on panel F as before. Ensure that D3 on the regulator panel is illuminated. Check the frequencies as in paragraph 10.2.2 and note that the respective readings on the frequency counter are 9.0000MHz and 9.9999MHz. Remove printed circuit panel F and the extender card from the module and refit panel F into the correct position in the module.

10.2.5 Output Loop

Insert printed circuit panels G and H into the correct positions in the module. On panel J set R58 fully anticlockwise and then insert into the module, via the extender card, in the correct position. Connect the DVM to the collector of TR16 and adjust R58 to give a reading of +60V $\pm$0.5V. Connect the oscilloscope probe to the collector of TR6 on panel J and, by switching between the '0' and 'SETTING' position on the FREQUENCY switch, adjust L4 such that the Mark-Space and Space-Mark ratios respectively are equal. Check that the ratio of Mark-Space is not more than 19-1 and conversely the Space-Mark ratio. Connect the frequency counter to SKTB and SKTD in turn ensuring that when the frequency switch is in the '0' position the count is 65MHz and in the 'SETTING' position is 94.99999MHz. Check that D4 on the regulator panel is illuminated. Insert panel J into its normal position in the module.

10.2.6 2nd LO Loop

Insert printed circuit panel L into the module. On panel K set R58 fully anticlockwise and then insert into the module via the extender card. Connect the DVM to the collector of TR16 and adjust R58 to give a reading of 18V $\pm$ 0.25V. Connect the oscilloscope probe to TR6 collector and adjust L4 to give a 1:1 Mark/Space ratio, within 10%. Connect the frequency counter to SKTC and E and check that the frequency is 63.60000MHz. Check that D5 on the regulator panel is illuminated.

10.2.7 Lock Indication Lamp

Check that all of the 5 LED's (D1 to D5) are illuminated on the regulator panel for frequency settings of '0' and 29.99999MHz ('0' and 'SETTING' on frequency switch). Check that the green LED indicator marked 'IN LOCK', on the test set, is illuminated.

10.2.8 Mute

Connect the oscilloscope probe to the "MUTE O/P" terminal on the Test Set (this O/P is connected to pin 30 on the synthesiser). Set the frequency on the Test Set to 0.00600MHz, and "UP/DOWN" switch to the 'UP' position. Check that, when the frequency switch is switched alternately between '0' and 'SETTING'. the 'MUTE' pulse only only occurs on the oscilloscope when switching from 'SETTING' to '0'. Check that the 'MUTE' pulse width is 15 to 35mS. Set the "UP/DOWN" switch to the 'DOWN' position and repeat the above test checking that

the 'MUTE' pulse only occurs when switching from 'SETTING' to '0'.

(NOTE: If when switching from '0' to 'SETTING' a spurious pulse is seen repeat the test at another frequency between 3 and 7kHz).

10.2.9 Output Levels

Connect the RF Millivoltmeter, together with the 50 ohm load, to SKTS B, C, D and E in turn. Check that the output levels from these sockets are are between 570 to 880mV. Connect the frequency counter to SKTB and select, in turn, the frequencies shown in Table 1. Check that the counter readings conform to the readings shown in Table 11.

TABLE 11 : OUTPUT FREQUENCY LEVELS

Setting (MHz)	Counter Reading
11.1111	76.1111
22.2222	87.2222
23.3333	88.3333
24.4444	89.4444
25.5555	90.5555
26.6666	91.6666
27.7777	92.7777
28.8888	93.8888
29.9999	94.9999
00.0000	65.0000

Check that all the five 'LOCK' lamps are illuminated for each setting.

10.2.10 'Jitter' Measurement

Connect the 'Spurious Frequency Deviation Meter' and the oscilloscope to SKTB, and measure the peak frequency deviation at the following settings of LO1:

00.00000MHz)
) Reading should
29.99999MHz) be not more
) than 2Hz peak.
13.50000MHz)

Connect the 'Frequency Deviation Meter' and the oscilloscope to SKTC and measure the peak deviation at LO2. The readings should be the same as for LO1.

10.3 The module should be inspected to ensure that no damage has been caused during testing.

11. COMPONENT LISTS

Main Assembly (630/1/32989/001)

Panel Electronic Circuit A (419/1/18045)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Panel Printed Circuit	Plessey	419/2/18046
-	Socket Semi-Conductor	Texas 14L DIL C931402	508/4/22096/002
-	Socket Semi-Conductor	Texas 16L DIL C931602	508/4/22096/003
C1,7,9,10	Capacitor 0.01uF ± 10% 100V	Erie 8121M-X7R	400/4/20673/002
C3,4	Capacitor 0.22uF + 5% 100V	Siemens B32560	435/4/90317/017
C2	Capacitor 10uF ± 20% 16V	ITT Tag	402/4/57057/008
C5	Capacitor 10uF ± 20% 35V	ITT Tag	402/4/57057/006
C6	Capacitor 22uF ± 20% 6.3V	ITT Tag	402/4/57057/012
C8	Capacitor 22uF ± 20% 16V	ITT Tag	402/4/57057/009
IC2	Integrated Circuit	Motorola MC14001CP	445/4/02383/001
IC4	Integrated Circuit	Motorola MC14011CP	445/4/02283/011
IC1	Integrated Circuit	Motorola MC14012CP	445/4/02383/012
IC3	Integrated Circuit	Motorola MC14025CP	445/4/02383/025
IC5	Integrated Circuit	RCA CD4098BE	445/4/02395
R9,10	Resistor 1k + 2% 0.25W	Electrosil TR4	403/4/05523/100
R8	Resistor 2.20k + 2% 0.25W	Electrosil TR4	403/4/05525/220
R1-7,11, 12	Resistor 1M ± 5%	Allen Bradley Type C8	403/4/04361/003
TR1	Transistor	Ferranti ZTX108L	417/4/02039/012
SK1	Socket PV Card	Berg 15-way D/Row 65000-215	508/9/22101/002

Panel Electronic Circuit B (419/1/18041)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Panel Printed Circuit	Plessey	419/2/18042
-	Socket Semi-Conductor	Texas 14L DIL C931402	508/4/22096/002
-	Socket Semi-Conductor	Texas 16L DIL C931602	508/4/22096/003
C12	Capacitor 4.7nF + 10% 100V	Erie 8111M-X7R	400/4/21280/001
C1-3,5,6, 8,9,11	Capacitor 10nF ± 10% 100V	Erie 8121M-X7R	400/4/20673/002
C4,10	Capacitor 10uF ± 20% 16V	ITT Tag	402/4/57057/008
C7	Capacitor 22uF ± 20% 6.3V	ITT Tag	402/4/57057/012
L1	Inductor 4.7uH ± 10%	Sigma SC10	406/4/31749/001
IC10	Integrated Circuit	Motorola MC14001CP	445/4/02383/001
IC2	Integrated Circuit	Motorola MC14008CP	445/4/02383/008
IC9	Integrated Circuit	Motorola MC14011CP	445/4/02383/011
IC8	Integrated Circuit	Motorola MC14028CP	445/4/02383/028
IC11	Integrated Circuit	Motorola MC14069CP	445/4/02383/069

Panel Electronic Circuit B (Cont'd)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
IC1	Integrated Circuit	Motorola MC14518CP	445/4/02383/518
IC3	Integrated Circuit	Plessey SP8311M	445/4/03085
IC4	Integrated Circuit	Plessey SP8317M	445/4/03037
IC7	Integrated Circuit	Plessey SP8323M	445/4/03083
IC5	Integrated Circuit	Plessey SP8325M	445/4/03089
R1,9,13	Resistor 47R ± 2% 0.25W	Electrosil TR4	403/4/05521/470
R3,4,10	Resistor 470R ± 2% 0.25W	Electrosil TR4	403/4/05522/470
R2,12	Resistor 560R ± 2% 0.25W	Electrosil TR4	403/4/05522/560
R42-53	Resistor 1k ± 2% 0.25W	Electrosil TR4	403/4/05523/100
R6	Resistor 2.2k ± 2% 0.25W	Electrosil TR4	403/4/05523/220
R8	Resistor 3.3k ± 2% 0.25W	Electrosil TR4	403/4/05523/330
R7	Resistor 6.8k ± 2% 0.25W	Electrosil TR4	403/4/05523/680
R14	Resistor 8.2k ± 2% 0.25W	Electrosil TR4	403/4/05523/820
R11	Resistor 10k ± 2% 0.25W	Electrosil TR4	403/4/05524/100
R15-27	Resistor 47k ± 2% 0.25W	Electrosil TR4	403/4/05524/470
R28,29	Resistor 100k ± 2% 0.25W	Electrosil TR4	403/4/05525/100
R5	Resistor 180k ± 2% 0.25W	Electrosil TR4	403/4/05525/180
R30-41,54	Resistor 1M ± 5%	Allen Bradley Type C8	403/4/04361/003
D1-10	Diode	Texas 1N4148	415/4/05720
TR1,3,4	Transistor	Ferranti ZTX314L	417/4/01873
TR2	Transistor	Ferranti ZTX320L	417/4/01874
SK2	Socket PV Card	Berg 3-way D/Row 65000-203	508/9/22101/001
SK1	Socket PV Card	Berg 15-way D/Row	508/9/22101/002

Panel Electronic Circuit C (419/1/18043)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Panel Printed Circuit	Plessey	419/2/18044
-	Screen Box	Plessey	630/2/33038/001
-	Screen Box	Plessey	630/2/33038/002
-	Socket Semi-Conductor	Texas 14L DIL C931402	508/4/22096/002
C6	Capacitor 15pF ± 5% 100V	Erie 8121M-100-COG	400/4/30011/105
C2,3,20	Capacitor 1nF ± 10% 100V	Erie 8121M-100-X7R	400/4/20673/001
C18,19,21	Capacitor 10nF ± 10% 100V	Erie 8121M-X7R	400/4/20673/002
C9	Capacitor 4.7nF ± 2.5% 30V	Suflex HSC30	437/4/30011/105
C15	Capacitor 4.7nF ± 5% 400V	Siemens B32560-250V	435/4/90317/027
C11	Capacitor 47nF ± 2% 160V	Wima Tropyfol M Series	435/4/98018/054
C1,7,10, 12	Capacitor 0.1uF ± 5% 100V	Siemens B32560-100V	435/4/90317/014
C14	Capacitor 0.22uF ± 5% 100V	Siemens B32560-100V	435/4/90317/017
C4	Capacitor 2.2uF ± 20% 35V	ITT Tag	402/4/57057/004
C5,22	Capacitor 10uF ± 20% 16V	ITT Tag	402/4/57057/008
C8,13,17	Capacitor 10uF ± 20% 35V	ITT Tag	402/4/57057/006
C16	Capacitor Variable 5-60pF	Mullard 80801001	401/4/32132/001
L4,5	Inductor 100uH ± 10%	Sigma SC30	406/4/31753/036

Panel Electronic Circuit C (Cont'd)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
L1	Inductor 53.8mH	Plessey	406/9/29666/006
L2	Inductor 538mH	Plessey	406/9/29666/007
L3	Inductor 2.4uH	Plessey	406/9/29664/001
IC1	Integrated Circuit	Motorola MC14011CP	445/4/02383/011
IC2,3	Integrated Circuit	Motorola MC14013CP	445/4/02383/013
R7,34,35	Resistor 47R ± 2% 0.25W	Electrosil TR4	403/4/05521/470
R11	Resistor 100R ± 2% 0.25W	Electrosil TR4	403/4/05522/100
R32	Resistor 180R ± 2% 0.25W	Electrosil TR4	403/4/05522/180
R31	Resistor 330R ± 2% 0.25W	Electrosil TR4	403/4/05522/330
R17,33	Resistor 390R ± 2% 0.25W	Electrosil TR4	403/4/05522/390
R6,8,23, 26	Resistor 1k ± 2% 0.25W	Electrosil TR4	403/4/05623/100
R23	Resistor 1.5k ± 2% 0.25W	Electrosil TR4	403/4/05523/150
R21	Resistor 2.2k ± 2% 0.25W	Electrosil TR4	403/4/05523/220
R14	Resistor 2.7k ± 2% 0.25W	Electrosil TR4	403/4/05523/270
R22	Resistor 3.9k ± 2% 0.25W	Electrosil TR4	403/4/05523/390
R16	Resistor 4.7k ± 2% 0.25W	Electrosil TR4	403/4/05523/470
R12,13,20	Resistor 8.2k ± 2% 0.25W	Electrosil TR4	403/4/05523/820
R30	Resistor 15k ± 2% 0.25W	Electrosil TR4	403/4/05524/150
R3,15	Resistor 18k ± 2% 0.25W	Electrosil TR4	403/4/05524/180
R10,19,25	Resistor 33k ± 2% 0.25W	Electrosil TR4	403/4/05524/330
R24	Resistor 82k ± 2% 0.25W	Electrosil TR4	403/4/05524/820
R29	Resistor 100k ± 2% 0.25W	Electrosil TR4	403/4/05525/100
R4,9	Resistor 220k ± 2% 0.25W	Electrosil TR4	403/4/05525/220
R5	Resistor 300k ± 2% 0.25W	Electrosil TR4	403/4/05525/300
R1,2	Resistor 1M ± 5%	Allen Bradley Type C8	403/4/04361/003
D1,2,4-6	Diode	Texas 1N4148	415/4/05720
D3	Diode	Motorola MV2115	415/9/98905/014
TR1-3,6-8	Transistor	Ferranti ZTX108L	417/4/02039/012
TR5	Transistor	Ferranti ZTX302L	417/4/01875
TR9	Transistor	Ferranti ZTX314L	417/4/01873
TR4	Transistor	Ferranti ZTX502L	417/4/01876
SK2	Socket PV Card	Berg 3-way D/Row 65000-203	508/9/22101/001
SK1	Socket PV Card	Berg 15-way D/Row 65000-215	508/9/22101/002

Panel Electronic Circuit D (419/1/18039)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Panel Printed Circuit	Plessey	419/2/18040
-	Socket Semi-Conductor	Texas 14L DIL C931402	508/4/22096/002
C3,5	Capacitor 2.2nF ± 2.5% 30V	Suflex HSC30	437/9/30043/002
C4	Capacitor 3.9nF ± 2.5% 30V	Suflex HSC30	437/4/30011/080
C1,8,10-13	Capacitor 10nF ± 10% 100V	Erie 8121M-X7R	400/4/20673/002
C7	Capacitor 0.22uF ± 5% 100V	Siemens B38560	435/4/90317/017
C2	Capacitor 1uF ± 20% 35V	ITT Tag	402/4/57057/003

Panel Electronic Circuit D (Cont'd)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
C6,14	Capacitor 10uF ± 20% 16V	ITT Tag	402/4/57057/008
C9	Capacitor 22uF ± 20% 6.3V	ITT Tag	402/4/57057/012
L3	Inductor 4.7uH ± 10%	Sigma SG10	406/4/31749/001
L1,2	Inductor 2.7uH ± 10%	Campion 553-3635-42	406/4/31748/042
FL1	Ceramic Filter	Vemitron TL16 x 40-556-1	422/9/07782
IC1,5	Integrated Circuit	Motorola MC14013CP	445/4/02383/013
IC2	Integrated Circuit	Motorola MC14066CP	445/4/02383/066
IC4	Integrated Circuit	Plessey SP8311M	445/4/03085
IC3	Integrated Circuit	Plessey SP8323M	445/4/03088
R7,17,20	Resistor 47R ± 2% 0.25W	Electrosil TR4	403/4/05521/470
R16,21,22	Resistor 470R ± 2% 0.25W	Electrosil TR4	403/4/05522/470
R1,14	Resistor 560R ± 2% 0.25W	Electrosil TR4	403/4/05522/560
R4	Resistor 1.5k ± 2% 0.25W	Electrosil TR4	403/4/05523/150
R5	Resistor 2.2k ± 2% 0.25W	Electrosil TR4	403/4/05523/220
R3,19	Resistor 3.3k ± 2% 0.25W	Electrosil TR4	403/4/05523/330
R18	Resistor 6.8k ± 2% 0.25W	Electrosil TR4	403/4/05523/680
R6	Resistor 8.2k ± 2% 0.25W	Electrosil TR4	403/4/05523/820
R15	Resistor 10k ± 2% 0.25W	Electrosil TR4	403/4/05524/100
R10-13	Resistor 47k ± 2% 0.25W	Electrosil TR4	403/4/05524/470
R2	Resistor 180k ± 2% 0.25W	Electrosil TR4	403/4/05525/180
T1	Transformer	Plessey	406/9/29657/012
TR2	Transistor	Ferranti ZTX302L	417/4/01875
TR1,4,5	Transistor	Ferranti ZTX314L	417/4/01873
TR6	Transistor	Ferranti ZTX320L	417/4/01874
TR3	Transistor	Ferranti ZTX502L	417/4/01876
SK2	Socket PV Card	Berg 3-way D/Row 65000-203	508/9/22101/001
SK1	Socket PV Card	Berg 15-way D/Row 65000-215	508/9/22101/002

Panel Electronic Circuit E (419/1/18037)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Panel Printed Circuit	Plessey	419/2/18038
-	Socket Semi-Conductor	Texas 14L DIL C931402	508/4/22096/002
-	Socket Semi-Conductor	Texas 16L DIL C931602	508/4/22096/003
C12	Capacitor 4.7nF ± 10% 100V	Erie 8111M-X7R	400/4/21280/001
C1-4,6,8, 10,11	Capacitor 10nF ± 10% 100V	Erie 8121M-X7R	400/4/20673/002
C7,9	Capacitor 10uF ± 20% 16V	ITT Tag	402/4/57057/008
C5	Capacitor 22uF ± 20% 16V	ITT Tag	402/4/57057/012
FL1	Ceramic Filter	Vemitron TL16 x 40-556-2	422/9/07782
L1	Inductor 4.7uH ± 10%	Sigma SC10	406/4/31749/009
L2	Inductor 100uH ± 10%	Sigma SC30	406/4/31753/036
IC2	Integrated Circuit	Motorola MC14001CP	445/4/02383/001
IC3	Integrated Circuit	Motorola MC14008CP	445/4/02383/008

Panel Electronic Circuit E (Cont'd)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
IC1	Integrated Circuit	Motorola MC14011CP	445/4/02383/011
IC6	Integrated Circuit	Motorola MC14017CP	445/4/02383/017
IC4	Integrated Circuit	Plessey SP8311M	445/4/03055
IC5	Integrated Circuit	Plessey SP8323M	445/4/03038
R4	Resistor 47R ± 2% 0.25W	Electrosil TR4	403/4/05521/470
R12	Resistor 100R ± 2% 0.25W	Electrosil TR4	403/4/05522/100
R2,5	Resistor 470R ± 2% 0.25W	Electrosil TR4	403/4/05522/470
R7	Resistor 560R ± 2% 0.25W	Electrosil TR4	403/4/05522/560
R16	Resistor 820R ± 2% 0.25W	Electrosil TR4	403/4/05522/820
R26-29	Resistor 1k ± 2% 0.25W	Electrosil TR4	403/4/05523/100
R19	Resistor 1.2k ± 2% 0.25W	Electrosil TR4	403/4/05523/120
R15	Resistor 1.8k ± 2% 0.25W	Electrosil TR4	403/4/05523/180
R14	Resistor 2.2k ± 2% 0.25W	Electrosil TR4	403/4/05523/220
R3	Resistor 3.3k ± 2% 0.25W	Electrosil TR4	403/4/05523/330
R13	Resistor 4.7k ± 2% 0.25W	Electrosil TR4	403/4/05523/470
R20	Resistor 6.8k ± 2% 0.25W	Electrosil TR4	403/4/05523/680
R6,18	Resistor 10k ± 2% 0.25W	Electrosil TR4	403/4/05524/100
R17	Resistor 33k ± 2% 0.25W	Electrosil TR4	403/4/05524/330
R8-11	Resistor 47k ± 2% 0.25W	Electrosil TR4	403/4/05524/470
R21	Resistor 180k ± 2% 0.25W	Electrosil TR4	403/4/05525/180
R22-25,30	Resistor 1M ± 5%	Allen Bradley Type C8	403/4/04361/003
D1	Diode	Texas 1N4148	415/4/05720
TR5	Transistor	Ferranti ZTX108L	417/4/02039/012
TR2,3	Transistor	Ferranti ZTX314L	417/4/01873
TR1	Transistor	Ferranti ZTX320L	417/4/01874
TR4	Transistor	Ferranti ZTX510L	417/4/98309/007
SK2,3	Socket PV Card	Berg 3-way D/Row 65000-203	508/9/22101/001
SK1	Socket PV Card	Berg 15-way D/Row 65000-215	508/9/22101/002

Panel Electronic Circuit F (419/1/18057)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Panel Printed Circuit	Plessey	419/2/18058
-	Screen Box	Plessey	630/2/33038/001
-	Screen Box	Plessey	630/2/33038/002
-	Socket Semi-Conductor	Texas 14L DIL C931402	508/4/22096/002
C6	Capacitor 15pF ± 5% 100V	Erie 8121M-100-C0G	400/4/20672/001
C2,3	Capacitor 220pF ± 5% 100V	Erie 8121M-100-C0G	400/4/20672/003
C18,19,21	Capacitor 10nF ± 10% 100V	Erie 8121M-X7R	400/4/20673/002
C9,11	Capacitor 1nF ± 2.5% 30V	Suflex HSC30	437/4/30011/021
C2	Capacitor 1nF ± 10% 100V	Erie 8121M-100-X7R	400/4/20673/001
C15	Capacitor 4.7nF ± 5% 400V	Siemens B32560-250V	435/4/90317/027
C1	Capacitor 0.1nF ± 5% 100V	Siemens B32560-100V	435/4/90317/014
C14	Capacitor 0.22uF ± 5% 100V	Siemens V32560-100V	435/4/90317/017
C7,10,12	Capacitor 0.01uF ± 5% 400V	Siemens B32560-250V	435/4/90317/029
C4	Capacitor 2.2uF ± 20% 35V	ITT Tag	402/4/57057/004
C5,22	Capacitor 10uF ± 20%	ITT Tag	402/4/57057/008

Panel Electronic Circuit F (Cont'd)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
C8,13,17	Capacitor 10uF ± 20% 35V	ITT Tag	402/4/57057/006
C16	Capacitor Variable 5-60pF	Mullard 80801001	401/4/32132/001
L4,5	Inductor 100uH ± 10%	Sigma SC30	406/4/31753/036
L1	Inductor 2.0mH	Plessey	406/9/29666/001
L2	Inductor 2.09mH	Plessey	406/9/29666/002
L3	Inductor 2.4mH	Plessey	406/9/29664/001
IC1	Integrated Circuit	Motorola MC14011CP	445/4/02383/011
IC2,3	Integrated Circuit	Motorola MC14013CP	445/4/02383/013
R7,34,35	Resistor 47R ± 2% 0.25W	Electrosil TR4	403/4/05521/470
R17	Resistor 56R ± 2% 0.25W	Electrosil TR4	403/4/05521/560
R11,18	Resistor 100R ± 2% 0.25W	Electrosil TR4	403/4/05522/100
R32	Resistor 180R ± 2% 0.25W	Electrosil TR4	403/4/05522/180
R31	Resistor 330R ± 2% 0.25W	Electrosil TR4	403/4/05522/330
R33	Resistor 390R ± 2% 0.25W	Electrosil TR4	403/4/05522/390
R6,8,23,26	Resistor 1k ± 2% 0.25W	Electrosil TR4	403/4/05523/100
R28	Resistor 1.5k ± 2% 0.25W	Electrosil TR4	403/4/05523/150
R21	Resistor 2.2k ± 2% 0.25W	Electrosil TR4	403/4/05523/220
R14	Resistor 2.7k ± 2% 0.25W	Electrosil TR4	403/4/05523/270
R22,25	Resistor 3.9k ± 2% 0.25W	Electrosil TR4	403/4/05523/390
R16	Resistor 4.7k ± 2% 0.25W	Electrosil TR4	403/4/05523/470
R12,13,20	Resistor 8.2k ± 2% 0.25W	Electrosil TR4	403/4/05523/820
R24	Resistor 10k ± 2% 0.25W	Electrosil TR4	403/4/05524/100
R30	Resistor 15k ± 2% 0.25W	Electrosil TR4	403/4/05524/150
R3,15	Resistor 18k ± 2% 0.25W	Electrosil TR4	403/4/05524/180
R10,19	Resistor 33k ± 2% 0.25W	Electrosil TR4	403/4/05524/330
R4,29	Resistor 100k ± 2% 0.25W	Electrosil TR4	403/4/05525/100
R9	Resistor 220k ± 2% 0.25W	Electrosil TR4	403/4/05525/220
R5	Resistor 300k ± 2% 0.25W	Electrosil TR4	403/4/05525/300
R1,2	Resistor 1M ± 5%	Allen Bradley Type C8	403/4/04361/003
D4,5,6	Diode	Texas 1N4148	415/4/05720
D3	Diode	Motorols MV2115	415/9/98905/014
TR1,2,3,6,7,8	Transistor	Ferranti ZTX108L	417/4/02039/012
TR5	Transistor	Ferranti ZTX302L	417/4/01875
TR9	Transistor	Ferranti ZTX314L	417/4/01873
TR4	Transistor	Ferranti ZTX502L	417/4/01876
SK2	Socket PV Card	Berg 3-way D/Row 65000-203	508/9/22101/001
SK1	Socket PV Card	Berg 15-way D/Row 65000-215	508/9/22101/002

Panel Electronic Circuit G (419/1/18055)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Panel Printed Circuit	Plessey	419/2/18056
-	Socket Semi-Conductor	Texas 14L DIL C931402	508/4/22096/002
C3,5	Capacitor 2.2pF ± 2.5% 30V	Suflex HSC30	437/9/30043/002
C4	Capacitor 3.9pF ± 2.5% 30V	Suflex HSC30	437/4/30011/080
C1,8,10-13	Capacitor 10pF +80% -20% 100V	Erie 8121C-100	400/4/19506/002

Panel Electronic Circuit G (Cont'd)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
C7	Capacitor 0.22uF ± 5% 100V	Siemens B32560-100	435/4/90317/017
C2	Capacitor 1uF ± 20% 35V	ITT Tag	402/4/57057/003
C6,14	Capacitor 10uF ± 20% 16V	ITT Tag	402/4/57057/008
C9	Capacitor 22uF ± 20% 6.3V	ITT Tag	402/4/57057/012
FL1	Ceramic Filter	Vemitron TL 40 x 64-571-1	422/9/07783
L3	Inductor 4.7uH ± 10%	Sigma SC10	406/4/31749/001
L1,2	Inductor 2.7uH ± 10%	Cambion 553-3635-42	406/4/31748/042
IC1,5	Integrated Circuit	Motorola MC14013CP	445/4/02383/013
IC2	Integrated Circuit	Motorola MC14066CP	445/4/02383/066
IC4	Integrated Circuit	Plessey SP8311M	445/4/03085
IC3	Integrated Circuit	Plessey SP8323M	445/4/0388
R7,17,20	Resistor 47R ± 2% 0.25W	Electrosil TR4	403/4/05521/470
R16,21,22	Resistor 470R ± 2% 0.25W	Electrosil TR4	403/4/05522/470
R1,14	Resistor 560R ± 2% 0.25W	Electrosil TR4	403/4/05522/560
R4	Resistor 1.5k ± 2% 0.25W	Electrosil TR4	403/4/05523/150
R5	Resistor 2.2k ± 2% 0.25W	Electrosil TR4	403/4/05523/220
R3,19	Resistor 3.3k ± 2% 0.25W	Electrosil TR4	403/4/05523/330
R18	Resistor 6.8k ± 2% 0.25W	Electrosil TR4	403/4/05523/680
R6	Resistor 8.2k ± 2% 0.25W	Electrosil TR4	403/4/05523/820
R15	Resistor 10k ± 2% 0.25W	Electrosil TR4	403/4/05524/100
R8-13	Resistor 47k ± 2% 0.25W	Electrosil TR4	403/4/05524/470
R2	Resistor 180k ± 2% 0.25W	Electrosil TR4	403/4/05525/180
T1	Transformer	Plessey	406/9/29657/012
TR2	Transistor	Ferranti ZTX302L	417/4/01875
TR1,4,5	Transistor	Ferranti ZTX314L	417/4/01873
TR6	Transistor	Ferranti ZTX320L	417/4/01874
TR3	Transistor	Ferranti ZTX502L	417/4/01876
SK2,3	Socket PV Card	Berg 3-way D/Row 65000-203	508/9/22101/001
SK1	Socket PV Card	Berg 15-way D/Row 65000-215	508/9/22101/002

Panel Printed Circuit H (419/1/18035)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Panel Printed Circuit	Plessey	419/2/18036
-	Socket Semi-Conductor	Texas 14L DIL C931402	508/4/22096/002
-	Socket Semi-Conductor	Texas 16L DIL C931602	508/4/22096/003
C1,4-6,9, 13,16	Capacitor 4.7nF ± 10% 100V	Erie 8111M-X7R	400/4/21280/001
C2,7,12, 14,16,17	Capacitor 10nF ± 10% 100V	Erie 8121M-X7R	400/4/20673/002
C8	Capacitor 0.1uF ± 5% 100V	Siemens B32560	435/4/90317/014
C18	Capacitor 1uF ± 20% 35V	ITT Tag	402/4/57057/003
C3,10	Capacitor 10uF ± 20% 16V	ITT Tag	402/4/57057/008
C11,15	Capacitor 22uF ± 20% 16V	ITT Tag	402/4/57057/009
FL1	Ceramic Filter	Vermitron TL 40 x 64-5711-2	422/9/07783
L1,4	Inductor 4.7uH ± 10%	Sigma SC10	406/4/31749/001

Panel Printed Circuit H (Cont'd)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
L2	Inductor 10uH ± 10%	Sigma SC30	406/4/31753/024
L3,	Inductor 100uH ± 10%	Sigma SC30	406/4/31753/036
IC7	Integrated Circuit	Motorola MC14001CP	445/4/02383/001
IC4	Integrated Circuit	Motorola MC14008CP	445/4/02383/008
IC2	Integrated Circuit	Motorols MC14017CP	445/4/01283/017
IC8	Integrated Circuit	Motorola MC14023CP	445/4/02383/023
IC9	Integrated Circuit	Motorola MC14507CP	445/4/02383/507
IC1	Integrated Circuit	Motorola MC10102P	445/4/03041/003
IC3	Integrated Circuit	Motorola MC10138P	445/4/03041/039
IC5	Integrated Circuit	Plessey SP8311M	445/4/03085
IC6	Integrated Circuit	Plessey SP8323M	445/4/03088
R5	Resistor 47R ± 2% 0.25W	Electrosil TR4	403/4/05521/470
R20,30	Resistor 100R ± 2% 0.25W	Electrosil TR4	403/4/05522/100
R11	Resistor 180R ± 2% 0.25W	Electrosil TR4	403/4/05522/180
R1,8	Resistor 220R ± 2% 0.25W	Electrosil TR4	403/4/05522/220
R12,15-19,22	Resistor 560R ± 2% 0.25W	Electrosil TR4	403/4/05522/560
R10	Resistor 820R ± 2% 0.25W	Electrosil TR4	403/4/05522/820
R37-42	Resistor 1k ± 2% 0.25W	Electrosil TR4	403/4/05523/100
R4	Resistor 1.2k ± 2% 0.25W	Electrosil TR4	403/4/05523/120
R9	Resistor 1.8k ± 2% 0.25W	Electrosil TR4	403/4/05523/180
R3,14	Resistor 2.2k ± 2% 0.25W	Electrosil TR4	403/4/05523/220
R2	Resistor 3.3k ± 2% 0.25W	Electrosil TR4	403/4/05523/330
R29	Resistor 4.7k ± 2% 0.25W	Electrosil TR4	403/4/05523/470
R7,21	Resistor 10k ± 2% 0.25W	Electrosil TR4	403/4/05524/100
R6	Resistor 33k ± 2% 0.25W	Electrosil TR4	403/4/05524/330
R23-28	Resistor 47k ± 2% 0.25W	Electrosil TR4	403/4/05524/470
R13	Resistor 180k ± 2% 0.25W	Electrosil TR4	403/4/05525/180
R31-36,43	Resistor 1M ± 5%	Allen Bradley Type C8	403/4/04361/003
D2	Diode	Texas iN4001	415/9/98466/001
D1	Diode	Texas 1N4148	415/4/05720
TR2	Transistor	Ferranti ZTX108L	417/4/02039/012
TR4,5	Transistor	Ferranti ZTX314L	417/4/01873
TR1	Transistor	Ferranti ZTX320L	417/4/01874
TR3	Transistor	Ferranti ZTX510L	417/4/98309/007
SK2,3	Socket PV Card	Berg 3-way D/Row 65000-203	508/9/22101/001
SK1	Socket PV Card	Berg 15-way D/Row 65000-215	508/9/22101/002

Panel Electronic Circuit J (419/1/18047)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Panel Printed Circuit	Plessey	419/2/18048
-	Screen	Plessey	
-	Screen Box	Plessey	630/2/33037/001
-	Screen Box	Plessey	630/2/33037/002
-	Socket Semi-Conductor	Texas 14L DIL C931402	508/4/22096/002
C11,13	Capacitor 180pF ± 2.5% 30V	Suflex HSC 30V	437/4/30011/015
C15	Capacitor 2,7000pF ± 2.5% 30V	Suflex HSC 30V	437/4/30011/104

Panel Electronic Circuit J (Cont'd)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
C6	Capacitor 15pF ± 5% 100V	Erie 8121M-100-COG	400/4/20672/001
C7,21	Capacitor 100pF ± 5% 100V	Erie 8121M-100-COG	400/4/20672/002
C3,4	Capacitor 220pF ± 5% 100V	Erie 8121M-100-COG	400/4/20672/003
C18	Capacitor 1,000pF ± 10% 100V	Erie 8121M-100-X7R	400/4/20673/001
C20,22-27, 29-33,35,36	Capacitor 4,700pF ± 10% 100V	Erie 8111M-X7R	400/4/21280/001
C14	Capacitor 0.001uF ± 5% 400V	Siemens B32560	435/4/90317/023
C10,12	Capacitor 0.0022uF ± 5% 400V	Siemens B32560	435/4/90317/025
C8,17	Capacitor 0.01uF ± 5% 400V	Siemens B32560	435/4/90317/029
C1	Capacitor 100nF ± 5% 100V	Siemens B32560	435/4/90317/014
C16,39	Capacitor 0.22uF ± 5% 100V	Siemens B32560	435/4/90317/017
C37	Capacitor 0.1uF ± 20% 35V	ITT Tag	403/4/57057/001
C2	Capacitor 2.2uF ± 20% 16V	ITT Tag	402/4/57057/007
C5,34,38	Capacitor 10uF ± 20% 16V	ITT Tag	402/4/57057/008
C28	Capacitor 10uF ± 20% 35V	ITT Tag	402/4/57057/006
C9	Capacitor 10uF +50% -10% 63V	ITT EN12.35	402/9/55702/022
L4	Inductor 0.64uH	Plessey	406/9/29665/001
L3	Inductor 6.8uH ± 10%	Sigma SC30	406/4/31753/022
L6	Inductor 10uH ± 10%	Sigma SC30	406/4/31753/024
L5,7	Inductor 100uH ± 10%	Sigma SC30	406/4/31753/036
L1	Inductor 9.03mH	Plessey	406/9/29666/003
L2	Inductor 9.85mH	Plessey	406/9/29666/004
IC3	Integrated Circuit	Motorola MC14011CP	445/4/02383/011
IC1,2	Integrated Circuit	Motorola MC14013CP	445/4/02383/013
R29	Resistor 10R ± 2% 0.25W	Electrosil TR4	403/4/05521/100
R17	Resistor 39R ± 2% 0.25W	Electrosil TR4	403/4/05521/390
R5,50	Resistor 47R ± 2% 0.25W	Electrosil TR4	403/4/05521/470
R44,45,47,48	Resistor 68R ± 2% 0.25W	Electrosil TR4	403/4/05521/680
R18,30	Resistor 82R ± 2% 0.25W	Electrosil TR4	403/4/05521/820
R10	Resistor 100R ± 2% 0.25W	Electrosil TR4	403/4/05522/100
R35,39	Resistor 150R ± 2% 0.25W	Electrosil TR4	403/4/05522/160
R38,43,46	Resistor 220R ± 2% 0.25W	Electrosil TR4	403/4/05522/220
R37,42,49	Resistor 680R ± 2% 0.25W	Electrosil TR4	403/4/05522/680
R3,8,54,56	Resistor 1k ± 2% 0.25W	Electrosil TR4	403/4/05523/100
R36	Resistor 1.2k ± 2% 0.25W	Electrosil TR4	403/4/05523/120
R14	Resistor 1.5k ± 2% 0.25W	Electrosil TR4	403/4/05523/150
R28	Resistor 1.8k ± 2% 0.25W	Electrosil TR4	403/4/05523/180
R16	Resistor 2.2k ± 2% 0.25W	Electrosil TR4	403/4/05523/220
R53	Resistor 2.7k ± 2% 0.25W	Electrosil TR4	403/4/05523/270
R11,24	Resistor 3.3k ± 2% 0.25W	Electrosil TR4	403/4/05523/330
R52	Resistor 3.9k ± 2% 0.25W	Electrosil TR4	403/4/05523/390
R27,32	Resistor 5.6k ± 2% 0.25W	Electrosil TR4	403/4/05523/560
R33,40,57	Resistor 6.8k ± 2% 0.25W	Electrosil TR4	403/4/05523/680
R13,20,41	Resistor 8.2k ± 2% 0.25W	Electrosil TR4	403/4/05523/820
R21,22,31,55	Resistor 12k ± 2% 0.25W	Electrosil TR4	403/4/05524/120
R4	Resistor 18k ± 2% 0.25W	Electrosil TR4	403/4/05524/180
R25,26	Resistor 22k ± 2% 0.25W	Electrosil TR4	403/4/05524/220
R12,15,19	Resistor 33k ± 2% 0.25W	Electrosil TR4	403/4/05524/330
R51	Resistor 47k ± 2% 0.25W	Electrosil TR4	403/4/05524/470
R23	Resistor 68k ± 2% 0.25W	Electrosil TR4	403/4/05524/680

Panel Electronic Circuit J (Cont'd)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
R7,34,36	Resistor 100k ± 2% 0.25W	Electrosil TR4	403/4/05525/100
R9	Resistor 220k ± 2% 0.25W	Electrosil TR4	403/4/05525/220
R6	Resistor 300k ± 2% 0.25W	Electrosil TR4	403/4/05525/300
R1,2	Resistor 1M ± 5%	Allen Bradley Type CB	403/4/04361/003
R58	Resistor Variable 2.2k	Allen Bradley Type 90H	403/4/05047/011
D1	Diode	Texas 1N4148	415/4/05720
D2,3	Diode	Texas 1N5148	415/4/05737
D4,5	Diode	Hewlett Packard HPA5082-2800	415/9/98532
D6	Diode	Mullard BZY88C5V6	415/4/05738/010
T1,2	Transformer	Plessey	406/9/29657/011
TR2	Transistor	Ferranti ZTX108L	417/4/02039/012
TR1	Transistor	Ferranti ZTX109L	417/4/02039/011
TR3,6,14, 15	Transistor	Ferranti ZTX304L	417/4/98308/010
TR13	Transistor	Ferranti ZTX510L	417/4/98308/007
TR7,9,10	Transistor	Texas BF576 or SGS BFR99	417/4/01883
TR8	Transistor	Sil Conix J310	417/4/01888/003
TR11,12	Transistor	Texas 2N5109	417/4/01784
TR5	Transistor	Motorola MPS-A43	417/4/01878
TR4,16	Transistor	Motorola MPS-A93	417/4/01885
SK2	Socket PV Card	Berg 3-way D/Row 65000-203	508/9/22101/001
SK1	Socket PV Card	Berg 15-way D/Row 65000-215	508/9/22101/002

Panel Electronic Circuit K (419/1/18049)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Panel Printed Circuit	Plessey	419/2/18050
-	Socket Semi-Conductor	Texas 14L DIL C931402	408/4/22096/002
-	Socket Semi-Conductor	Texas 16L DIL C931602	508/4/22096/003
C1,2,4-6, 8,9	Capacitor 4.7nF ± 10% 100V	Erie 8111M-X7R	400/4/21280/001
C10,12,14	Capacitor 10nF ± 10% 100V	Erie 8121M-X7R	400/4/20673/002
C3,11,13	Capacitor 10uF ± 20% 16V	ITT Tag	402/4/57057/008
C7	Capacitor 22uF ± 20% 6.3V	ITT Tag	402/4/57057/012
L2	Inductor 4.7uH ± 10%	Sigma SC10	406/4/31749/001
L1	Inductor 10uH ± 10%	Sigma SC30	406/4/31753/024
IC7	Integrated Circuit	Motorola MC14011CP	445/4/02383/011
IC4,6,9	Integrated Circuit	Motorola MC14013CP	445/4/02383/013
IC5	Integrated Circuit	Motorola MC14017CP	445/4/02383/017
IC3	Integrated Circuit	Mullard HEF4027P	445/4/03056
IC1	Integrated Circuit	Motorola MC10102P	445/4/03041/003
IC2	Integrated Circuit	Motorola MC10178P	445/4/03041/079
IC8	Integrated Circuit	Motorola MC14526CP	445/4/03041/526
R4,18	Resistor 47R ± 2% 0.25W	Electrosil TR4	403/4/05521/470
R11,14	Resistor 100R ± 2% 0.25W	Electrosil TR4	403/4/05522/100

Panel Electronic Circuit K (Cont'd)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
R1,5	Resistor 220R ± 2%, 0.25W	Electrosil TR4	403/4/05522/220
R6,10,15	Resistor 560R ± 2% 0.25W	Electrosil TR4	403/4/05522/560
R3,13,17	Resistor 2.2k ± 2% 0.25W	Electrosil TR4	403/4/05523/220
R2	Resistor 3.3k ± 2% 0.25W	Electrosil TR4	403/4/05523/330
R19	Resistor 18k ± 2% 0.25W	Electrosil TR4	403/4/05524/180
R12,16	Resistor 180k ± 2% 0.25W	Electrosil TR4	403/4/05525/180
D1	Diode	Texas 1N4001	415/9/98466/001
D2	Diode	Texas 1N4148	415/4/05720
TR2,3,4	Transistor	Ferranti ZTX314L	417/4/01873
TR1	Transistor	Ferranti ZTX302L	417/4/01874
SK2	Socket PV Card	Berg 3-way D/Row 65000-203	508/9/22101/001
SK1	Socket PV Card	Berg 15-way D/Row 65000-215	508/9/22101/002

Panel Electronic Circuit L (419/1/18059)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Panel Printed Circuit	Plessey	419/2/18060
-	Screen	Plessey	
-	Screen Box	Plessey	630/2/33037/001
-	Screen Box	Plessey	630/2/33037/002
-	Socket Semi-Conductor	Texas 14L DIL C931402	508/4/22096/002
C11,13	Capacitor 3,300pF ± 2.5% 30V	Suflex HSC30	437/9/30043/004
C6	Capacitor 15pF ± 5% 100V	Erie 8121M-100-C0G	400/4/20672/001
C19	Capacitor 27pF ± 5% 100V	Erie 8121M-100-C0G	400/4/20672/007
C7,21	Capacitor 100pF ± 5% 100V	Erie 8121M-100-C0G	400/4/20672/002
C3,4,18	Capacitor 1000pF ± 10% 100V	Erie 8121M-100-X7R	400/4/20673/001
C20,22-27, 29-33,35, 36	Capacitor 4700pF ± 10% 100V	Erie 8111M-X7R	400/4/21280/001
C8,17	Capacitor 0.01uF ± 5% 400V	Siemens B32560	435/4/90317/007
C10,12,14	Capacitor 0.068uF ± 5% 100V	Siemens B32560	435/4/90317/012
C1	Capacitor 0.1uF ± 5% 100V	Siemens B32560	435/4/90317/014
C16,39	Capacitor 0.22uF ± 5% 100V	Siemens B32560	435/4/90317/017
C37	Capacitor 0.1uF ± 20% 35V	ITT Tag	402/4/57057/001
C2	Capacitor 2.2uF ± 20% 16V	ITT Tag	402/4/57057/007
C5,34,38	Capacitor 10uF ± 20% 16V	ITT Tag	402/4/57057/008
C28	Capacitor 10uF ± 20% 35V	ITT Tag	402/4/57057/006
C9	Capacitor 10uF +50% -10% 63V	ITT EN12-35	402/9/55702/022
L4	Inductor 0.75uH	Plessey	406/9/29665/001
L3	Inductor 6.8uH ± 10%	Sigma SC30	406/4/31753/022
L6	Inductor 10uH ± 10%	Sigma SC30	406/4/31753/024
L5,7	Inductor 100uH ± 10%	Sigma SC30	406/4/31753/036
L1,2	Inductor 12.28mH	Plessey	406/9/29666/005
IC3	Integrated Circuit	Motorola MC14011CP	445/4/02383/011

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
IC1,2	Integrated Circuit	Motorola MC14013CP	445/4/02383/013
R29	Resistor 10R ± 2% 0.25W	Electrosil TR4	403/4/05521/100
R5,50	Resistor 47R ± 2% 0.25W	Electrosil TR4	403/4/05521/470
R44,45,47,48	Resistor 68R ± 2% 0.25W	Electrosil TR4	403/4/05521/680
R3	Resistor 82R ± 2% 0.25W	Electrosil TR4	403/4/05521/820
R10	Resistor 100R ± 2% 0.25W	Electrosil TR4	403/4/05522/100
R35,39	Resistor 150R ± 2% 0.25W	Electrosil TR4	403/4/05522/150
R17	Resistor 180R ± 2% 0.25W	Electrosil TR4	403/4/05522/180
R38,43,46	Resistor 220R ± 2% 0.25W	Electrosil TR4	403/4/05522/220
R18	Resistor 470R ± 2% 0.25W	Electrosil TR4	403/4/05522/470
R24,37,42,49	Resistor 680R ± 2% 0.25W	Electrosil TR4	403/4/05522/680
R3,8,54,59	Resistor 1k ± 2% 0.25W	Electrosil TR4	403/4/05523/100
R36	Resistor 1.2k ± 2% 0.25W	Electrosil TR4	403/4/05523/120
R28	Resistor 1.8k ± 2% 0.25W	Electrosil TR4	403/4/05523/180
R14,23,53	Resistor 2.7k ± 2% 0.25W	Electrosil TR4	403/4/05523/270
R52	Resistor 3.3k ± 2% 0.25W	Electrosil TR4	403/4/05523/330
R21,22	Resistor 3.9k ± 2% 0.25W	Electrosil TR4	403/4/05523/390
R16	Resistor 4.7k ± 2% 0.25W	Electrosil TR4	403/4/05523/470
R32	Resistor 5.6k ± 2% 0.25W	Electrosil TR4	403/4/05523/560
R11,33,40,57	Resistor 6.8k ± 2% 0.25W	Electrosil TR4	403/4/05523/680
R13,20,41	Resistor 8.2k ± 2% 0.25W	Electrosil TR4	403/4/05523/820
R51	Resistor 10k ± 2% 0.25W	Electrosil TR4	403/4/05524/100
R31,55	Resistor 12k ± 2% 0.25W	Electrosil TR4	403/4/05524/120
R56	Resistor 15k ± 2% 0.25W	Electrosil TR4	403/4/05524/150
R4,15	Resistor 18k ± 2% 0.25W	Electrosil TR4	403/4/05524/180
R24	Resistor 22k ± 2% 0.25W	Electrosil TR4	403/4/05524/220
R12,19	Resistor 33k ± 2% 0.25W	Electrosil TR4	403/4/05524/330
R7,34	Resistor 100k ± 2% 0.25W	Electrosil TR4	403/4/05525/100
R9	Resistor 200k ± 2% 0.25W	Electrosil TR4	403/4/05525/200
R6	Resistor 300k ± 2% 0.25W	Electrosil TR4	403/4/05525/300
R1,2	Resistor 1M ± 5%	Allen Bradley Type CB	403/4/04361/003
R26	Resistor 47k ± 2% 0.25W	Electrosil TR4	403/4/05524/470
R58	Resistor Variable 2.2k ± 20%	Allen Bradley 90H	404/9/05047/011
D1	Diode	Texas 1N4148	415/4/05720
D4,5	Diode	Hewlett Packard HPA 5082-2800	415/9/98532
D3	Diode	Motorola MV2114	415/9/98905/013
D6	Diode	Mullard BZY88C5V6	415/9/98905/013
T1,2	Transformer	Plessey special	406/9/29657/011
TR2,3,14, 15	Transistor	Ferranti ZTX108L	417/4/02039/012
TR1,6	Transistor	Ferranti ZTX109L	417/4/02039/011
TR5	Transistor	Ferranti ZTX302L	417/4/01875
TR4,16	Transistor	Ferranti ZTX502L	417/4/01876
TR13	Transistor	Ferranti ZTX510L	417/4/98309/007
TR7,9,10	Transistor	Texas BF576 or SGS BFR99	417/4/01883
TR8	Transistor	Siliconix J310	417/4/01888/003
TR11,12	Transistor	Texas 2N5109	417/4/01784
SK2	Socket PV Card	Berg 3-way D/Row 65000-203	508/9/22101/001
SK1	Socket PV Card	Berg 15-way D/Row 65000-215	508/9/22101/002

Regulator P.E.C. (419/1/18033)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Panel Printed Circuit	Plessey	419/2+18034
C1,2,3	Capacitor 1uF ± 20% 35V	ITT Tag	402/4/57057/003
C4	Capacitor 10uF ± 20% 16V	ITT Tag	402/4/57057/008
C5	Capacitor 22uF ± 20% 16V	ITT Tag	402/4/57057/009
R1	Resistor 100R ± 2% 0.25W	Electrosil TR4	403/4/05522/001
R2	Resistor Variable 220R ± 20%	Allen Bradley 90H	403/9/05047/013
D1-5	Diode LED	Texas TIL 209	520/9/97665
D6	Diode	Texas 1N4148	415/4/05720
IC1	Integrated Circuit	Motorola MC7712C	445/4/03074/007
IC2	Integrated Circuit	Motorola MC7720C	445/4/03074/004
IC3	Integrated Circuit	Motorola MC7806C	445/9/03051/002
IC4	Integrated Circuit	National LM 317T	445/4/03073

Connector Assembly (702/1/20093/005)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
SKF	Socket Electrical R.F. (Fixed)	Belling Lee L1465 'K' BS	508/4/22059
-	Cable R.F.	Suhner R.G. 316/U	998/4/82832/000

Connector Assembly (702/1/20093/012)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
SKE	Socket Electrical R.F. (Fixed)	Belling Lee L1465 'K' BS	508/4/22059
-	Cable R.F.	Suhner R.F. 316/U	998/4/82832/000

Connector Assembly (702/1/33370/001)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
SKE & D	Socket Electrical R.F. (Fixed)	Belling Lee L1465 'K' BS	508/4/22059
-	Cable R.F.	Suhner R.F. 316/U	998/4/82832/000

Connector Assembly (702/1/33370/002)

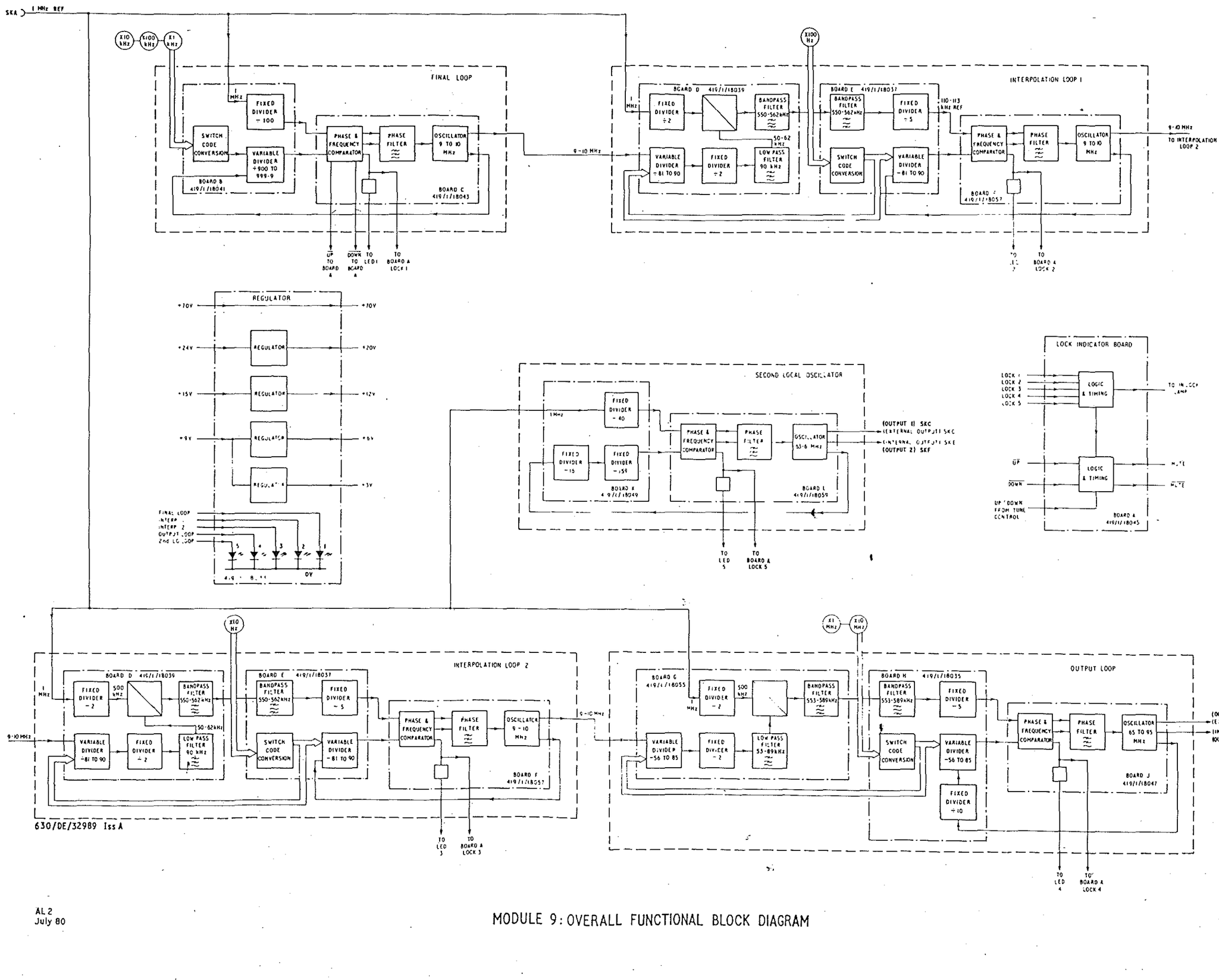
Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
SKB	Socket Electrical R.F. (Fixed)	Belling Lee L1465 'K' BS	508/4/22059
-	Cable R.F.	Suhner R.G. 316/U	998/4/82832/000

Connector Assembly (702/1/33370/003)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
SKA	Socket Electrical R.F. (Fixed)	Belling Lee L1465 'K' BS	508/4/22059
-	Cable R.F.	Suhner R.F. 316/U	998/4/82832/000

Cableform Assembly (702/1/33368)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Cable Tie	Insulock MS Series Type T18R	915/4/98775/000
-	Sleeve Ident Black 0	Hellerman	915/4/04042/060
-	Sleeve Ident Brown 1	Hellerman	915/4/04042/061
-	Sleeve Ident Red 2	Hellerman	915/4/04042/062
-	Sleeve Ident Orange 3	Hellerman	915/4/04042/063
-	Sleeve Ident Yellow 4	Hellerman	915/4/04042/064
-	Sleeve Ident Green 5	Hellerman	915/4/04042/065
-	Sleeve Ident Blue 6	Hellerman	915/4/04042/066
-	Sleeve Ident Violet 7	Hellerman	915/4/04042/067
-	Sleeve Ident Grey 8	Hellerman	915/4/04042/068
-	Sleeve Ident White 9	Hellerman	915/4/04042/069



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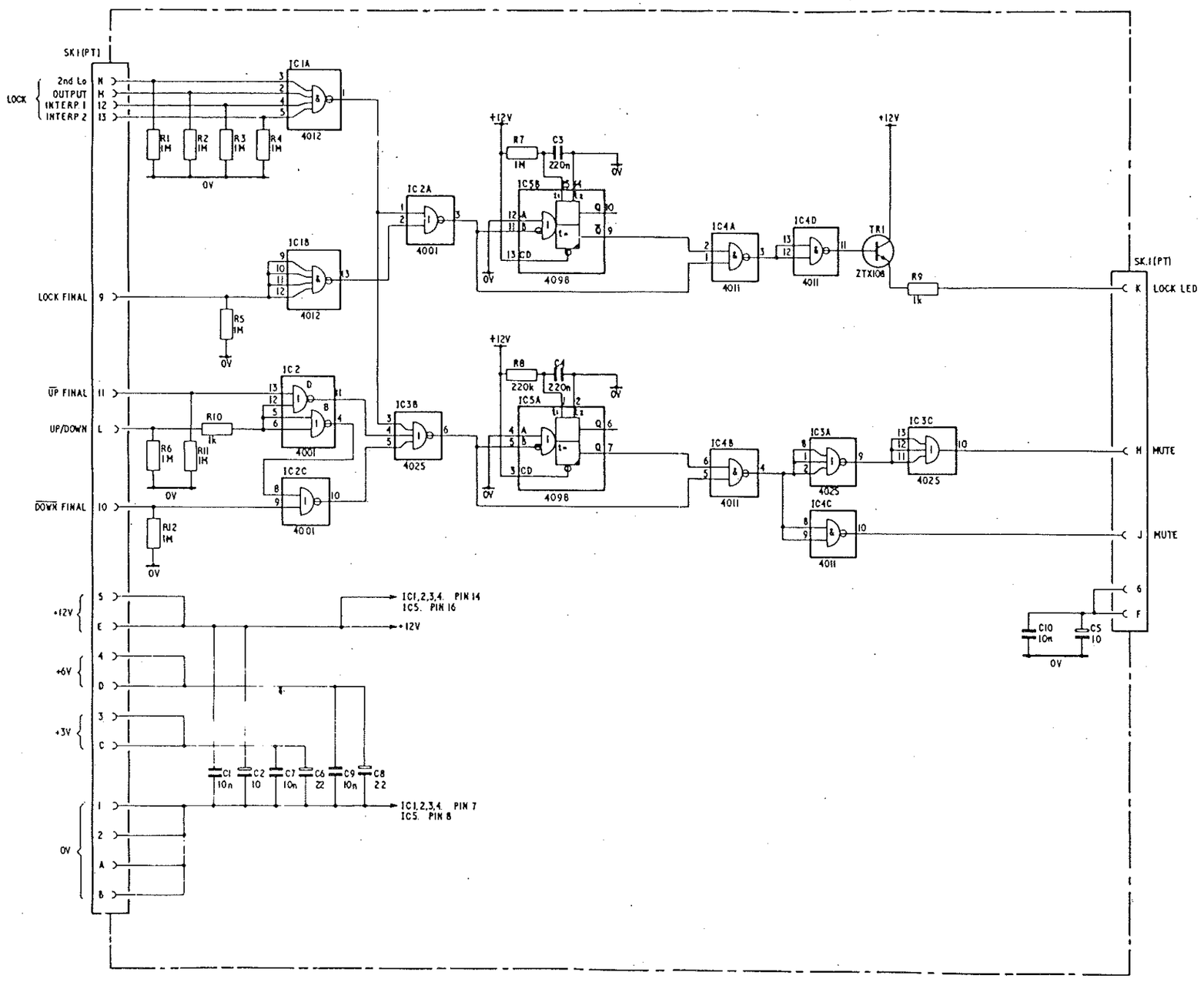
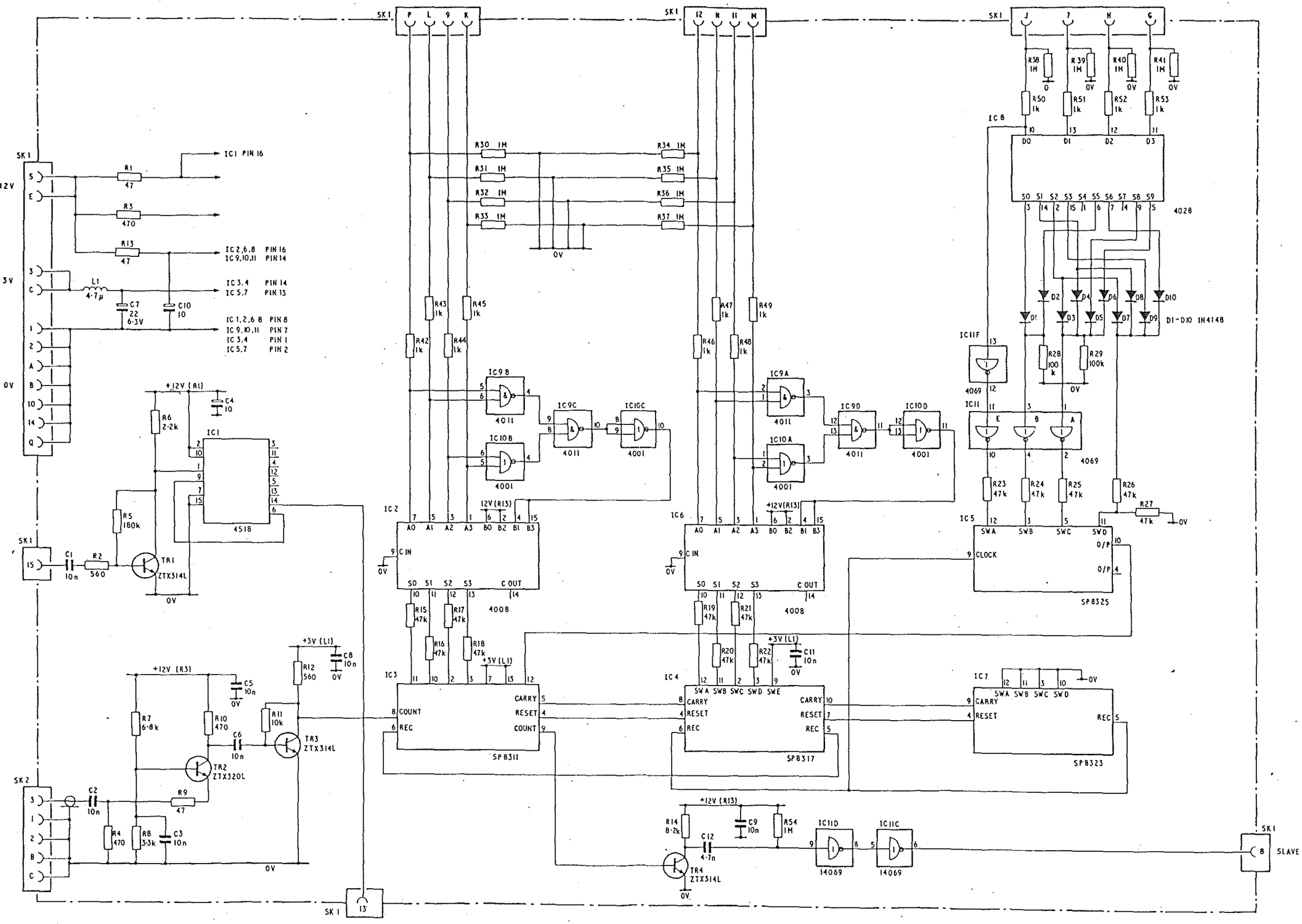
MODULE 9: OVERALL FUNCTIONAL BLOCK DIAGRAM

FIG 1



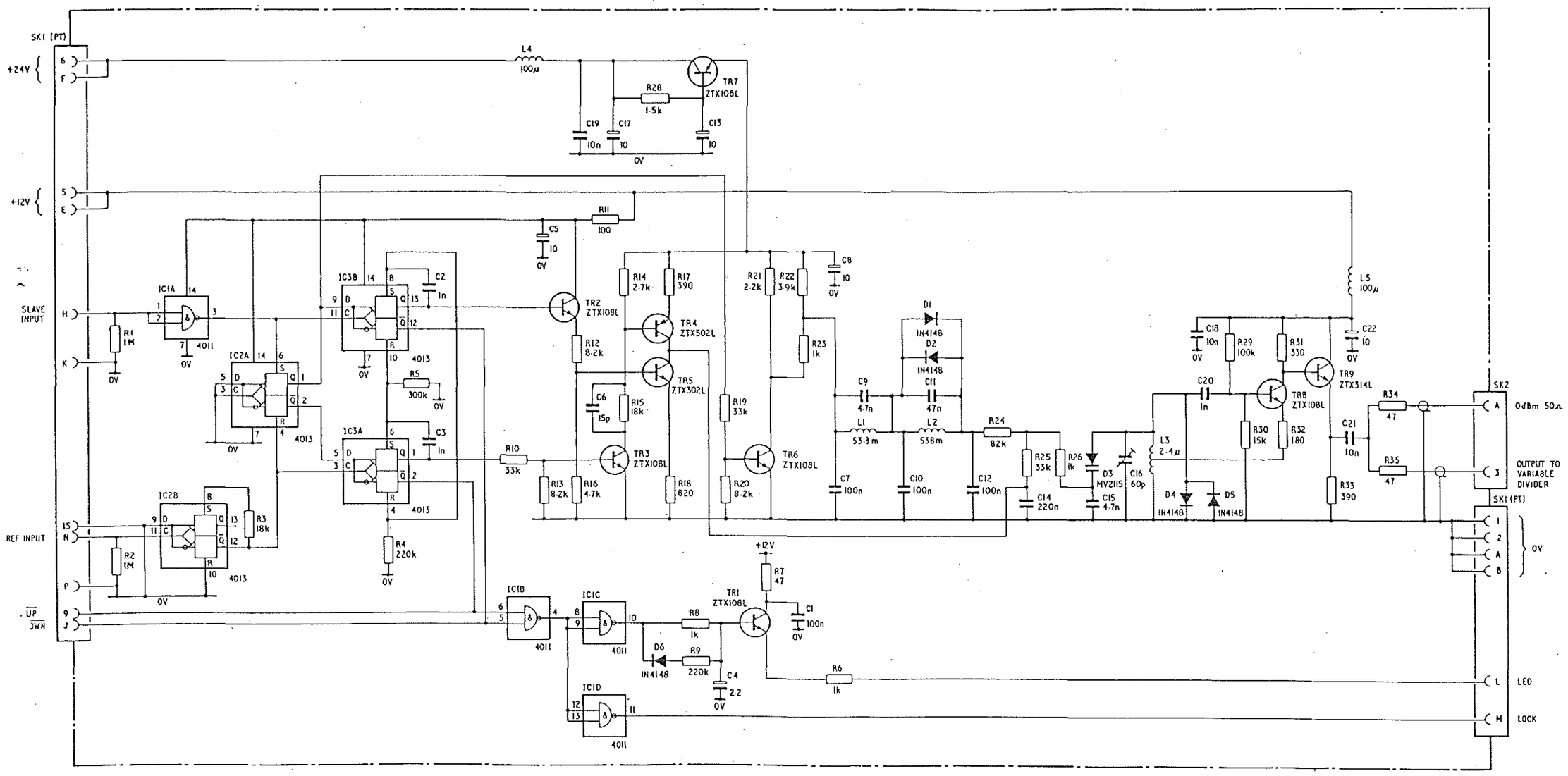
MODULE 9 : PANEL A, LOCK INDICATOR AND MUTING CIRCUIT DIAGRAM

FIG 2



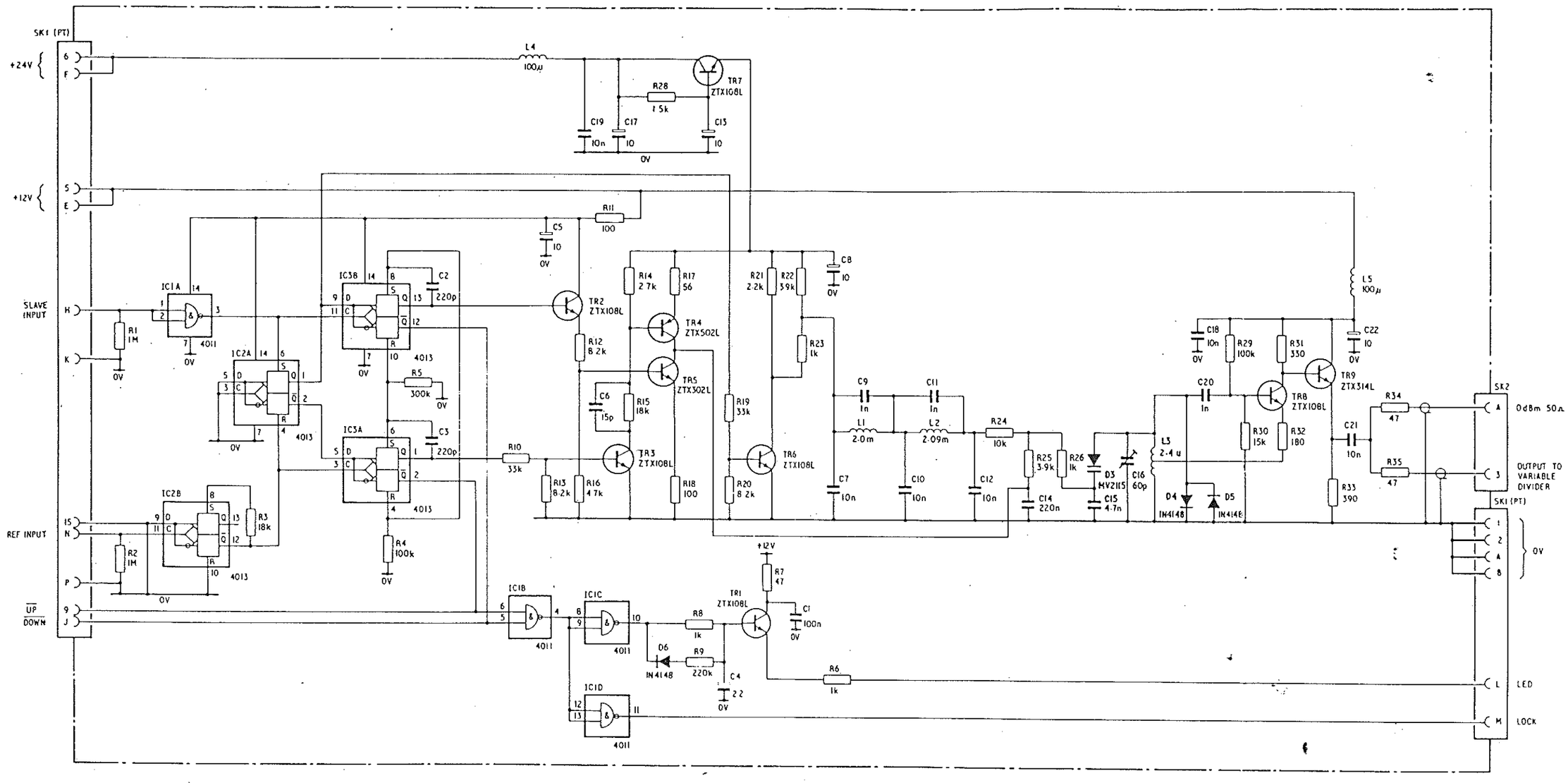
MODULE 9 : PANEL B, FINAL LOOP VARIABLE DIVIDER CIRCUIT DIAGRAM

FIG 3



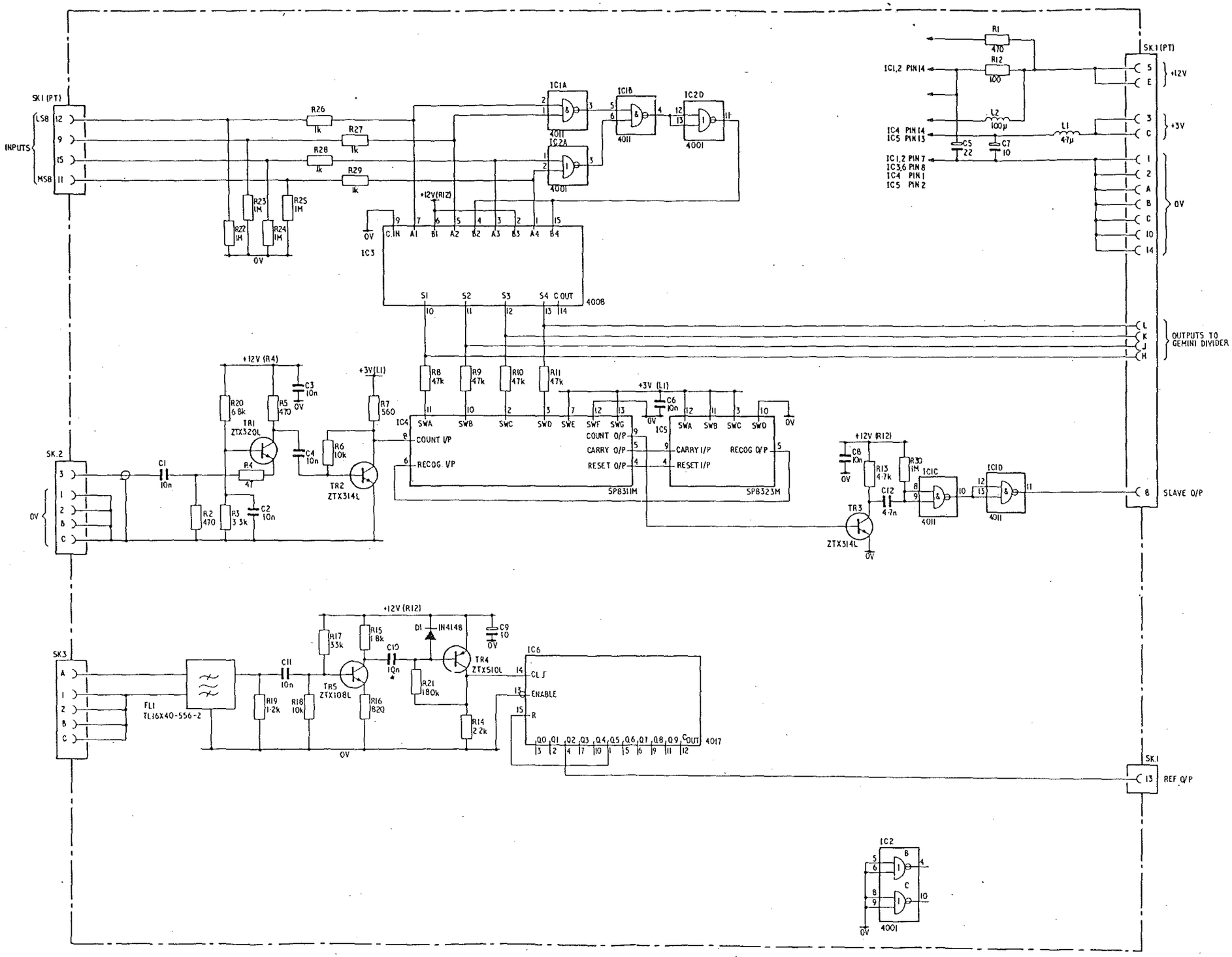
MODULE 9 : PANEL C, FINAL LOOP PHASE COMPARATOR AND OSCILLATOR CIRCUIT DIAGRAM

FIG 4



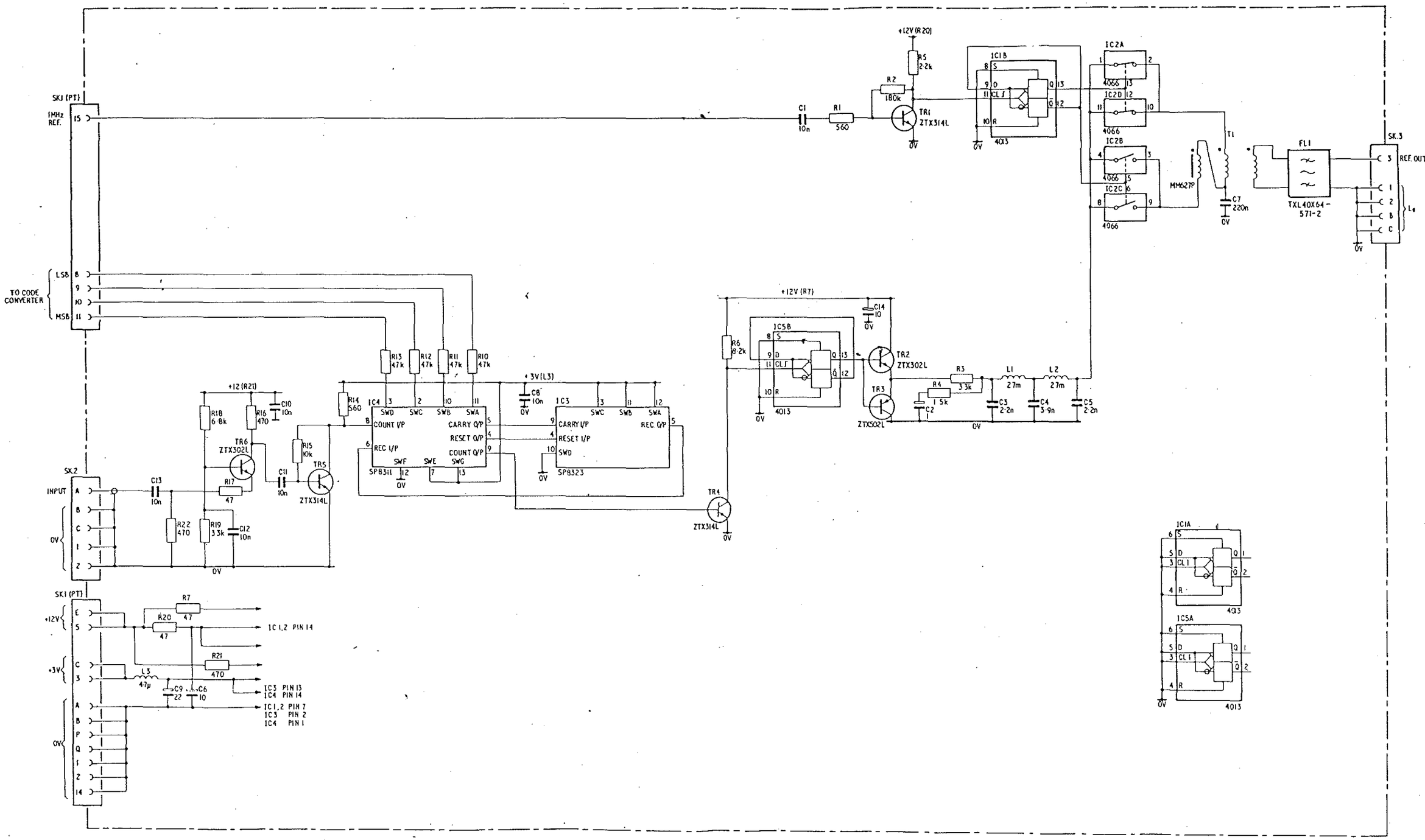
MODULE 9 : PANEL D, INTERPOLATION LOOPS 1 AND 2 DIVIDER AND MIXER CIRCUIT DIAGRAM

FIG 5



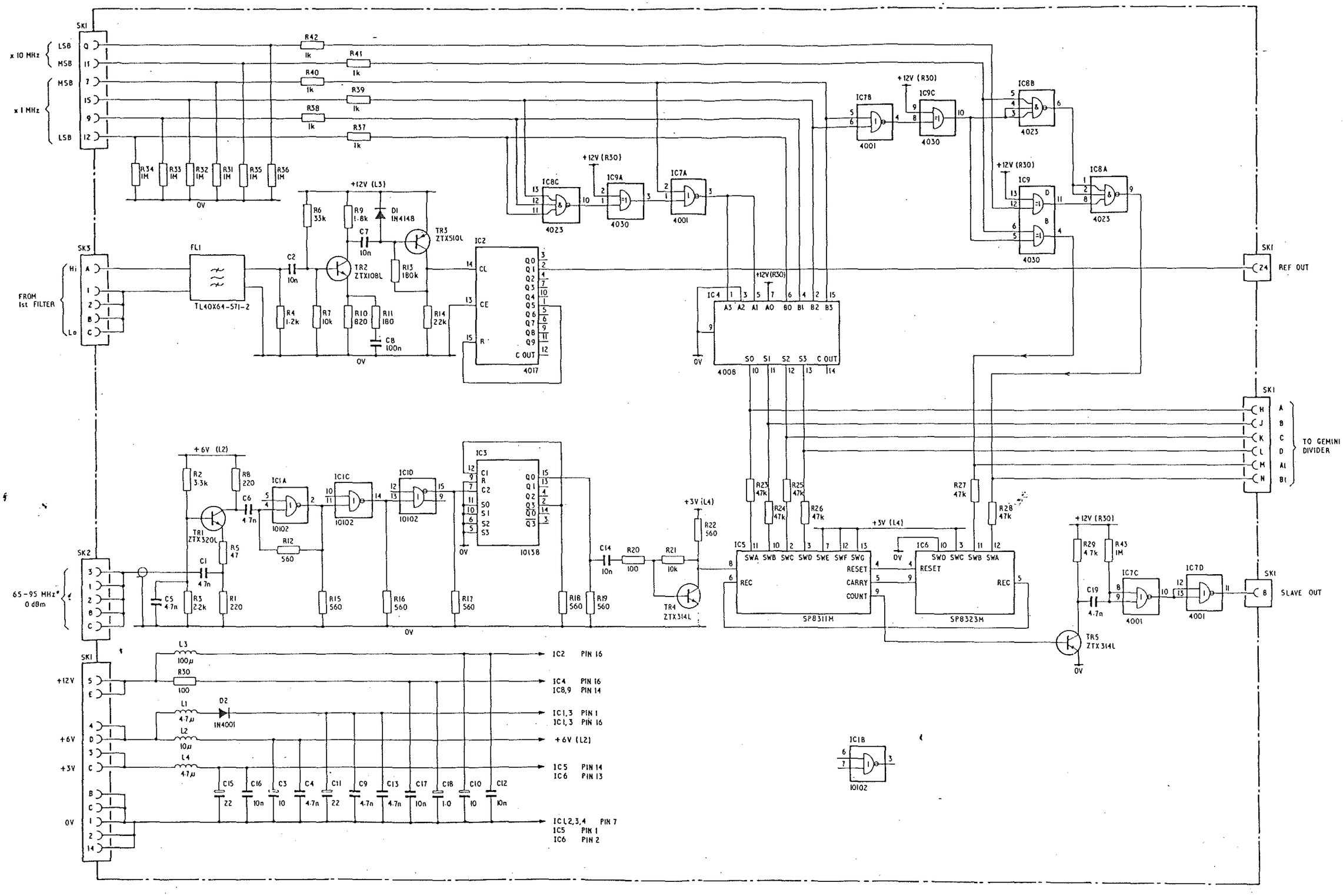
MODULE 9 : PANEL E, INTERPOLATION LOOPS 1 AND 2 VARIABLE DIVIDER CIRCUIT DIAGRAM

FIG 6



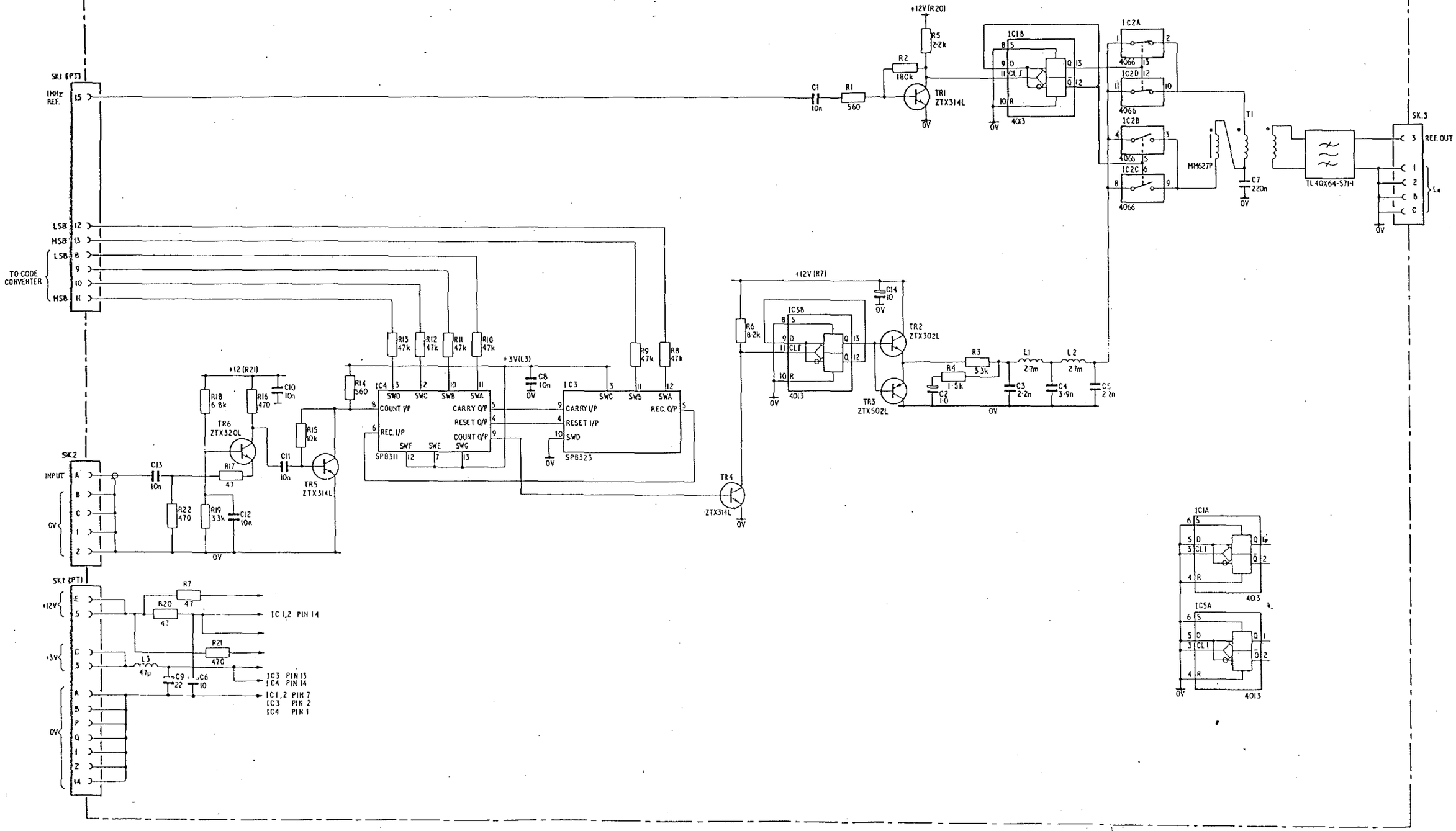
MODULE 9 : PANEL F, INTERPOLATION LOOPS 1 AND 2 PHASE COMPARATOR AND OSCILLATOR CIRCUIT DIAGRAM

FIG 7



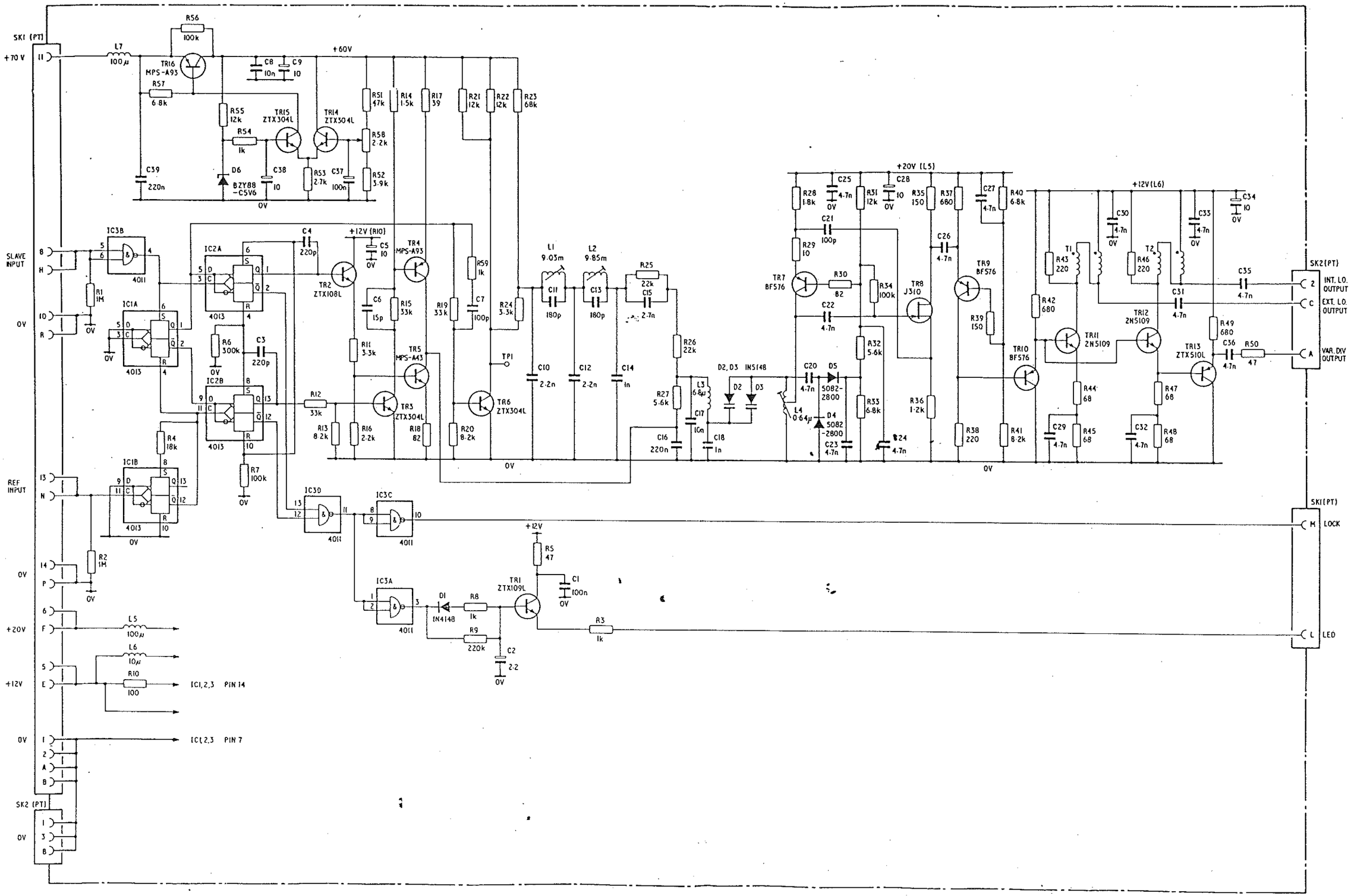
MODULE 9 : PANEL G, OUTPUT LOOP DIVIDER AND MIXER CIRCUIT DIAGRAM

FIG 8



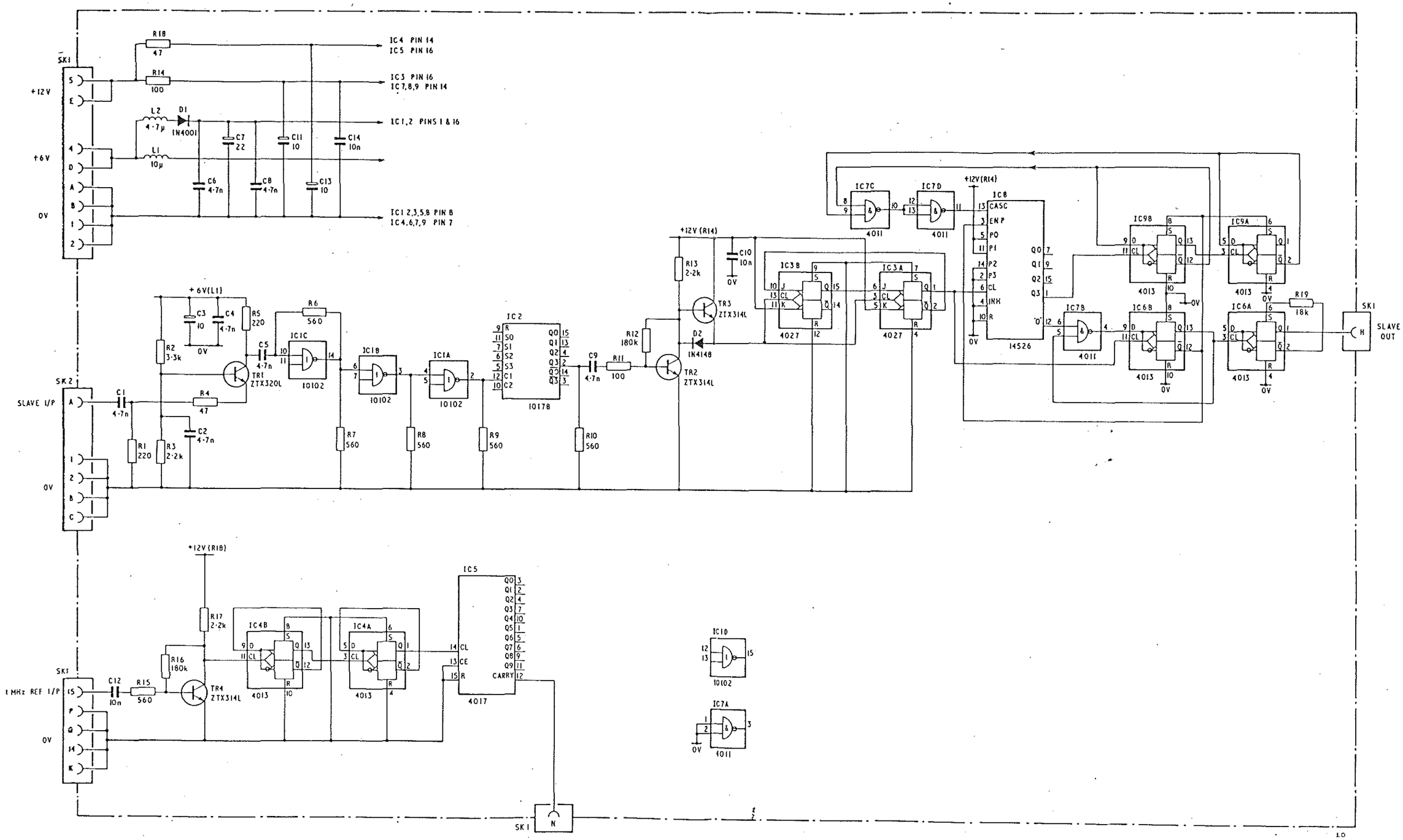
MODULE 9 : PANEL H, OUTPUT LOOP VARIABLE DIVIDER CIRCUIT DIAGRAM

FIG 9



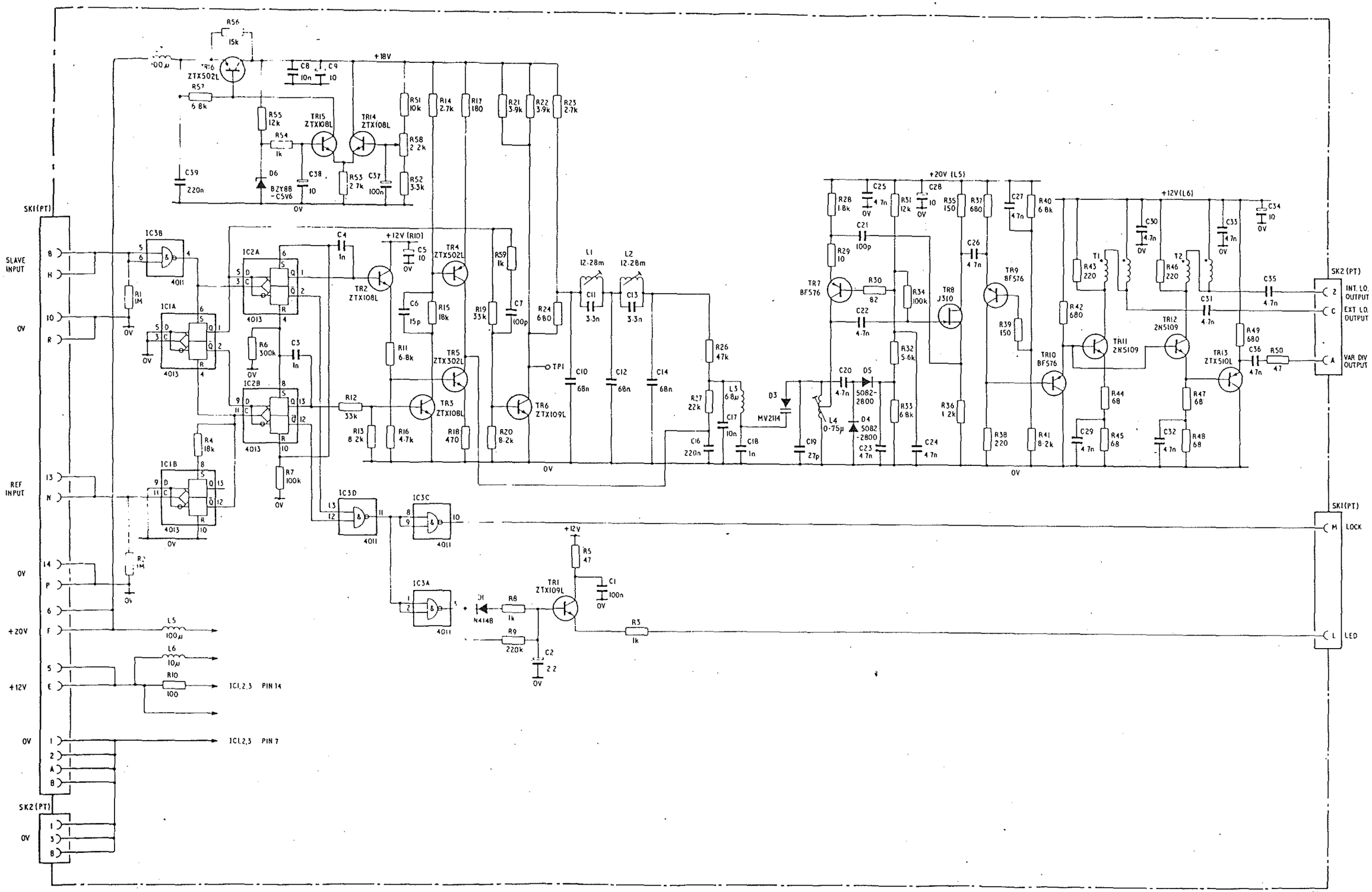
MODULE 9 : PANEL J, OUTPUT LOOP, PHASE COMPARATOR AND OSCILLATOR CIRCUIT DIAGRAM

FIG 10



MODULE 9 : PANEL K, 2ND LOCAL OSCILLATOR AND DIVIDER CIRCUIT DIAGRAM

FIG 11



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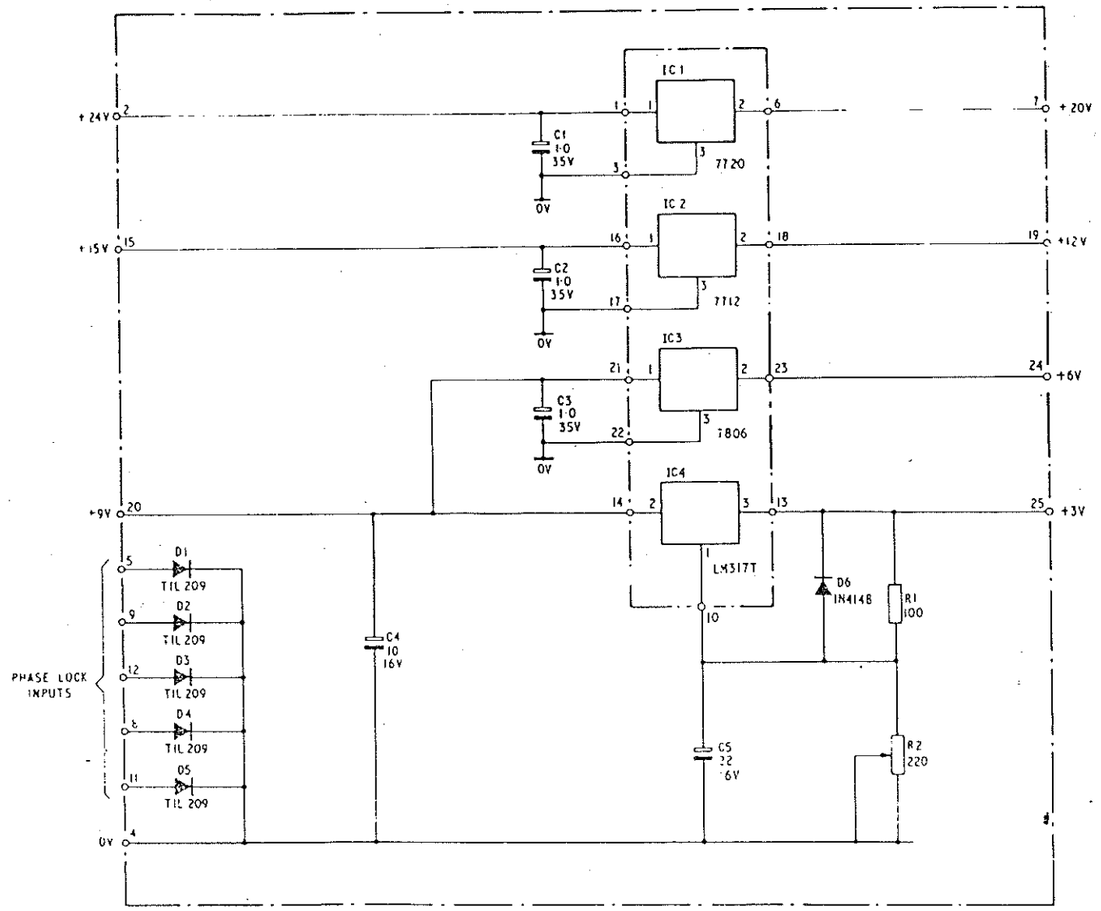
MODULE 9 : PANEL L, 2ND LOCAL OSCILLATOR AND PHASE COMPARATOR CIRCUIT DIAGRAM

FIG 12



MODULE 9 : POWER REGULATOR AND INDICATOR CIRCUIT DIAGRAM FIG 13

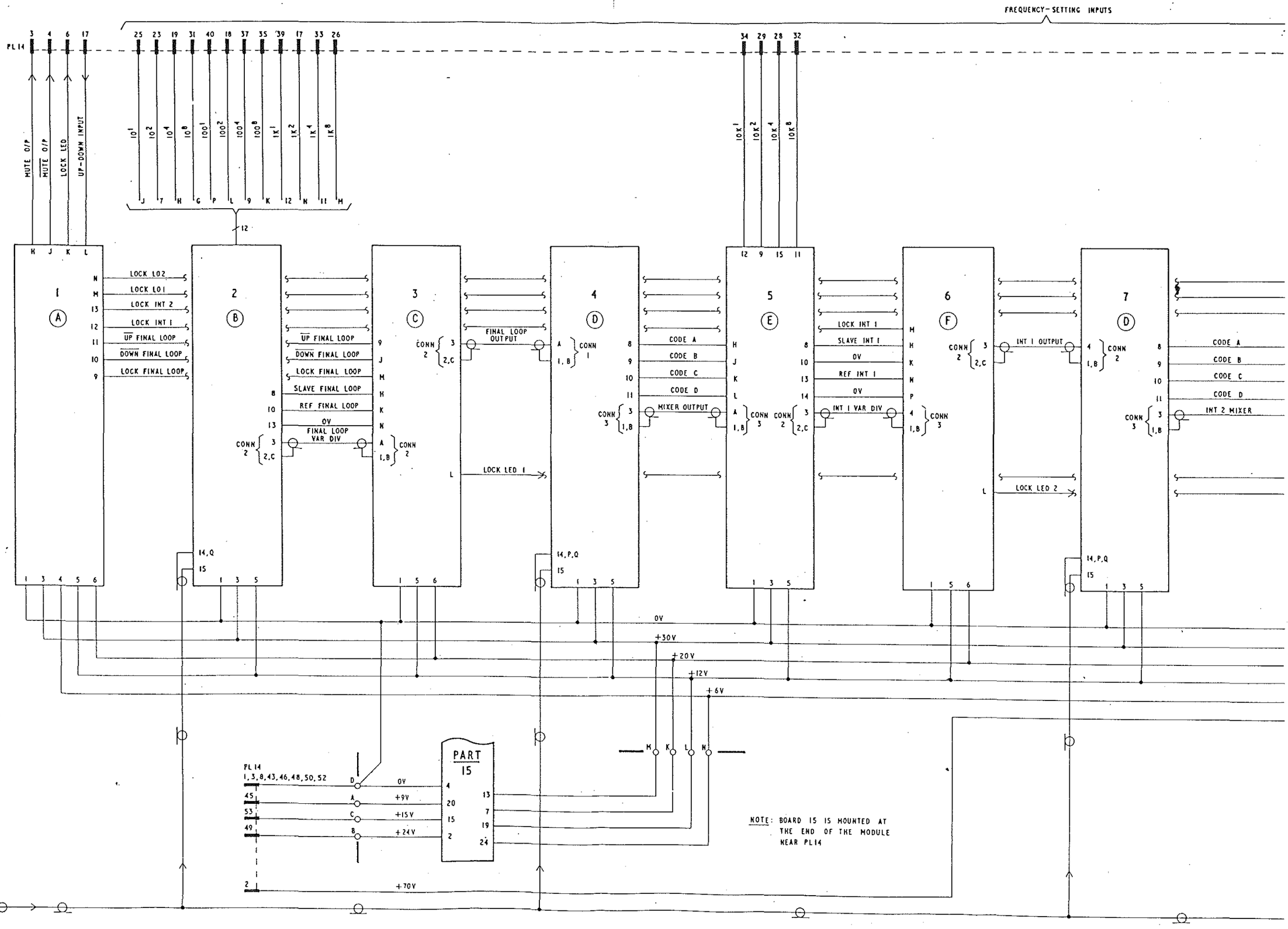
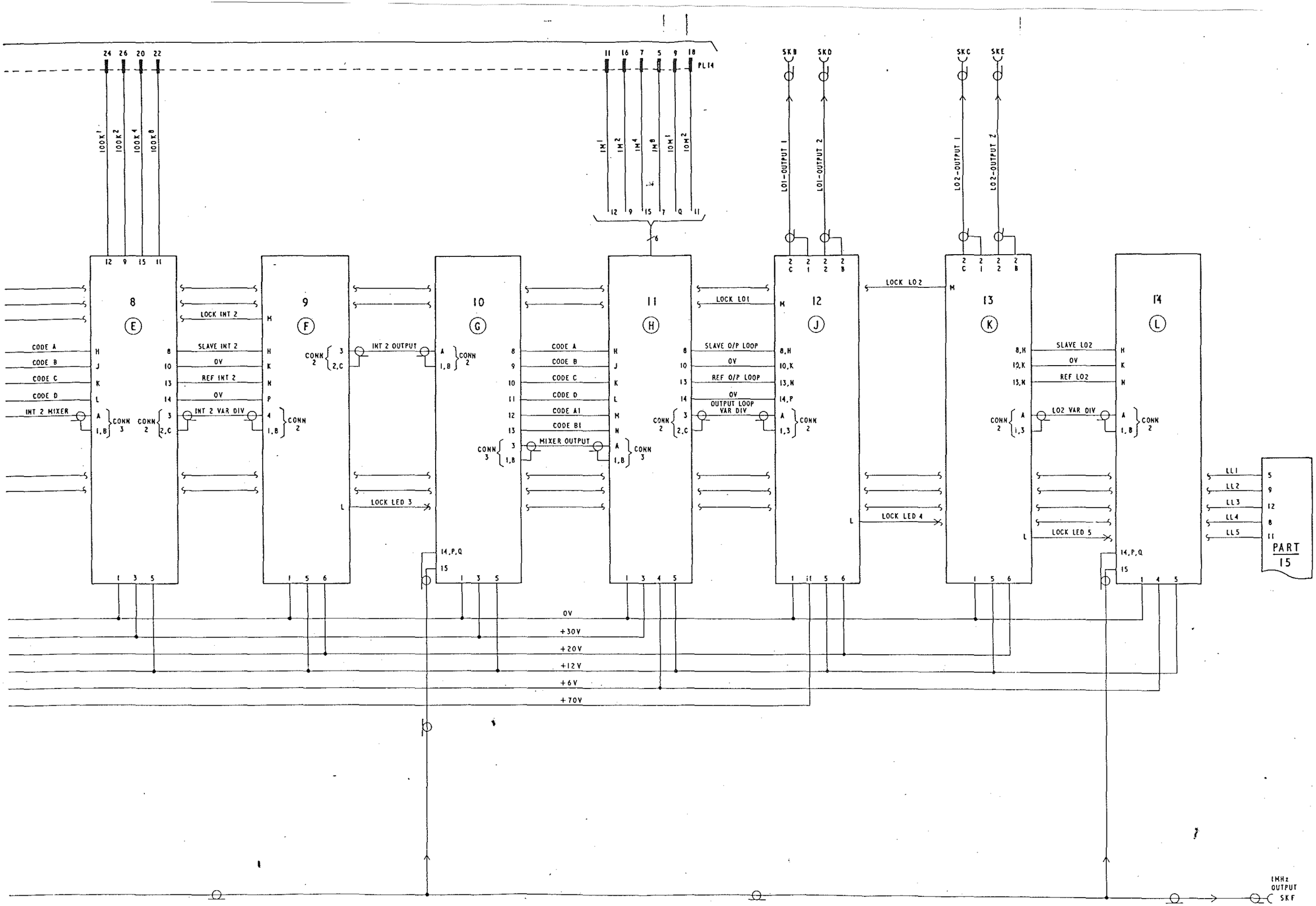


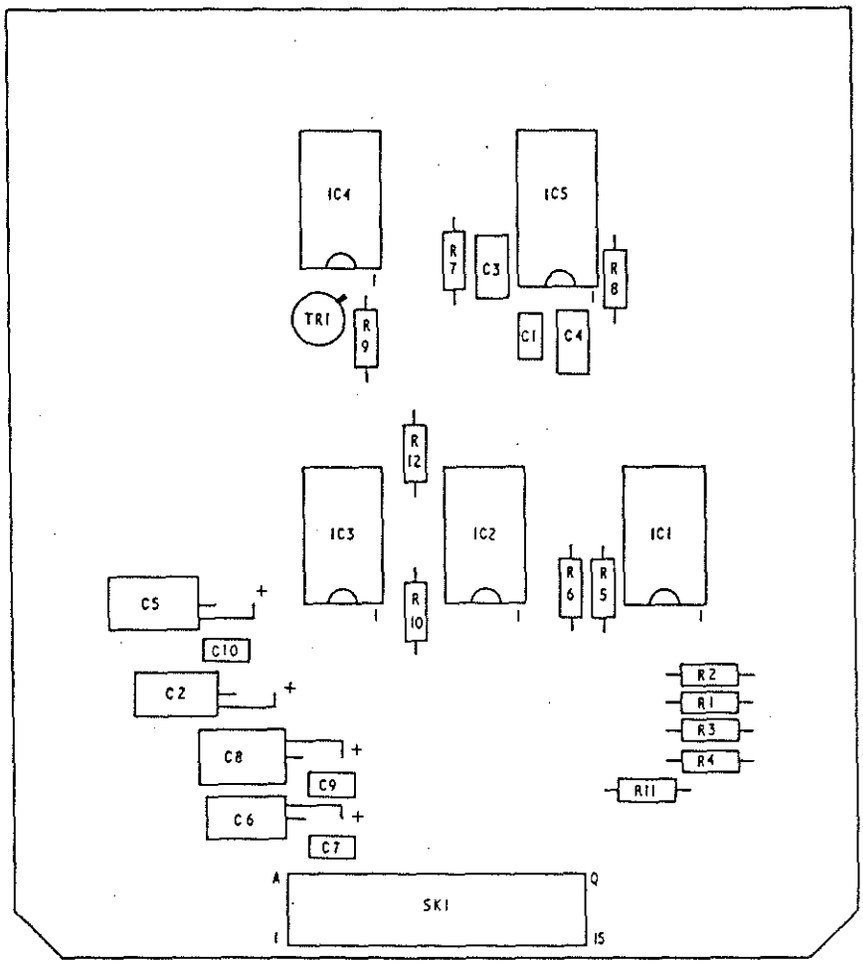
FIG 14

MODULE 9 : INTERCONNECTION DIAGRAM(a)



MODULE 9 : INTERCONNECTION DIAGRAM(b)

FIG 14



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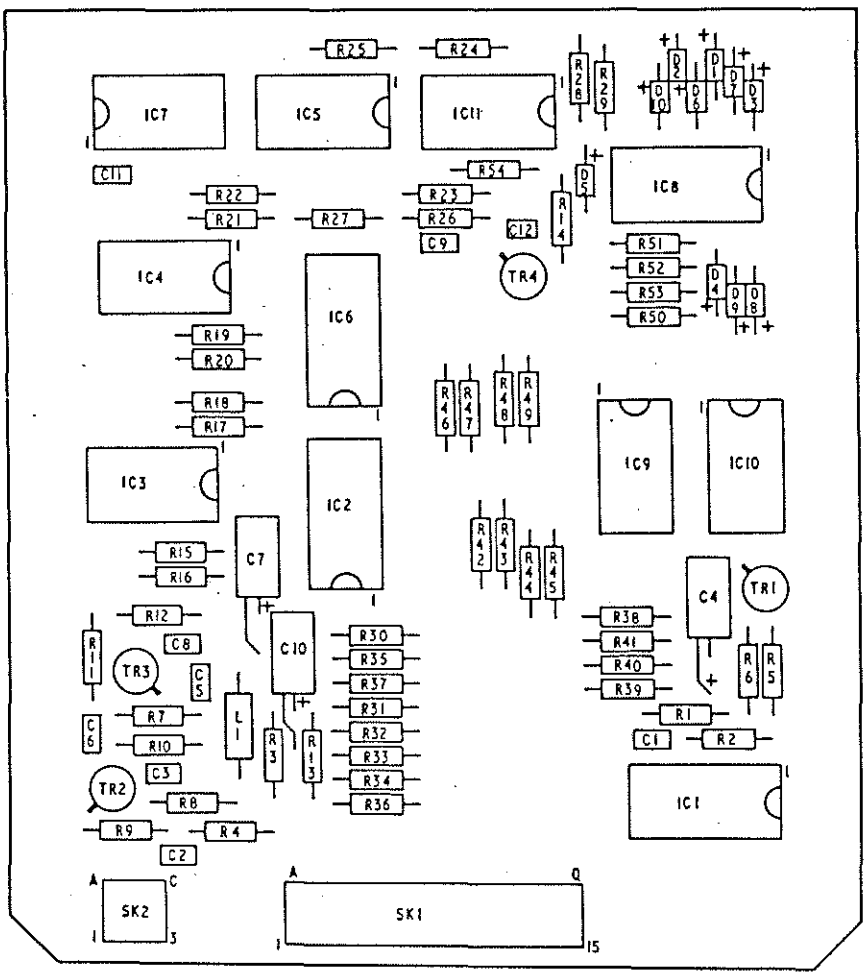
MODULE 9 PANEL A - COMPONENT LAYOUT

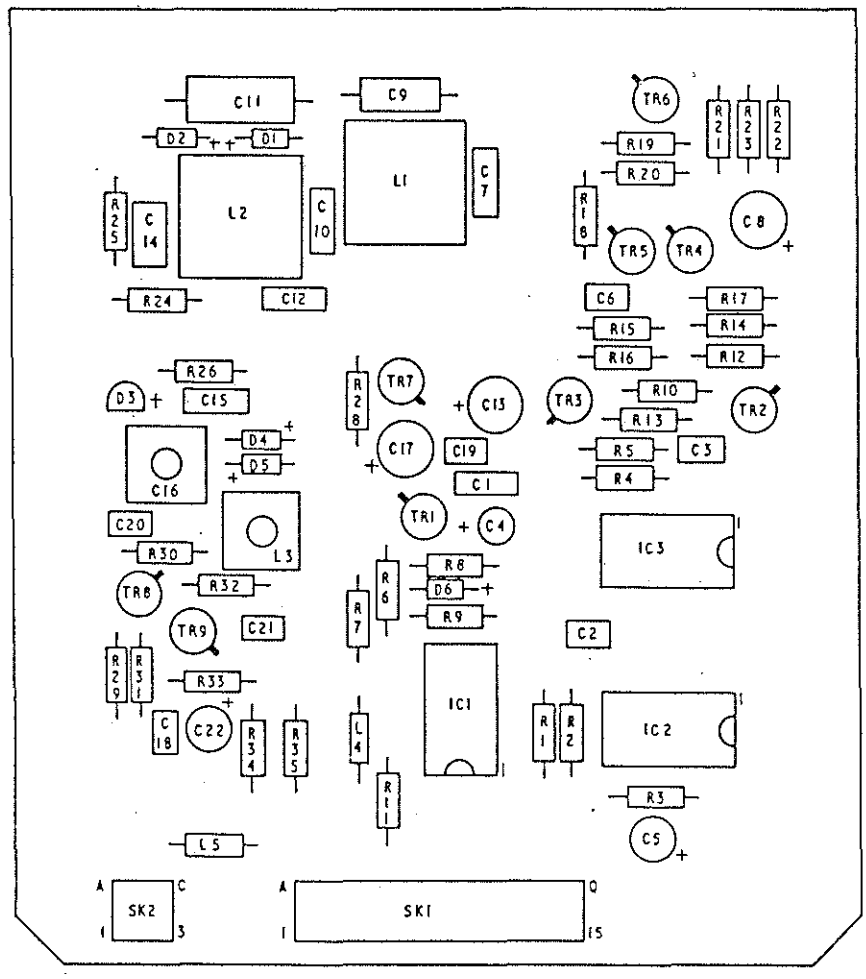
FIG. 15



419/1/18041 Iss A

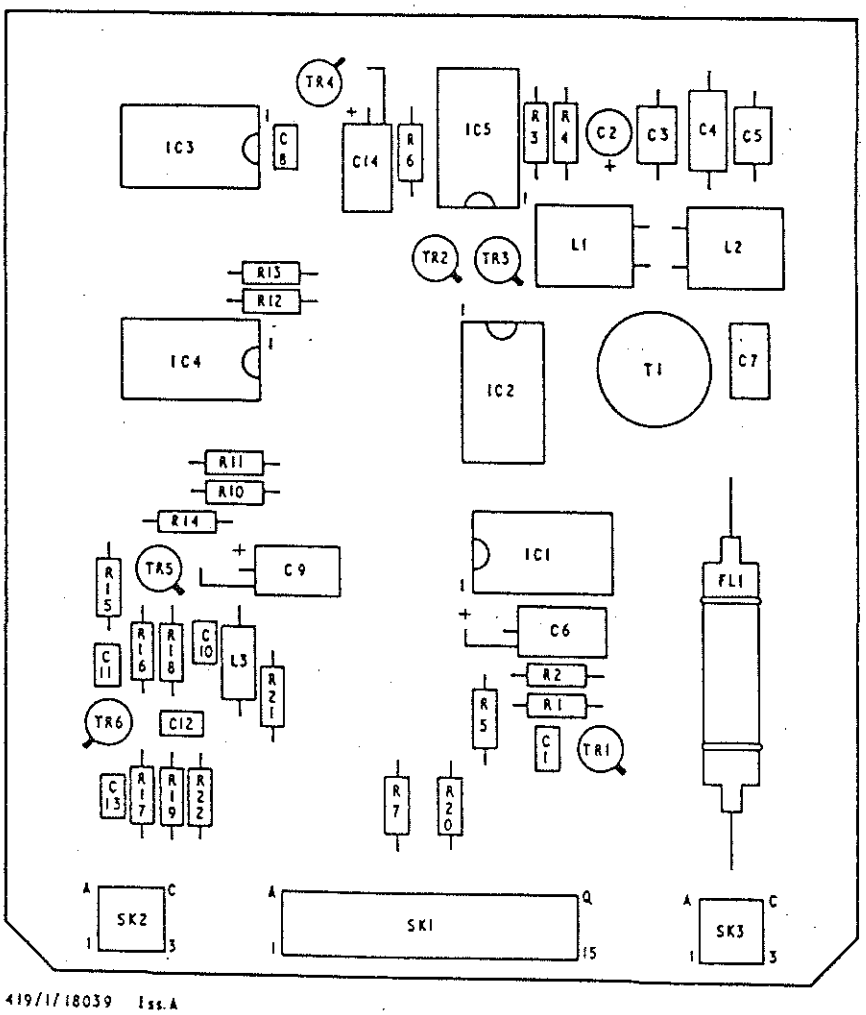
MODULE 9 PANEL B - COMPONENT LAYOUT

FIG. 16



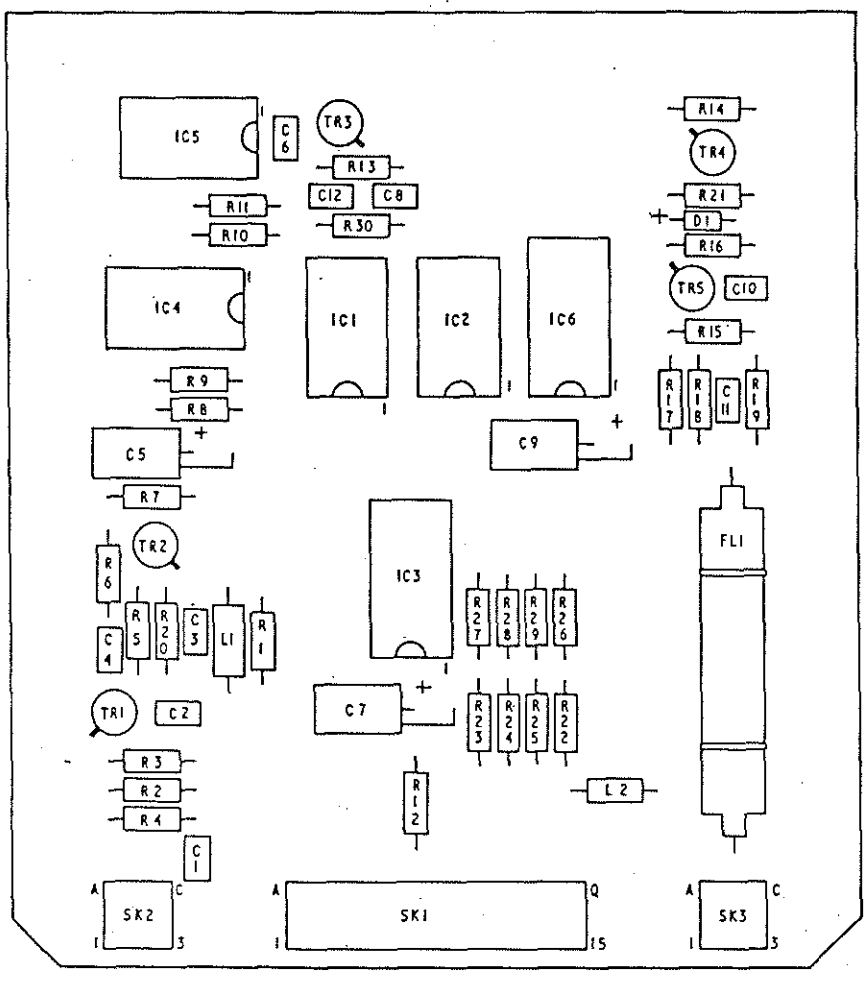
419/1/18043 Iss.A

MODULE 9 PANEL C - COMPONENT LAYOUT FIG. 17



MODULE 9 PANEL D - COMPONENT LAYOUT

FIG. 18



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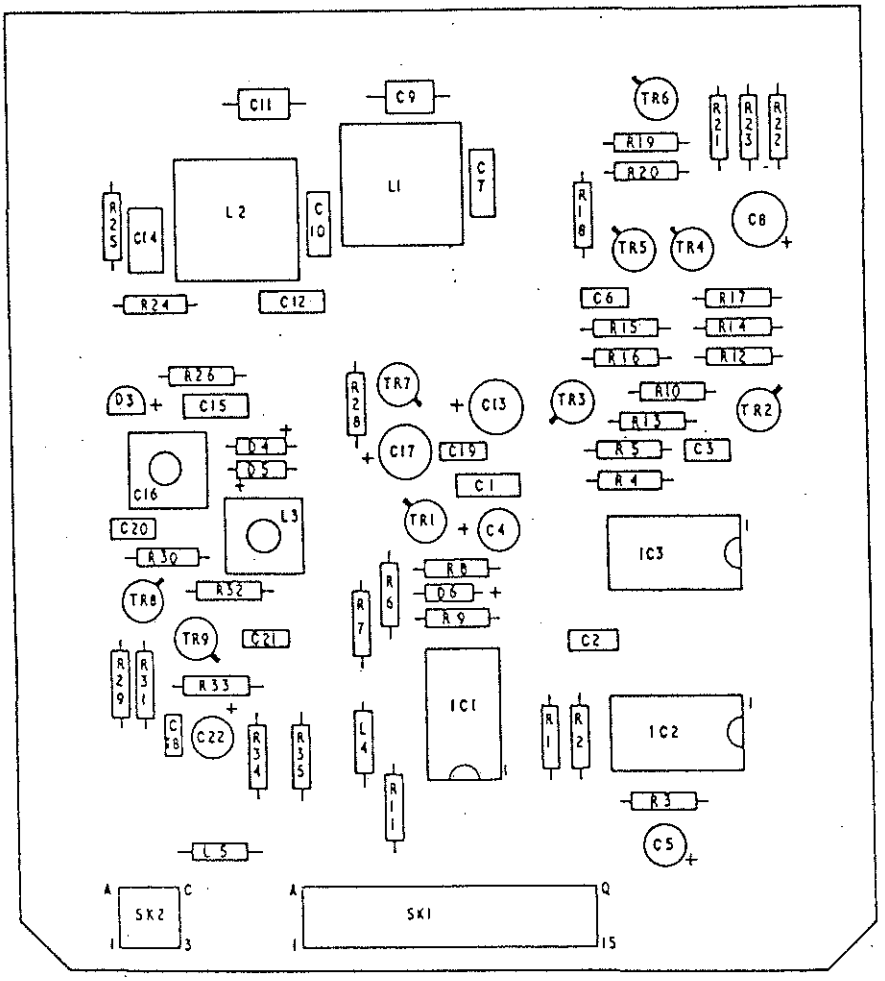
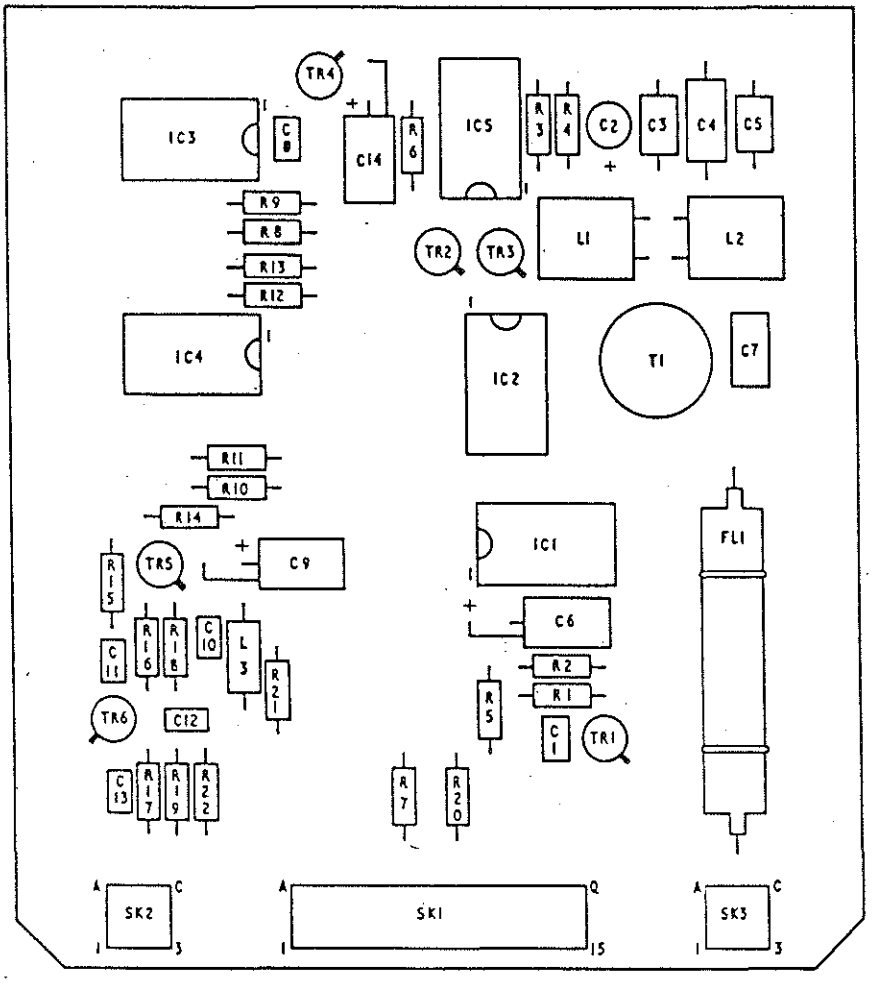
MODULE 9 PANEL E - COMPONENT LAYOUT FIG. 19



419/1/18057 Iss. A

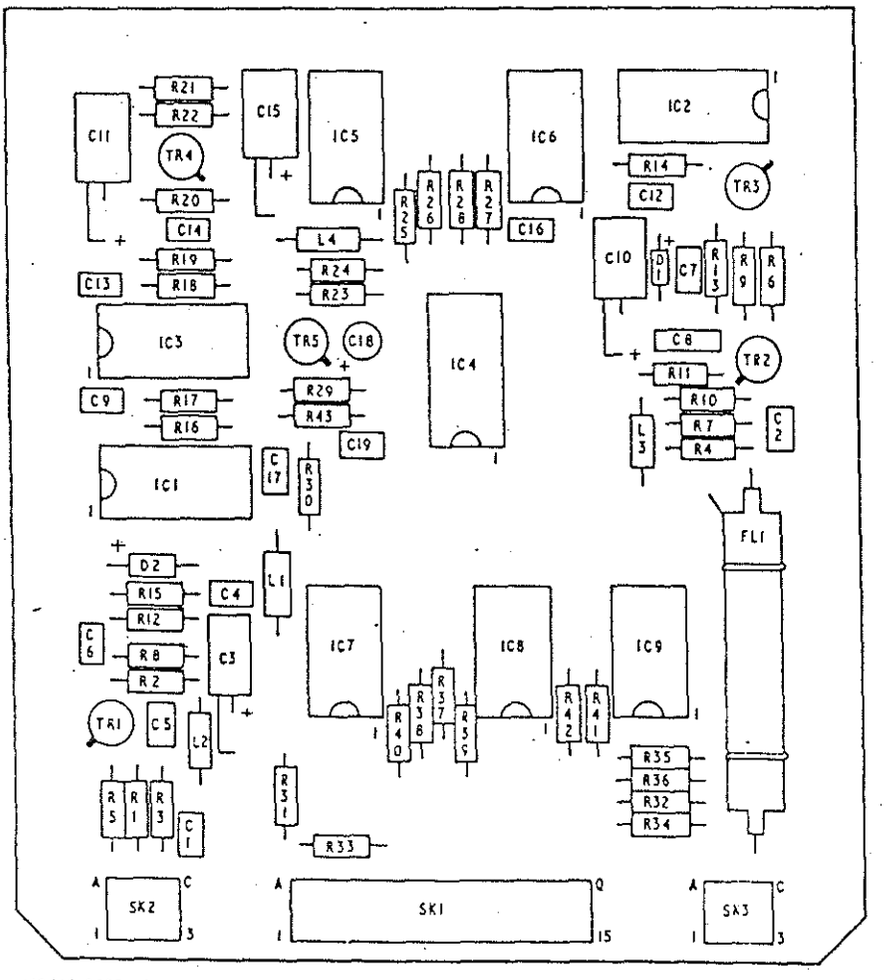
MODULE 9 PANEL F - COMPONENT LAYOUT

FIG. 20



419/1/18055 Iss. A

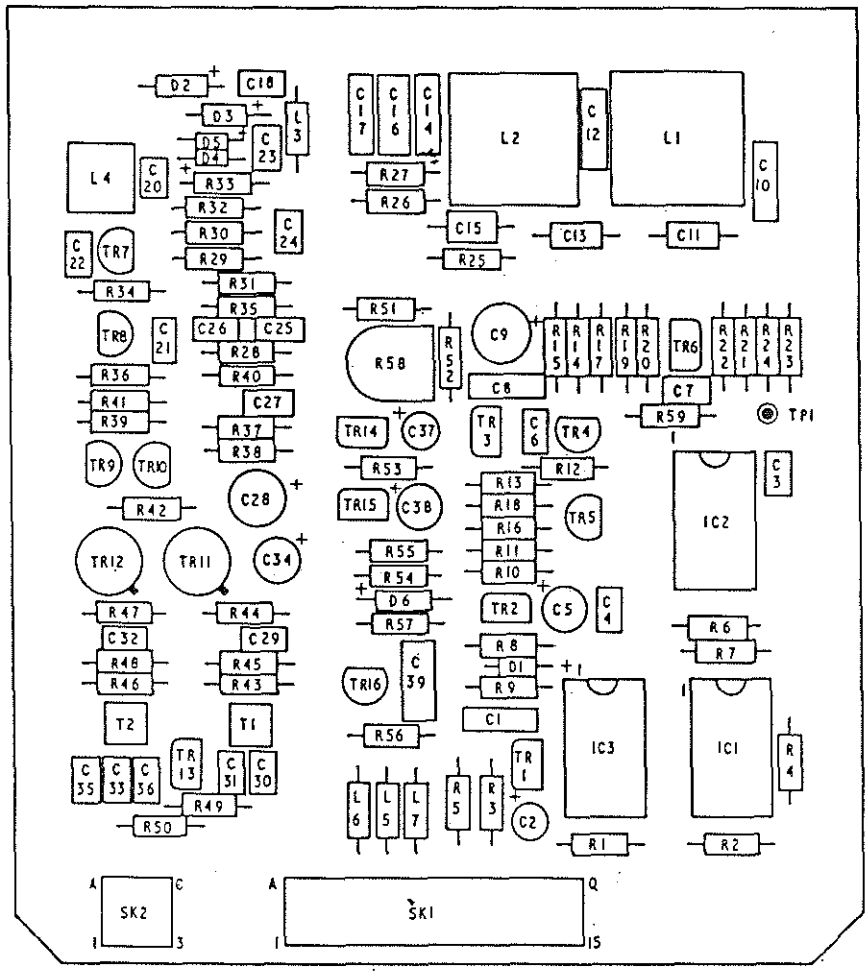
MODULE 9 PANEL G - COMPONENT LAYOUT FIG. 21



419/1/18035 Iss A

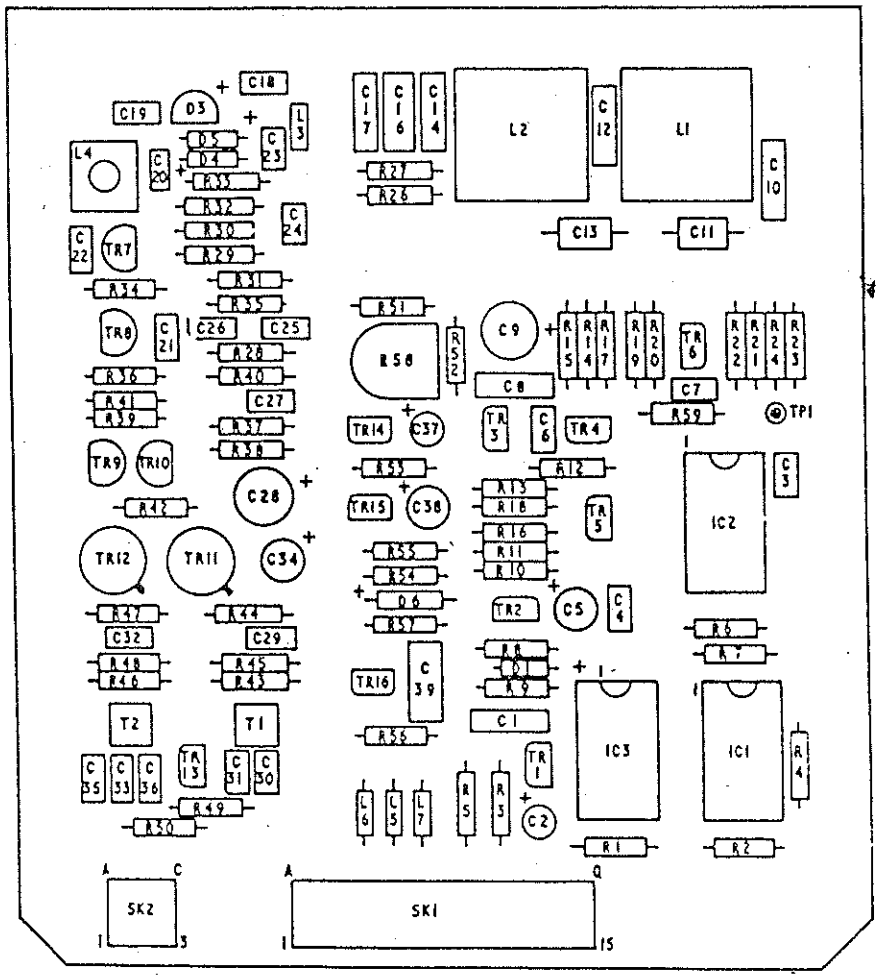
MODULE 9 PANEL H - COMPONENT LAYOUT

FIG. 22



419/1/18047 Iss. A

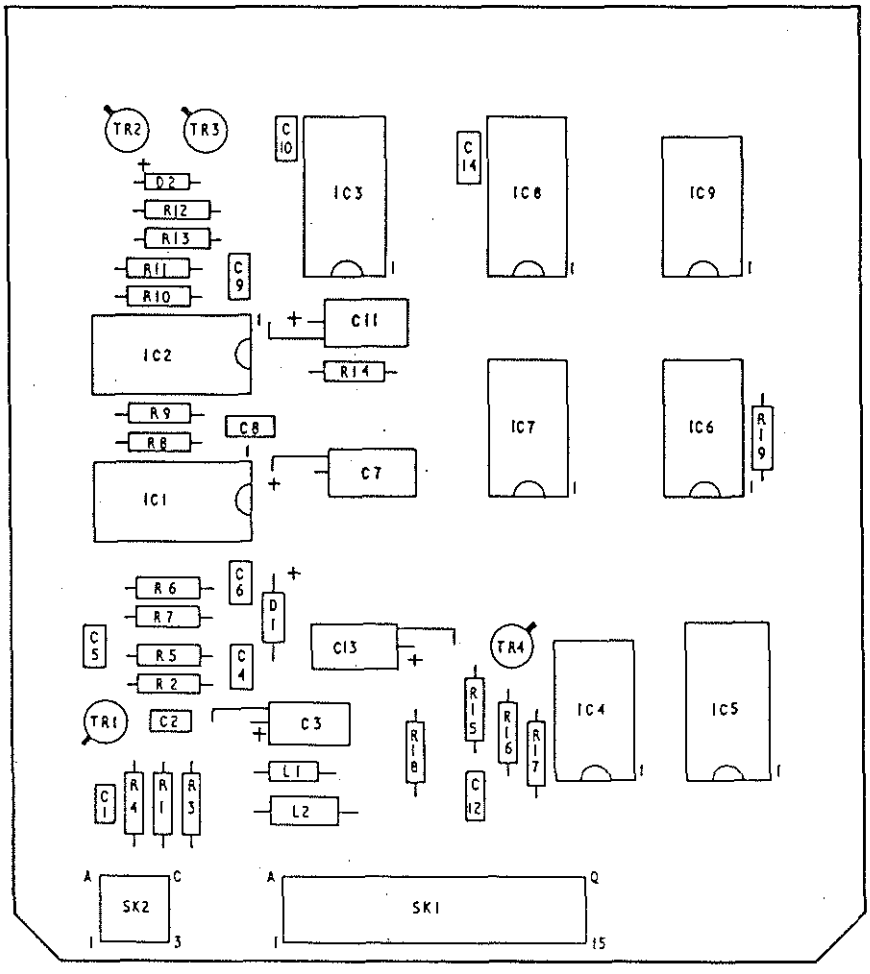
MODULE 9 PANEL J - COMPONENT LAYOUT FIG. 23



419/1/18059 Iss.A

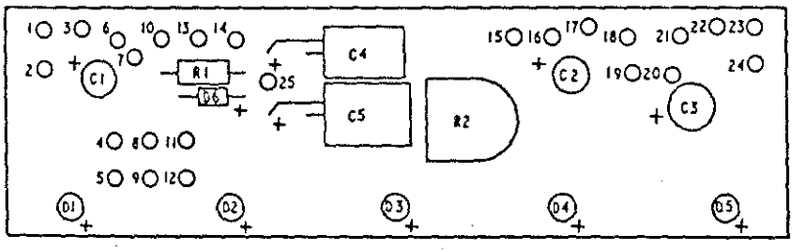
MODULE 9 PANEL K -COMPONENT LAYOUT

FIG. 24



419/1/18049 Iss. A

MODULE 9 PANEL L - COMPONENT LAYOUT FIG. 25



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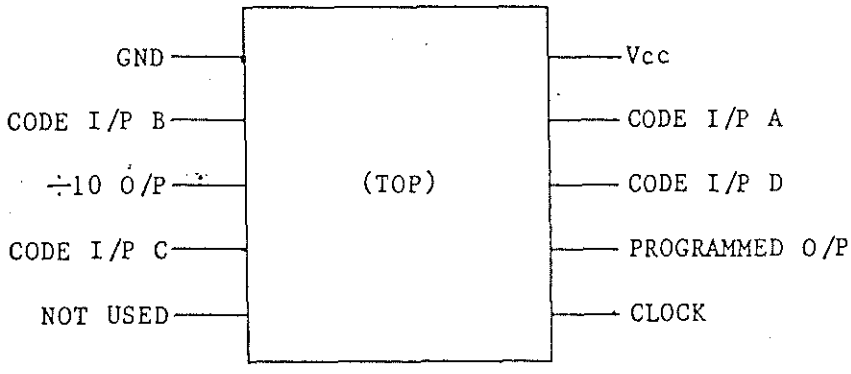
MODULE 9 REGULATOR PANEL - COMPONENT LAYOUT FIG. 26

INTEGRATED CIRCUIT DEFINITIONS

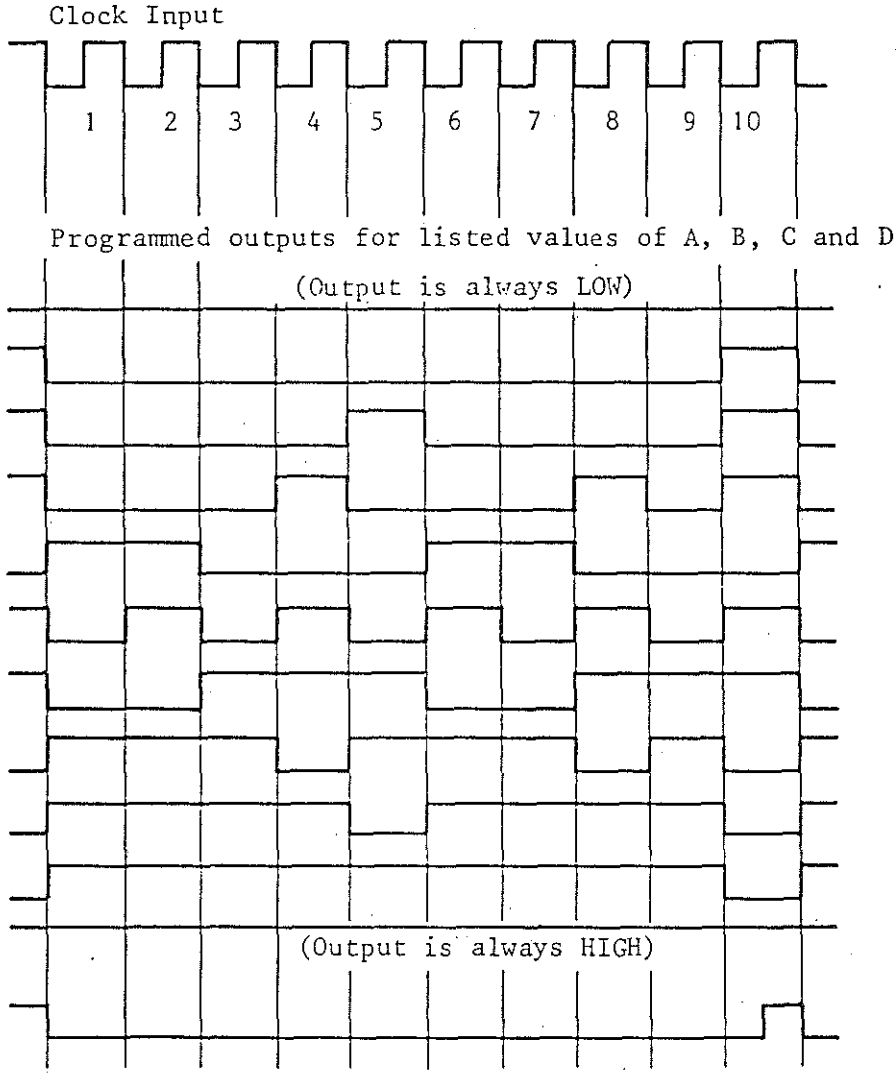
This information forms a supplement to the circuit diagrams in respect of complex integrated circuits which are shown diagrammatically by a rectangular outline only.

SP 8325

A clocked variable-waveform generator, controlled by levels applied to CODE I/P A, B, C, and D. Flat-pack i.c. as shown below.

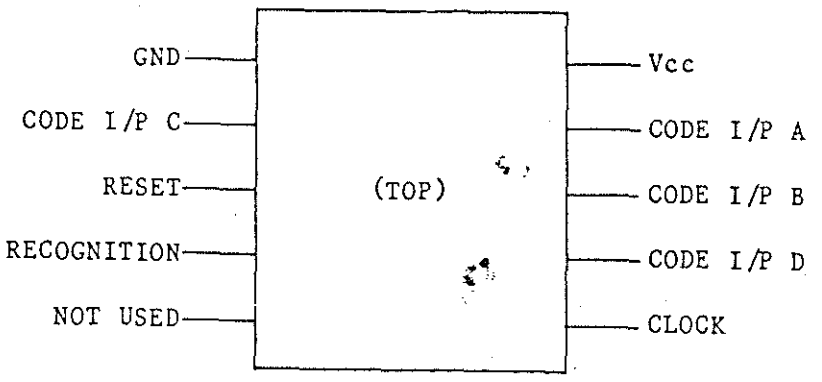


Code Inputs			
A	B	C	D
0	0	1	1
1	1	0	0
0	1	0	0
1	1	1	0
0	1	1	1
1	0	1	0
0	1	1	0
1	1	1	1
0	1	0	1
1	1	0	1
0	0	1	0
÷by ten output			

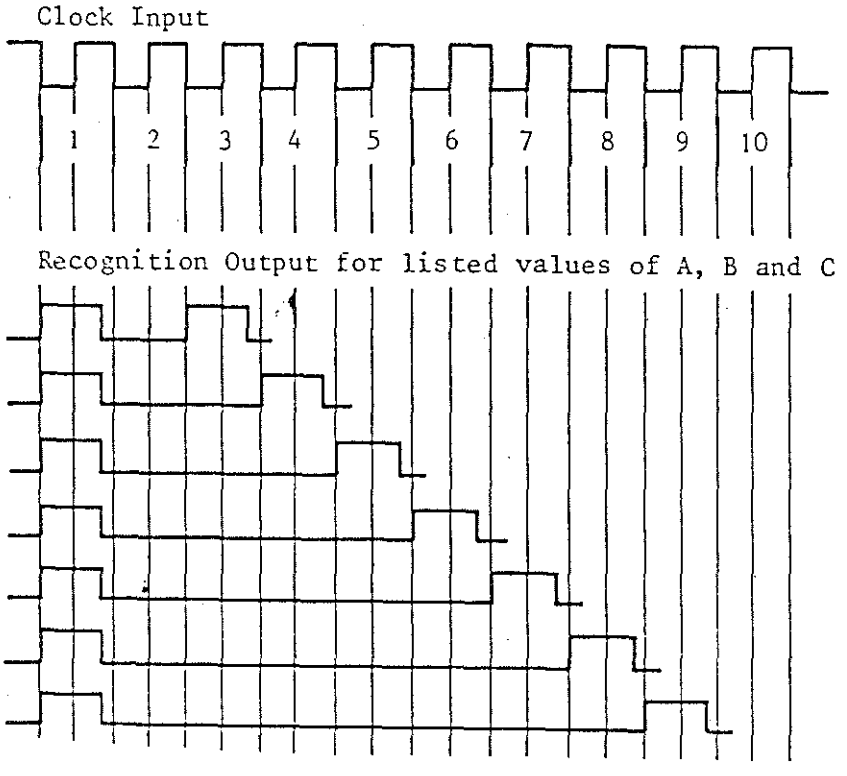


SP 8323

A Variable-ratio counter divider. Flat pack i.c. as shown below.

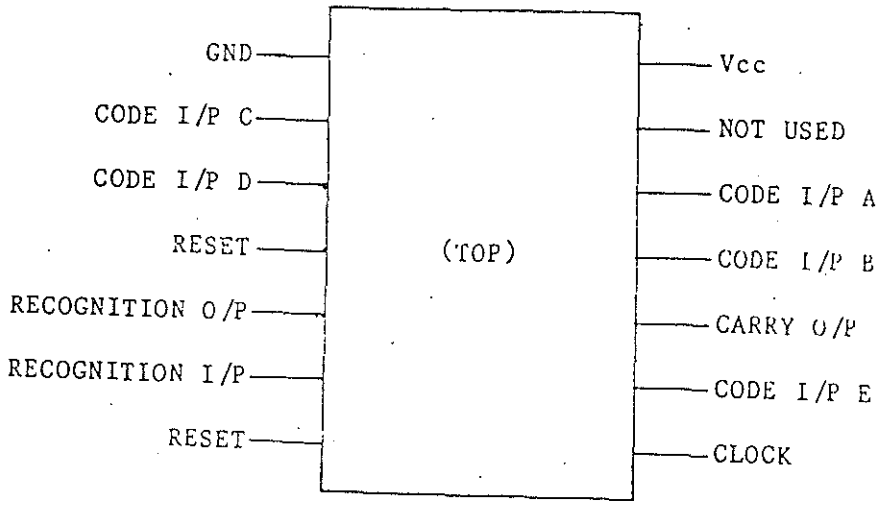


Code Inputs		
A	B	C
0	1	0
1	1	0
0	0	1
1	0	1
0	1	1
1	1	1
0	0	0

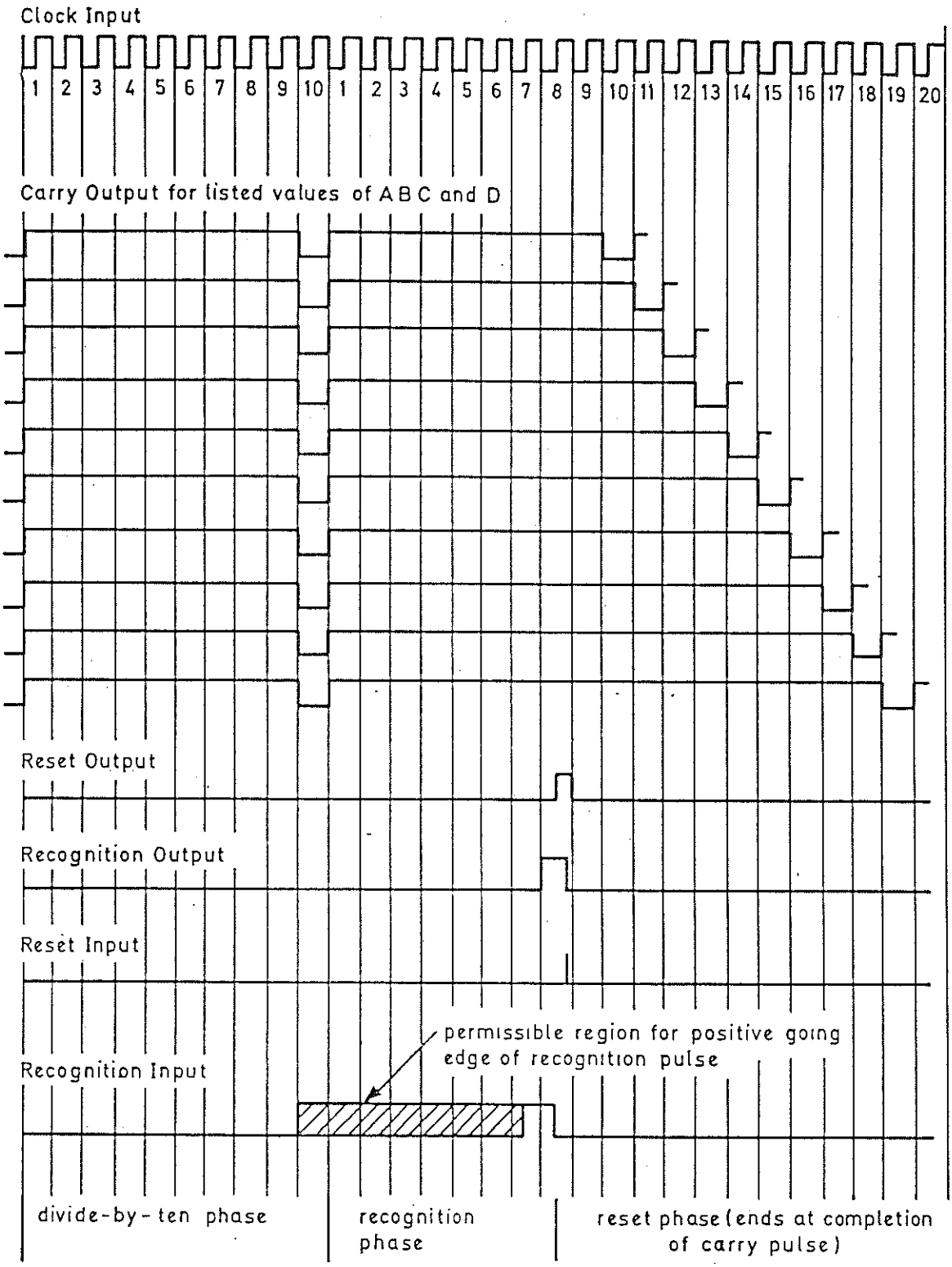


SP 8317

A variable-ratio counter-divider. Flat-pack i.c. as shown below.

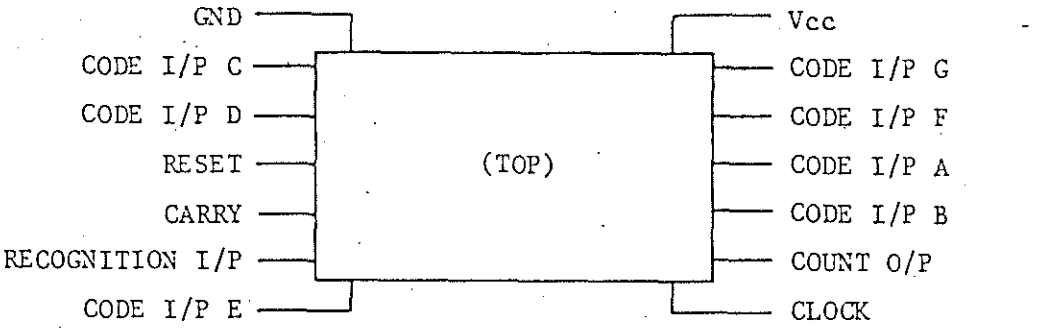


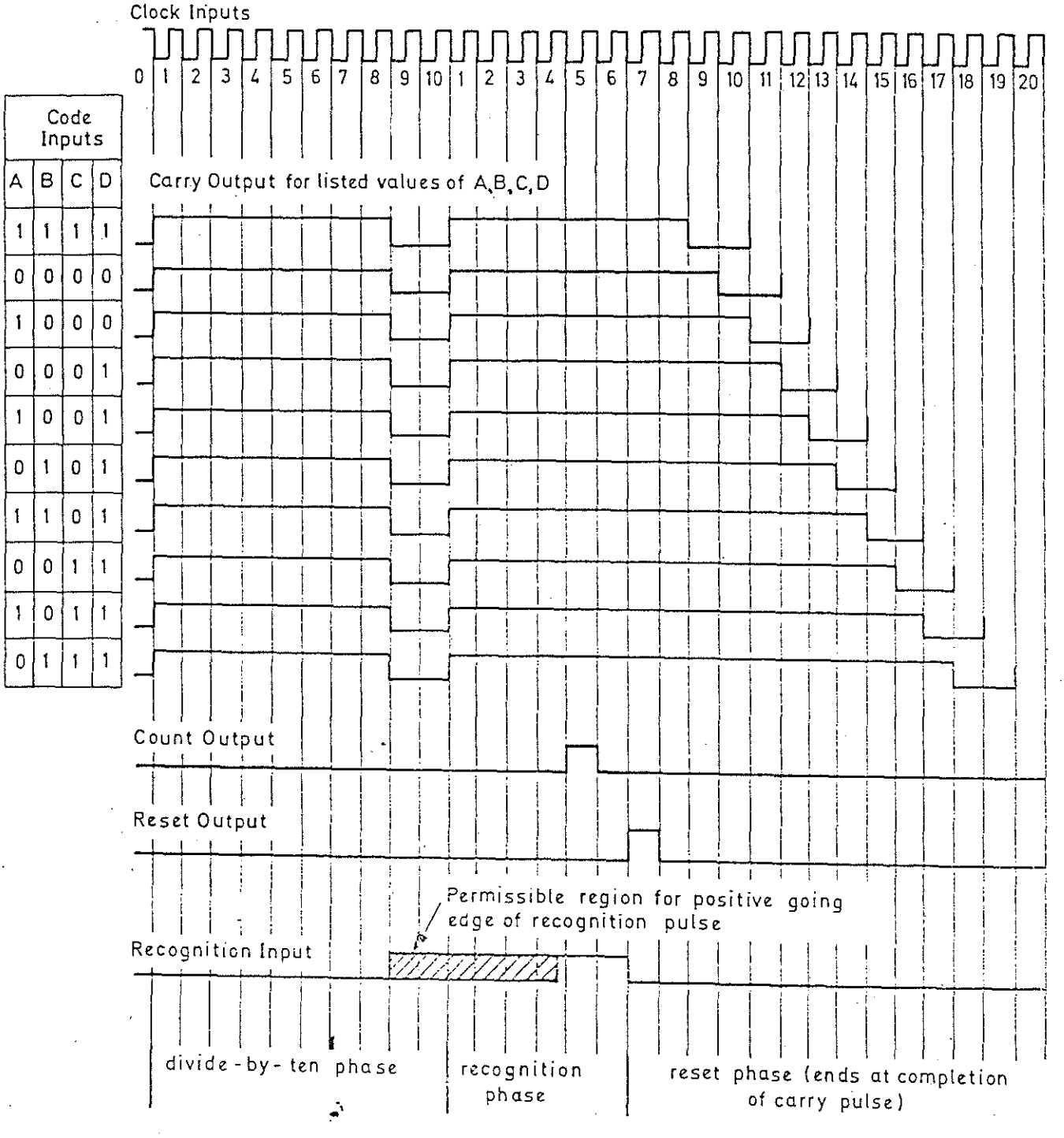
Code Inputs			
A	B	C	D
1	1	1	1
0	0	0	0
1	0	0	0
0	0	0	1
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	1



SP8311

A variable-ratio counter-divider. Flat-pack i.e. as shown below.





MC 10178

A 4-bit binary counter. With inputs R, S0, S1, S2, and S3 all at '0' a binary count up from '0' is produced on Q0 (LSB), Q1, Q2, Q3 (MSB) outputs. Count increments on positive-going edges to inputs C1 or C2 (or to both). Input R = '1' sets all Q outputs to '0'. Inputs S0, S1, S2, and S3 all at '1' sets all Q outputs to '1'. No count is produced if either C1 or C2 is held at '1'.

MC 14008

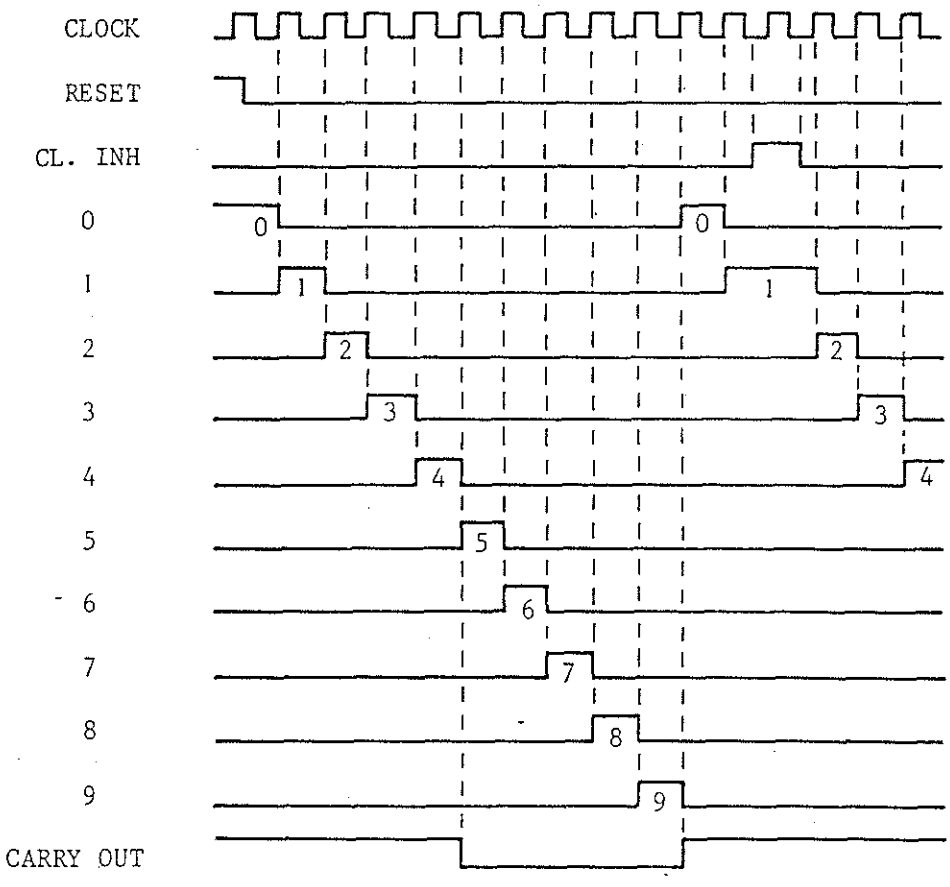
A 4-bit full adder. Forms the sum of inputs A + B + C_{IN}, where A and B are 4-bit numbers. Output sum is 5-bit full sum(S0, S1, S2, S3, C_{OUT}). C_{OUT} = 0 if full sum ≤ 15.

MC 10138

A 4-bit counter producing a binary output on Q1 (LSB), Q2, Q3, Q0 (MSB). Action as MC 10178.

CD 4017

A 5-stage Johnson counter. Clockpulses are counted and decoded to produce outputs as shown below.



CHAPTER 10

MODULE 10 FRONT PANEL AND CONTROL CIRCUITS

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ILLUSTRATIONS

ILLUSTRATIONS (Cont'd)

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MODULE 10 FRONT PANEL AND CONTROL CIRCUITS

1. INTRODUCTION

1.1 The name 'Module 10' embraces the front-panel of a PR2250 receiver and the circuit-board mounted upon it. These two items together embody all the digital logic which forms the interface between the operator and the receiver proper. The logic operates in conjunction with memory circuits contained in either Module 11 or Module 12, whichever is fitted. Where Module 12 is fitted, remote control of the receiver can be exercised. Modules 10A and 10B are dealt with in paragraphs 8 and 9.

2. BASIC FUNCTIONAL DESCRIPTION (Figure (a))

2.1 Frequency Control

The operator controls frequency either by means of an entry on the keypad or by use of the manual tuning control. He can also recall a frequency stored in the memory. The manual tuning control operates an optical encoder. These controls produce inputs to the tuning logic. Two control outputs to the receiver are produced by the tuning logic: the first is a frequency-determining input to the synthesiser (1st L.O.), while the second selects an input filter (in Module 1) appropriate to the frequency set in by the operator. The second output is not used in receivers fitted with Module 1A. In addition, a frequency data output is fed to the memory circuits.

2.2 Mode and Bandwidth Control

Mode and Bandwidth controls are to a certain extent interdependent, inasmuch as selecting some modes automatically selects and appropriate bandwidth. However, where this is so the automatically selected bandwidth setting can be later over-ridden if desired. The mode and bandwidth logic produces a memory output, in addition to control outputs to the mode and bandwidth circuits.

2.3 AGC Control

AGC decay time-constant is operator selected. The selected value is fed to the AGC Circuits and to the memory.

2.4 Memory Control

The memory has 16 storage channels. One is reserved for 'temporary dump' use, while the remaining 15 are available for long-term storage. The memory is battery maintained, and will hold data for several months while the receiver is switched off. Recall facilities allow any stored set of data to be instantly applied to the receiver controls.

2.5 Remote Control

Where Module 12 is fitted to a receiver, remote control can be exercised via the 'memory' output lines to the logic circuits of Module 10. This control can perform all operations available on a normal PR2250 front-panel. In PR2252 receivers, Module 10B is fitted: in this module, no operator controls are fitted, and all control operations are carried out via Module 12. The logic circuits are identical with those of Module 10 except that all operations are initiated from the 'memory' lines.

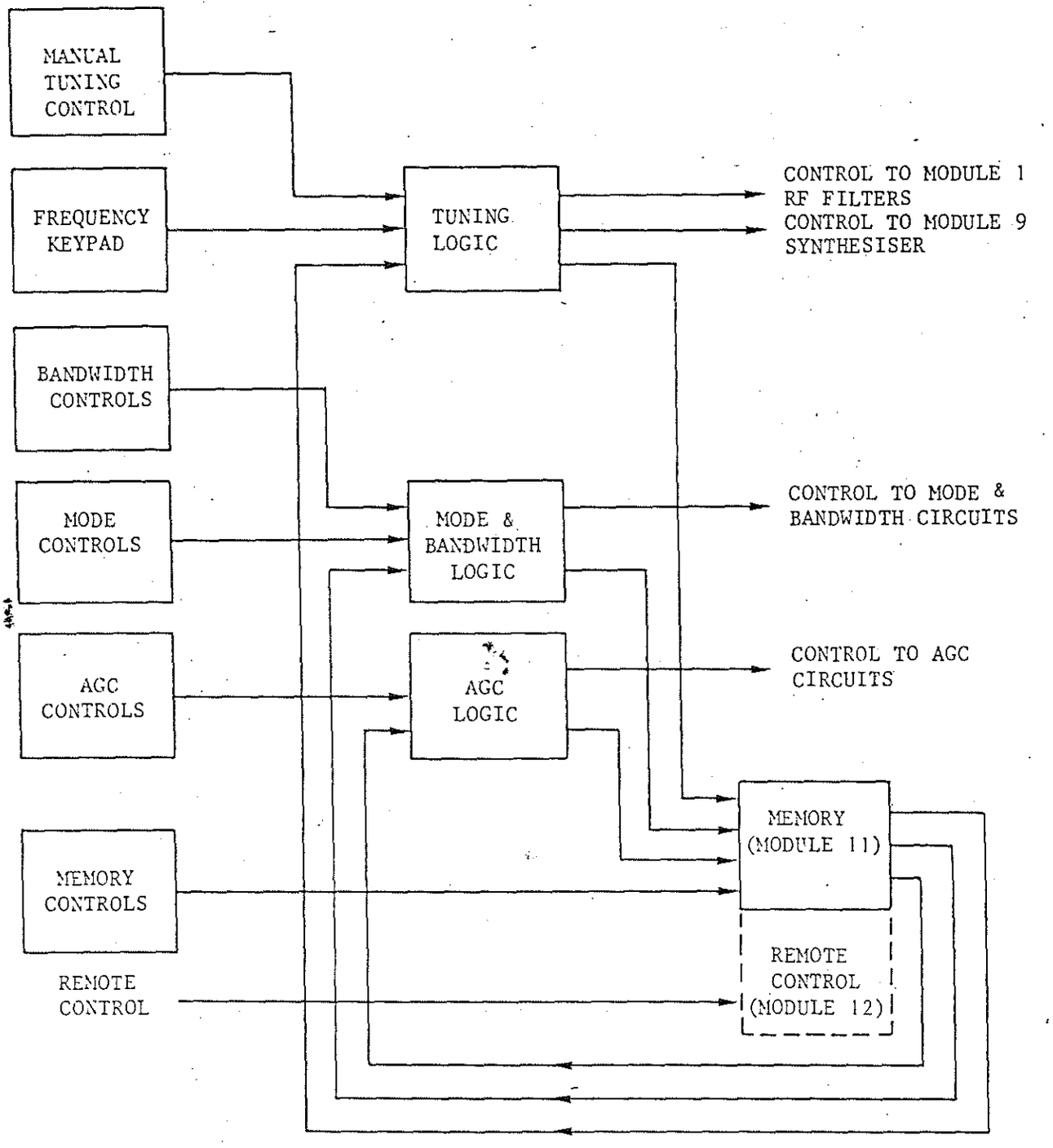
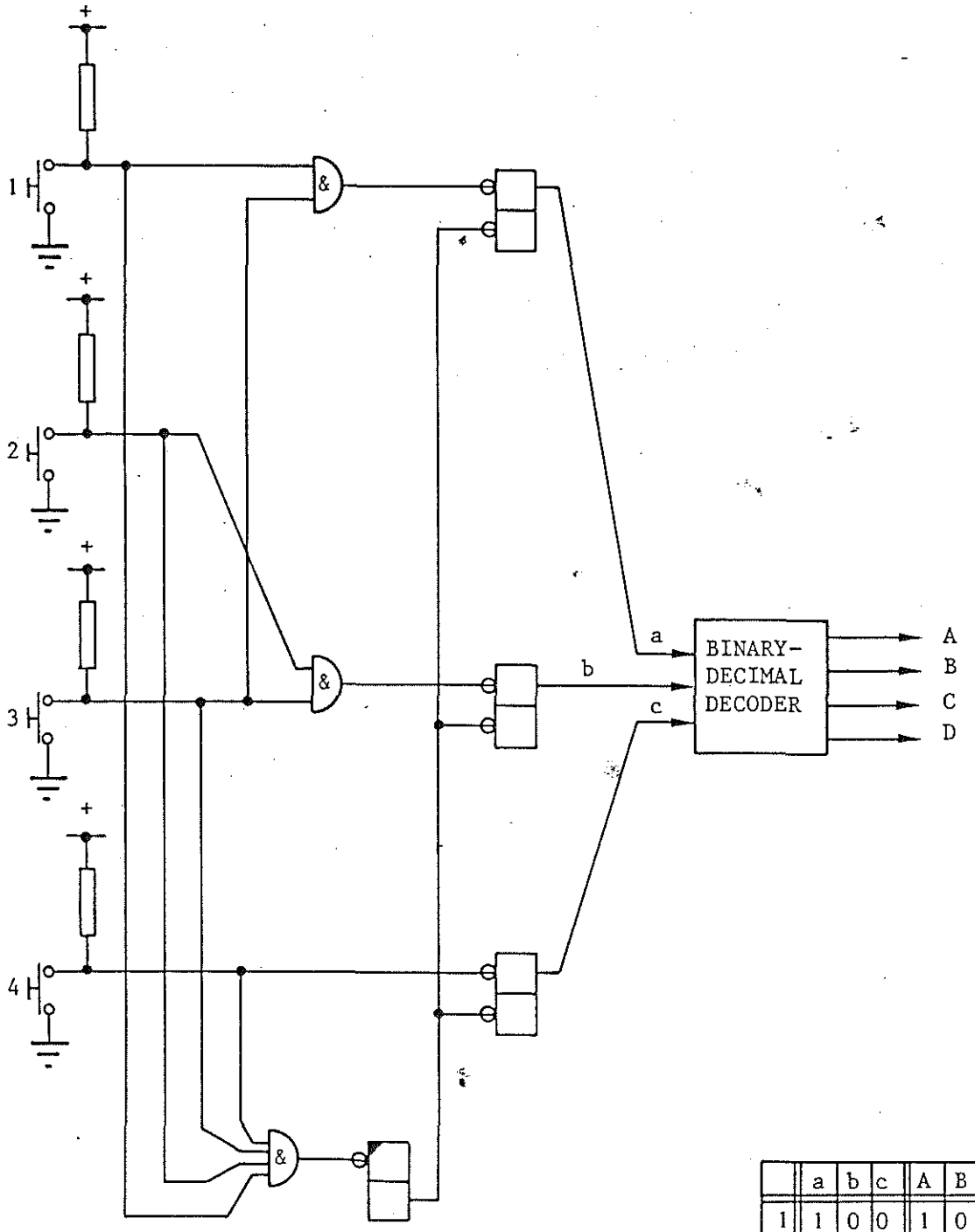


FIG (a) MODULE 10 (FRONT PANEL) BASIC FUNCTIONAL DIAGRAM

3. PUSH-BUTTON CONTROL

3.1 Apart from the manual tuning and a few switches, all operator controls are 'press to operate' buttons. The basic system can be seen in Figure (b). Operation of any button triggers the monostable, producing a very



	a	b	c	A	B	C	D
1	1	0	0	1	0	0	0
2	0	1	0	0	1	0	0
3	1	1	0	0	0	1	0
4	0	0	1	0	0	0	1

FIG (b) BASIC PUSH-BUTTON SYSTEM

NOTE: Example shows 4 buttons: the only difference for a full 0-9 keypad is in the gating to produce a 4-bit parallel binary input to the decoder.

short '1-0-1' output pulse and also applying a '0' set level to one or more bistables. Those bistables which do not receive a '0' set level are reset by the monostable output pulse, which ends before the operator releases the button. In the period between the end of the monostable output pulse and the button release, one or more bistables are set.

3.2 In Figure (b), a four-button circuit is shown. Button 1 produces binary 1 at a, b, c, Button 2 produces binary 2, and so on. The binary number set into the bistables is decoded to produce a '1' level on one output of the decoder. The system is applicable to, any number of buttons by use of suitable 'AND' gating and sufficient bistables to store the largest binary number required.

3.3 As an example, Push-Button 4 in Figure (b). The monostable produces a short '1-0-1' pulse which resets the upper two bistables. It cannot reset the lower bistable because of the '0' set level applied by Button 4. After the end of the monostable output pulse, the button will still be held. During this period, the lower bistable is set, producing a=0, b=0, c=1, i.e. binary 4 in parallel form. This binary 4 will remain stored in the bistables until another button is pressed: it is decoded to produce a '1' output on line D.

4. FREQUENCY CONTROL - DESCRIPTION

4.1 Keypad - Functional Description

4.1.1 A functional diagram of the keypad circuit is shown in Figure 1: all logic is reduced to basic functions. The 0-9 numerical keypad and the ENTER and CLEAR controls are push-buttons of the type described in paragraph 7. The circuit as a whole is an extension of the basic circuit shown in Figure (b). The keypad, ENTER, and CLEAR inputs can also be supplied by the memory.

4.1.2 Assume a number is entered from the keypad. Each key operation produces a 4-bit parallel binary number at points A, B, C, D; A is the least significant bit. All keypad inputs are applied to an 'OR' function which fires a monostable: a single strobe pulse is therefore produced for each key operation.

4.1.3 A 'single number' entry first appears on the Q0 outputs of shift registers IC26 to 29. If the entry produces a '1' level at the Q0 outputs of both IC28 and IC29, the entry must have been a decimal point. This fact is recognised by IC25C producing a '1' level output.

4.1.4 Successive keypad entries shift the 4-bit parallel binary numbers one stage along the shift registers for each entry. If, for example, 862 had been entered, the 8 would be on the Q2 outputs, the 6 would be on the Q1 outputs, and the 2 would be on the Q0 outputs.

4.1.5 If then the decimal point key is pressed, which must be done to make a valid frequency entry, the fact is recognised by IC25C sensing IC28 and IC29 Q0 levels at '1': this sets B3$\overline{Q}$ level to '1'. The resultant '0' level at B3Q then prevents further decimal point entries from having any effect. Whether further numerical entries were or were not made after the decimal point entry does not affect the operation so, for simplicity, we will assume there were none.

4.1.6 The next operation is to press the ENTER button. This in conjunction with B3Q level at '1', (due to decimal point entry), sets B1Q level to

'1'. As the Q5 levels of the shift registers cannot be all '1's, IC30B output level is '1' and the '1' level from B1Q sets B2$\overline{Q}$ to '1'. This allows the strobe oscillator to run, clocking the shift registers. When the decimal point (1-1-1-1) reaches the Q5 outputs from the shift registers, IC30B output level drops from '1' to '0' and sets B2$\overline{Q}$ level back to '0'. The strobe oscillator stops. The entries made on the keypad are now in the correct positions in the shift registers to operate the display decoders and produce a meaningful output to the synthesiser. This is done via BCD up/down counters which, for keypad entries, merely act as stores.

4.1.7 At the same time as the strobe oscillator stops, the combination of IC30B output at '0' and B1Q output at '1' has three effects:

(1) The two monostables are fired. The first one applies preset to the up-down counters (IC8 to 14), allowing the register outputs to appear on the counter outputs: IC17 to 21 are normally transparent to data. The second monostable, a little later, resets the shift registers ready for the next entry.

(2) B1Q level is set to '0', which is the start state for another operation.

(3) B3Q level is set to '1', which is the start state for another operation.

4.1.8 The connection between the shift registers and the up/down counters is made via transfer gates which are normally transparent to data. Their function is to break the connection when clearing an erroneous keypad entry. If, after a keypad numerical entry has been made but before the ENTER button is operated, it is desired to 'start again', the CLEAR button is pressed. This functions exactly as the enter button but with one additional action. The additional action is to disable the transfer gates and therefore prevent the erroneous entry from appearing at the counter outputs.

4.1.9 IC14 of the counter handles the '10MHz' digit. This must not exceed 2, as the maximum frequency is 29.99999MHz. An 'OVER 2' detector therefore continually senses the output from IC14: if it exceeds binary 2 due to erroneous keypad entry, the detector resets IC14 to produce either binary 0 or binary 2. This brings the output within the frequency range of the receiver.

4.1.10 The manual tuning control is applied to the up/down and clock inputs of the up-down counters. This is dealt with in paragraph 4.3 et. seq.

4.1.11 The outputs of the up-down counters are in the form of a parallel BCD number defining frequency in kHz. The output is fed to four places, namely:-

(1) Synthesiser frequency control input

(2) LED decoders of the front-panel frequency display.

(3) Filter-switching logic controlling Module 1

(4) Memory circuits of Module 11 (or Module 12)

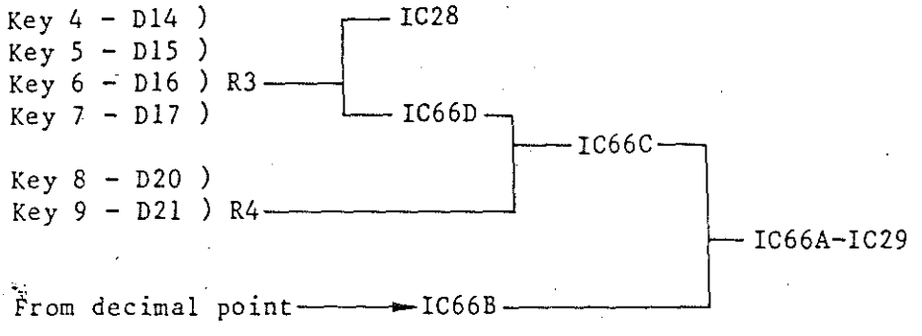
4.2 Keypad - Circuit Description

4.2.1 The circuitry of the keypad function is shown in Figure 2. Reference can also be made to the functional diagram, Figure 1. The keypad 0 to 9 and 'Decimal Point' inputs from the operator controls produce a logic '1' (positive) output when a key is pressed. This is opposite to the remainder of the push-button controls of the receiver, which produce logic '0' (0V) outputs when pressed.

4.2.2 Operation of any numerical key produces the appropriate 4-bit parallel binary number on the inputs to shift registers IC26, IC27, IC28 and IC29 (least significant bit to IC26). The gating functions (see Figure 3) which produce all inputs except '0' to the shift registers are made up as follows:-

Key 1 - D1)
Key 3 - D2)
Key 5 - D3) R1 - IC26
Key 7 - D4)
Key 9 - D5)

Key 2 - D8)
Key 3 - D9) R2 - IC27
Key 6 - D10)
Key 7 - D11)



4.2.3 The zero key is connected to one input of a 5-input 'OR' function formed by D24, D7, D13, D19, and D23 with R5. The other four inputs are connected to the keypad inputs to IC26, IC27, IC28, and IC29. The output from this OR function fires a monostable formed by IC62A and IC62B, as shown in Figure (c) on the facing page.

Note: that D97 also forms part of this 'OR' function, but is not immediately relevant. It is dealt with in para.4.2.12.

A short '0-1-0 input pulse produces a delayed '1-0-1' output pulse from IC2B $\overline{Q}$.

4.2.4 Consider the output across R5 produced by the 'OR' function. For any binary number between 1 and 9, at least one of the shift register inputs must be '1', and therefore a '1' level will appear on R5. Similarly, operation of the zero key will cause a '1' level to appear on R5. Therefore operation of any numerical key will fire the monostable. The output pulse produced by IC26B is applied as strobe to shift registers IC26, 27, 28, and 29: a single shift register strobe pulse is therefore produced for each numerical key operation. Monostable IC62 delays the strobe pulse to allow any front-panel button contact bounce to die out.

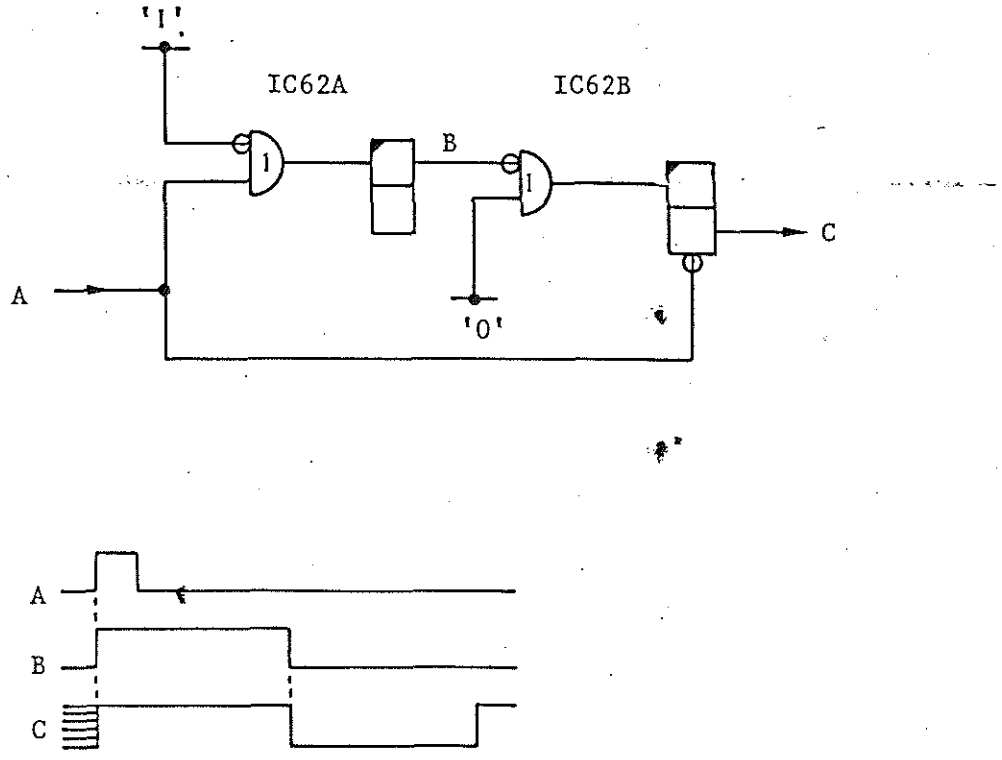


FIG (c) IC62 MONOSTABLE FUNCTION

4.2.5 A single numerical key operation produces an equivalent 4-bit binary number on the Q0 outputs of the four shift register IC's. A second operation shifts this number to the Q1 outputs, and presents a second equivalent binary number on the Q0 outputs. The cycle repeats for each numerical key operation. Operation of the decimal point key produces the same action, and in addition is recognised by IC25C. This recognition depends upon the fact that, as the decimal point is '1-1-1-1', it is the only key input which produces a '1-1' input combination to IC25C. The resultant '0' output from IC25C sets the output level of set-reset bistable IC25A/IC25B to '1' and this level, inverted by IC16B, holds TR1 base at 0V via D81. In consequence, further operations of the decimal point key have no effect; the circuit prevents more than one decimal point being applied in one set of entries. For reasons which will be described later, it is necessary that each set of entries contains a decimal point: for example, while 1636.4 contains a decimal point naturally, 1878 does not, and therefore must be entered as '1878.'.

4.2.6 The longest entry which can be made (because of the 10Hz minimum frequency step) is xxxxx.xxkHz. This contains eight key operations (seven numerical and one decimal point), and fixes the shift register capacity at eight for each stage (Q0 to Q7 inclusive). The Q5 stages of each register IC are connected to a 4-input 'NAND' gate (IC 30B) which recognises a '1-1-1-1' combination on the four Q5 lines. A '1-1-1-1' combination is produced by a decimal point. For any shift register content to be meaningful to the frequency control and display circuits, it must appear at the shift register output with the decimal point on the Q5 outputs. Obviously this only occurs directly from an eight-operation entry, and therefore means of shifting entries of less than eight operations must be provided.

4.2.7 After a numerical entry has been made, the ENTER key is pressed, applying a '1' level via D96 to IC63D. The initial recognition of a decimal point

by IC25C has set IC25B pin 4 level to '1', therefore operation of the ENTER key produced a '1-1' input combination to IC63D. The resultant '0' output level sets IC63A pin 3 level to '1'.

4.2.8 The output from Q5 detector IC30B is at present '1', unless an eight-operation entry has been made. IC30B output and IC63A output produce a '1-1' input combination in IC64C, setting IC64D output level to '1'. This '1' level, applied to IC65B, allows the oscillator formed by IC65A and IC65B to run. Its output, via IC30A, clocks the shift register until the decimal point appears on the Q5 outputs. At this point, IC30B output level changes from '1' to '0'.

4.2.9 A '0' output level from IC30B has the following effects:

(1) IC30A output level becomes '1', preventing further clockpulses from reaching the shift registers.

(2) Via IC63B and IC64A, it resets IC64D output level to '0', so stopping the oscillator.

(3) Via IC65D, it produces a '1-1' input, combination on IC65C: this produces:

(a) a '0-1' transition at IC25D output which fires monostables IC31A and IC31B.

(b) a '0' output from IC16C which resets IC25B and IC63A output levels to '0'.

4.2.10 The shift register output is now correctly placed, with the decimal point on the Q5 outputs. The ENTER circuit is reset ready for the next operation. If the numerical entry had been of eight operations, the same action would have occurred except for the running of oscillator IC65A - IC65B: this would have been prevented by the '0' output from IC30B produced by the decimal point on the shift register Q5 outputs.

4.2.11 The operation of monostables IC31A and IC31B produces two successive '0-1-0' pulses: the leading edge of IC31B Q output coincides with the trailing edge of IC31A Q output. The first '0-1-0' pulse applies preset to the up-down counters (IC8 to IC14), allowing the register outputs to appear on the up-down counter outputs via transfer gates IC17 to IC21 which are normally transparent to data. The second '0-1-0' pulse resets the shift register ready for the next entry.

4.2.12 The transfer gates are, as has been stated, normally transparent to data. Their function is to break the connection between shift registers and up-down counter when clearing an erroneous keypad entry and when data is being entered from the memory. If, after a numerical entry has been made (but before ENTER has been pressed) it is desired to cancel the entry, the CLEAR button is operated. The CLEAR and ENTER buttons are both connected to an OR function formed by D87, D96, and R8, and therefore have identical effects via IC63D. However, the CLEAR input via R9, D37, and D88 also applies a disabling '1' input to the transfer gates; with this input applied, the gates present open-circuit outputs. Additionally, the CLEAR input via D85 simulates a decimal point to 'complete' the erroneous entry which is being cleared.

4.2.13 The up-down counter consists of IC8 to IC14 inclusive. It simply acts as a store in respect of keypad and memory entries: the counter action is

used solely in conjunction with the output from the manual tuning control (q.v. in paras.4.3 and 4.4.

4.2.14 As the P2 (pin 13) and P3 (pin 3) presetting inputs to IC14 are tied to 0V (logic '0') by R16 and R17, the Q2 (pin 14) and Q3 (pin 2) outputs from IC14 cannot be changed from logic '0' by presetting inputs. These presetting inputs are 10M1 and 10M2 from the shift register (via the transfer gates), and are applied to IC14 pin 4 (P0) and pin 12 (P1): the 10M2 input to pin 12 is applied via OR gate IC22A, IC22B and delay circuit R19 C8. Hence, only the two least significant bits of the input '10MHz' number are applied: for keypad entries of 0, 4, and 8, binary 0 is applied. For keypad entries of 1, 5, and 9, binary 1 is applied. For keypad entries of 2 and 6, binary 2 is applied, and for keypad entries of 3 and 7 binary 3 is applied.

4.2.15 A correct keypad entry can only apply either 0, 1, or 2 to IC14; any other entry must be erroneous, as the highest frequency which can be correctly entered is 29.9999MHz. Erroneous entries of a '10MHz' figure of 4, 5, 6, 8, or 9 are self correcting, as they will produce a response of either 0, 1, or 2: however, entries of 3 or 7 apply binary 3 to IC14, producing a Q0=1, Q1=1 output. This is sensed by IC15C which, via IC15D, produces a resetting '1' level to IC14 pin 9; Q0 and Q1 levels then fall to '0'. Therefore, keypad 'tens of MHz' entries from 0 to 9 produce displayed frequency figures as shown below:

ENTRY	0	1	2	3	4	5	6	7	8	9
DISPLAY	0	1	2	0	0	1	2	0	0	1

4.2.16 When the up-down counter is clocked from the manual tuning control (and also at switch-on), IC14 'Q' outputs can (in theory) assume any value up to binary 15 should the control be so operated. As previously described, IC15C will detect a '1-1' output combination on Q0 and Q1. A '1' level on Q2 is detected (via IC16F) by IC15D, and produces a resetting '1' level to IC14 pin 9 to reset Q0 and Q1 to '0'. Binary 3, 4, 5, 6 and 7 entries are therefore detected.

4.2.17 Gates IC15A, IC15B, IC16A, and IC16D form a set-reset bistable, the two inputs of which sense IC14 Q1 and Q3 levels to detect entries of 8 or 9. A '1' from IC14 Q3 (pin 2) sets IC15A output level to '1': this level, via IC22 (4 elements), applies a '1' level 'enable preset' to IC14 pin 1 and a '1' level preset input to IC14 pin 12 (P1). IC14 is therefore preset to Q3=0, Q2=0, Q1=1, and Q0 = the level applied from 10M1: an output binary number of either 2 or 3 is produced, therefore. Should binary 3 be produced, it will be immediately detected by IC15C; the resultant resetting action will immediately produce an output of binary 0. For an applied entry of 8, therefore, an output of binary 2 is obtained; for an applied entry of 9, an output of binary 0 is obtained.

4.2.18 The outputs from the up-down counters are fed out of Module 10 to the memory circuits and the frequency control circuits. Inside Module 10, they are applied to seven BCD 7-segment LED decoders (IC1 to IC7). These devices drive the front-panel frequency display. The decimal point on the display is a separate LED which is permanently illuminated via R57.

4.3 Manual Tuning - Functional Description (Figure (e))

4.3.1 The optical encoder driven by the manual tuning knob produces two square-wave outputs, 'Channel 1' and 'Channel 2'. These outputs have a 90° phase relationship. Each produces 500 pulses per revolution of the

manual control, i.e. 0.72° rotation per pulse. Two tuning rates are provided, 1kHz per revolution or 20kHz per revolution. In both cases, frequency changes in 10Hz steps.

4.3.2 The two encoder outputs are cleaned by trigger circuits and applied to inverters and CR differentiators. Each encoder output is therefore made available in four forms, as shown in Figure (d).

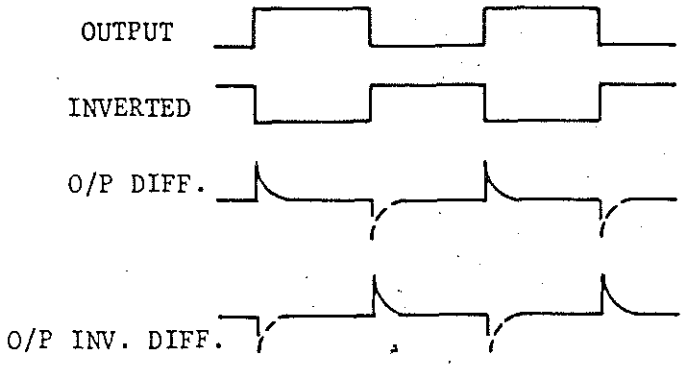


FIG (d) ENCODER OUTPUT PROCESSING

4.3.3 The four processed 'Channel 1' and four processed 'Channel 2' outputs are applied to two gating circuits. Two outputs are always produced: one is a train of '1-0-1' short pulses at four times encoder outputs pulse rate, while the second is a steady '1' level (Points A and B in Figure (e). Reversal of control rotation direction reverses the two states. The two outputs are applied to a set-reset bistable and to a NAND gate. The bistable $\overline{Q}$ output level indicates direction of rotation, while the pulse train indication of rotational speed and quantity appears at the output of the NAND gate. The action can be seen from the waveforms shown in Figure (f).

4.3.4 The output from the bistable is fed to the up-down inputs of IC8 to 14 (see Figure 1), while the output from the NAND gate is applied to the clock inputs of IC8 to 14. According to direction of control rotation, the numbers stored in the counters can be increased or decreased, so controlling the counter output values.

4.3.5 The 'SLOW' tuning rate of 20kHz per rev is provided by a 20 circuit which can be switched in after the NAND gate referred to in paragraph 4.3.3.

4.3.6 Manual tuning can be inhibited by a front-panel switch and is also inhibited when the receiver control is set to 'remote'.

4.4 Manual Tuning - Circuit Description

4.4.1 The optical encoder driven by the manual tuning knob is a sealed unit, receiving a 12V dc supply and producing two square-wave outputs, 'Channel 1' and 'Channel 2': these outputs have a 90° phase relationship and, at worst case, have a '1' level value of +11V and a '0' level value of +3V. On each channel, 500 pulses are produced per encoder revolution.

4.4.2 The two outputs from the encoder are 'cleaned' by trigger inverters IC40B and IC40D. Two further trigger inverters IC40A and IC40C provide inverted signals. The output from each of the four trigger inverters is app-

lied to a CR differentiation circuit. Each of the two encoder outputs is therefore available in four forms:

(a) direct

(b) inverted

(c) direct differentiated

(d) inverted differentiated

producing a total of eight inputs to a gating circuit formed by IC39 and IC45 together with D71-D78 and R78-R79. The action of this gating circuit is described in paragraphs 4.3.3 to 4.3.4 of the functional description. According to the direction of rotation of the manual control, the outputs across R78 and R79 are a train of '1-0-1' pulses at four times encoder output frequency and a steady '1' level. Reversal of rotation reverses the two outputs. Both are applied to IC34A, producing a corresponding train of '0-1-0' pulses from whichever channel is pulsing: this is the tuning control signal. Waveforms are shown in Figure (f).

4.4.3 Whichever of the two outputs across R78 and R79 is pulsing is seen by bistable IC34C-IC34D as a '0' level input and, in consequence, the output level of IC34D is either '1' or '0' depending upon direction of control rotation. It is applied to pin 10 (up-down) of each up-down counter: a '1' value is 'count up' (clockwise rotation) and a '0' value is 'count down' (anticlockwise rotation).

4.4.4 The tuning control signal from IC34A is fed via IC34B and IC24A to divide-by-twenty circuit IC23. It can be stopped at IC34B by application of a '0' level to pin 6. This level can be applied from either the INHIBIT switch below the tuning control, or from the REMOTE press-button (paralleled with a corresponding remote-control input, where applicable).

4.4.5 Divide-by-twenty circuit IC23 is a dual BCD counter with the MSB output of the first counter (pin 6) clocking the second counter. The second counter LSB output (pin 11) provides a pulse train at 1/20 of the frequency of that applied to pin 2 (1st counter clock). Output pulse-length from each counter is twice clockpulse length.

4.4.6 The output from IC23 pin 11 and the output from IC24A are both applied to IC24C. With IC23 pins 7 and 15 at '0', an output is produced from IC24D, and IC24B output is a steady '1' level. Under these conditions, IC38B output is at 1/20 the frequency of that of IC24A. With IC23 pins 7 and 15 at '1', IC23 is shut down and pin 11 is at a steady '0' level. IC24B allows the output from IC24A to pass to IC24C and IC38B, the output from which is at the same frequency as that from IC24A.

4.4.7 The control level applied to IC23 and IC24B is provided by the bistable formed by IC33A and IC33B. The bistable is set and reset by the FAST and SLOW buttons on the front-panel. Two LED indicators are driven via IC32 to indicate the selected state (either 1kHz or 20kHz tuning variation per revolution of the control knob).

4.4.8 The output from IC38B is applied to pin 15 of each IC in the up-down counter. According to whether the up-down output from IC34D is '1' or '0', the count value will be increased or decreased as the manual

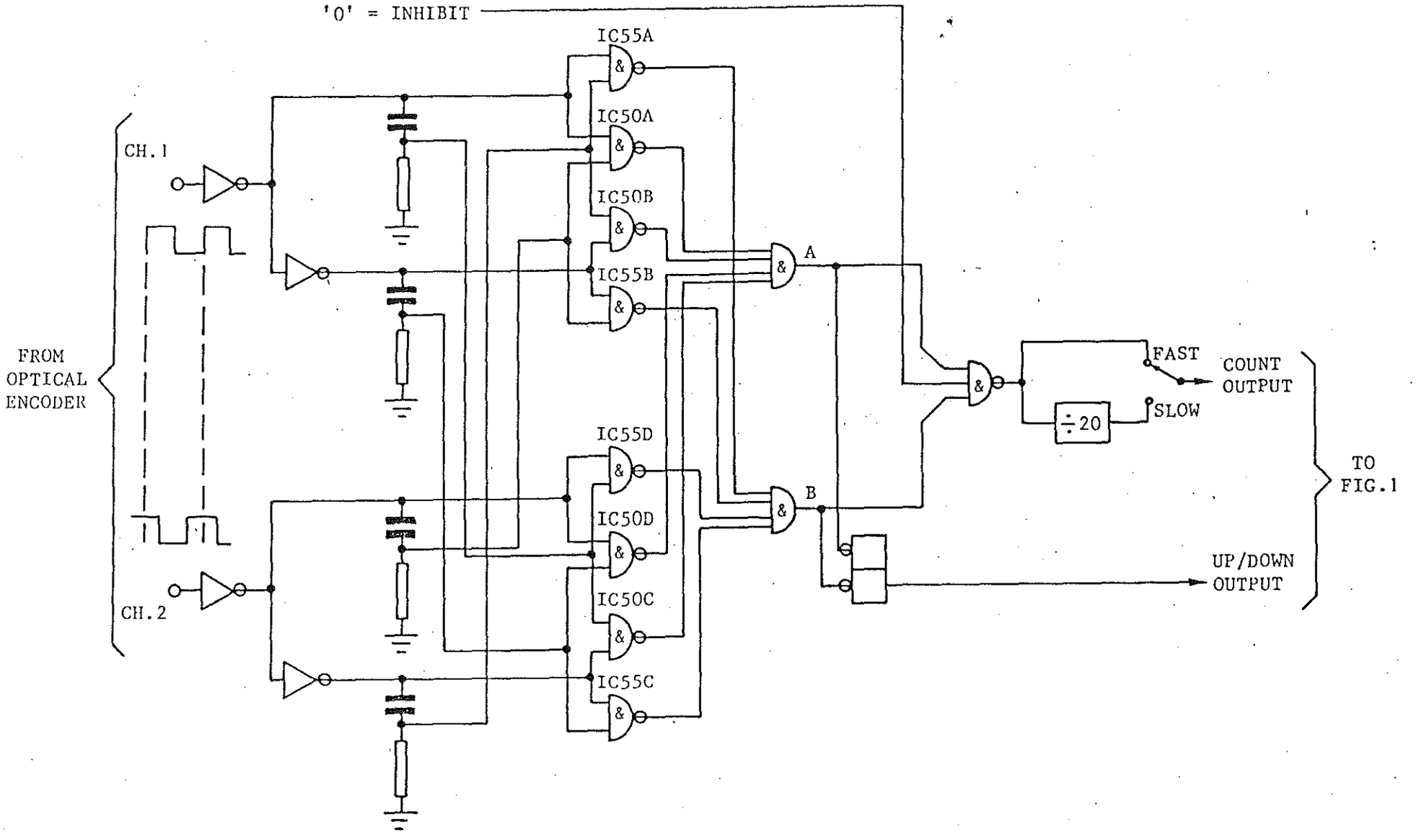


FIG (e) BASIC MANUAL TUNING LOGIC

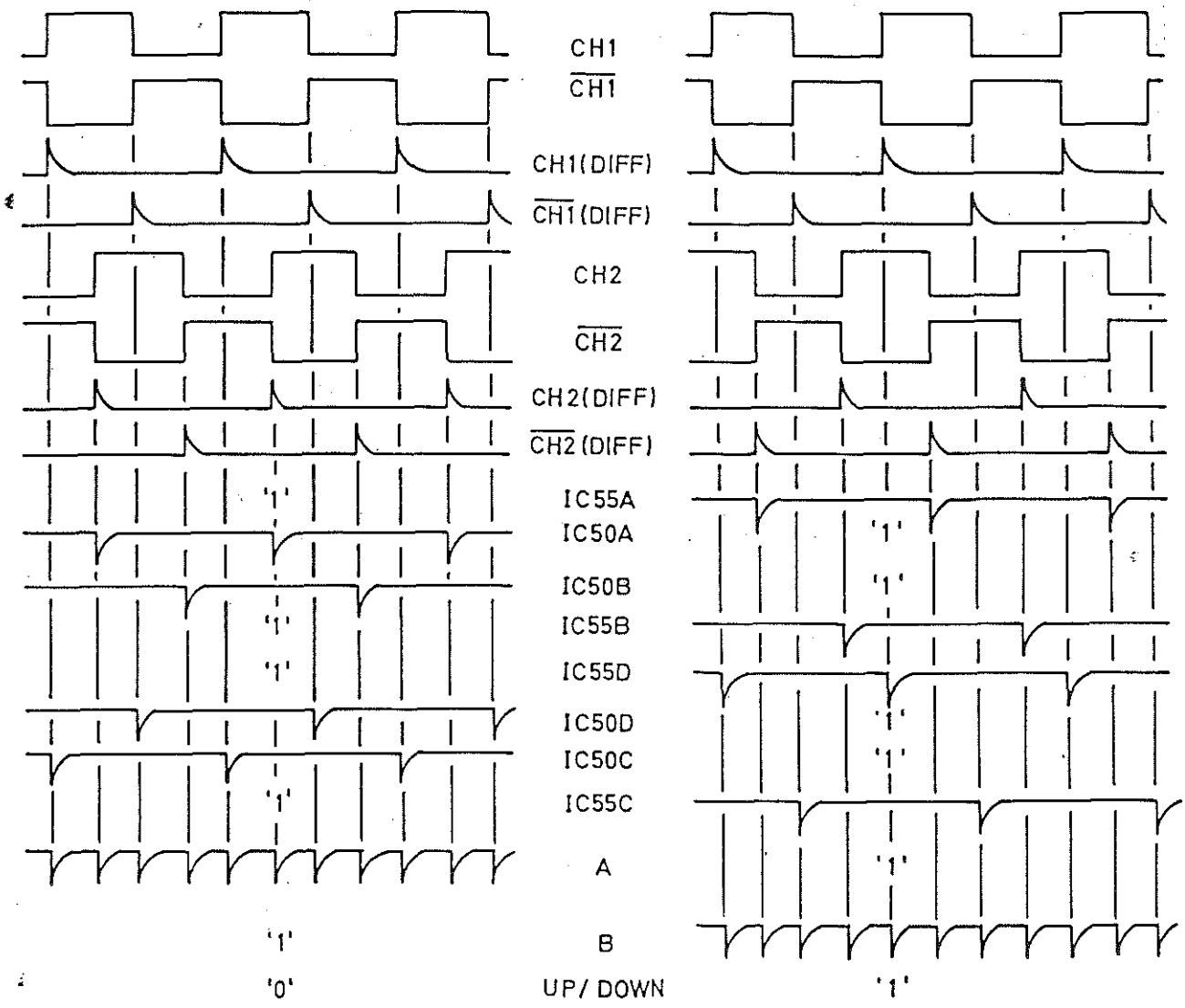


FIG (f) MANUAL TUNING CIRCUIT ACTION

tuning knob is rotated. The circuits controlled by the up-down counter outputs will react accordingly.

4.5 Filter Switching - Functional Description

4.5.1 Module 1 contains nine bandpass filters switched by PIN diodes. At all times the appropriate filter must be connected for the frequency in use. The control circuits are contained in Module 10, and consists of gating circuits which recognise particular output combinations from the up-down counters (Figure 1). A logic '1' output is produced by a gating circuit when the frequency to which the receiver is tuned falls within its 'recognition' band, as shown below:

0	to 1.39999MHz
1.4	to 1.99999MHz
2.0	to 2.99999MHz
3.0	to 3.99999MHz
4.0	to 5.99999MHz
6.0	to 8.99999MHz
9.0	to 13.99999MHz
14.0	to 20.99999MHz
21.0	to 29.99999MHz

4.6 Filter Switching - Circuit Description

4.6.1 Module 1 contains nine filters switched by PIN diodes. At all times the correct filter for the frequency in use must be connected in circuit. This switching is carried out by the outputs from a number of gating circuits which sense the outputs from the up-down counter. For physical economy of integrated circuits, a somewhat complex network of gates is used: the devices concerned are IC51, 52, 53, 54, 57, 58, 60 and 61. Nine separate circuits exist, one to control each filter in Module 1, and these nine circuits are shown, together with basic logic diagrams and truth tables in Figure (g) to (q).

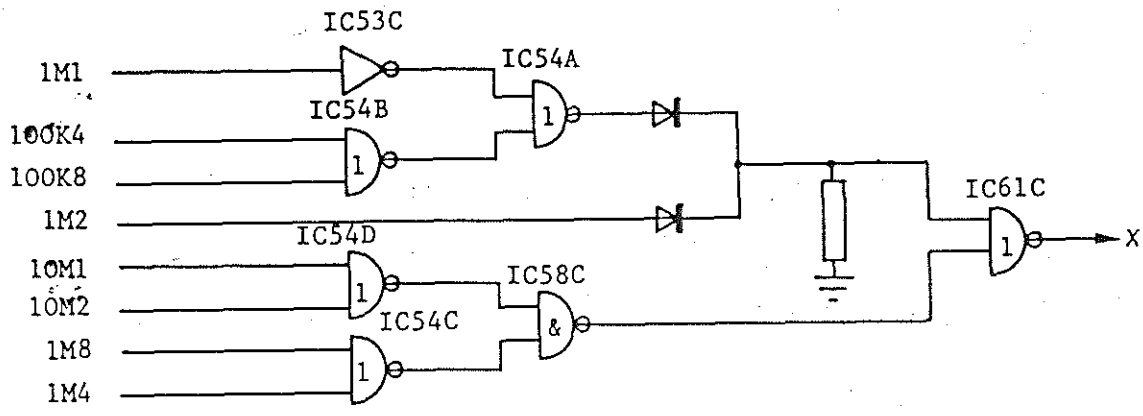
4.6.2 These outputs from the up-down counters are defined functionally in these diagrams, which correspond with their lead-titling on logic-board edge-pins 53 to 78. The titling corresponds with BCD coding of frequency in Hz, e.g. 1M0 - 1M1 - 1M2 - 1M3 are the four BCD lines which define the 'MHz' digit of the frequency value.

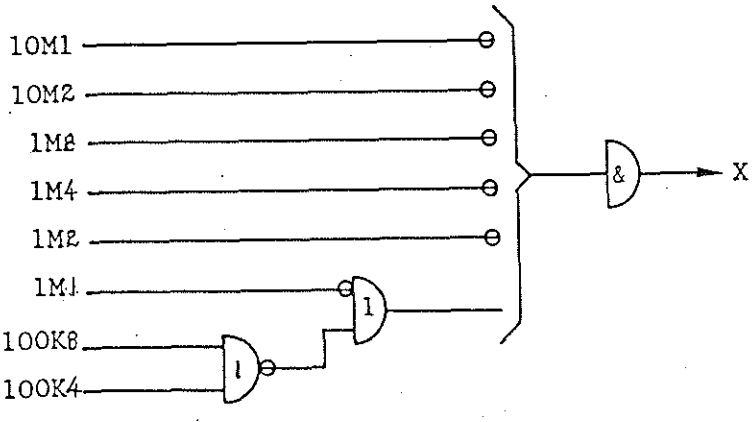
5. MODE AND BANDWIDTH CONTROL - DESCRIPTION

5.1 Mode and Bandwidth Control - Functional Description

5.1.1 The mode and Bandwidth Control circuit is a straightforward extension of the basic circuit shown in Figure (b). Two groups of press-buttons are employed, one for mode (F, CW, LSB, USB, ISB, AM, XTAL) and one for bandwidth (8, 6, 1.2, 0.3, 0.1). Each group is gated into three bistables. The two groups of inputs can be produced either by the front-panel buttons or from the memory.

5.1.2 Three AND functions interconnect the two groups. Because of their presence, the use of the F, CW, or AM mode buttons automatically sets up a particular bandwidth. However, this does not prevent subsequent selection of a different bandwidth. For example, if AM is operated, the 6kHz bandwidth is automatically selected. However, if the AM and 1.2 buttons are pressed in sequence the receiver will operate in AM mode on 1.2kHz bandwidth.

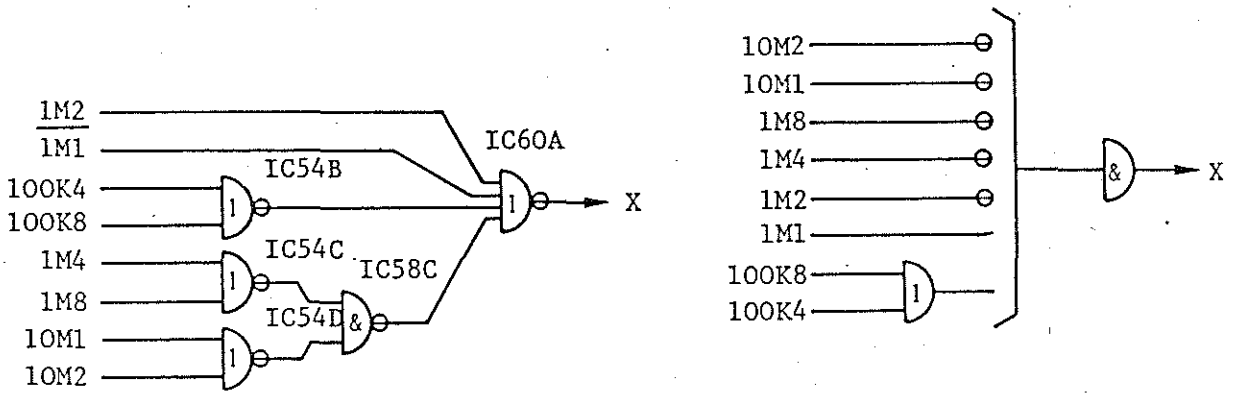




X = 1 FOR :-

10M2	10M1	1M1	1M2	1M4	1M8	100K4	100K8
0	0	0	0	0	0	1	0
0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0
0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0

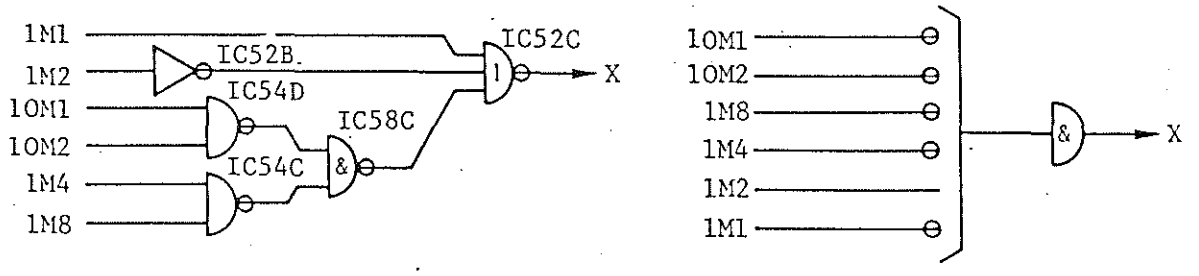
FIG (g) 0-1.39999MHz FILTER GATING



X = 1 FOR :-

10M1	10M2	1M1	1M2	1M4	1M8	100K4	100K8
0	0	1	0	0	0	1	0
0	0	1	0	0	0	0	1

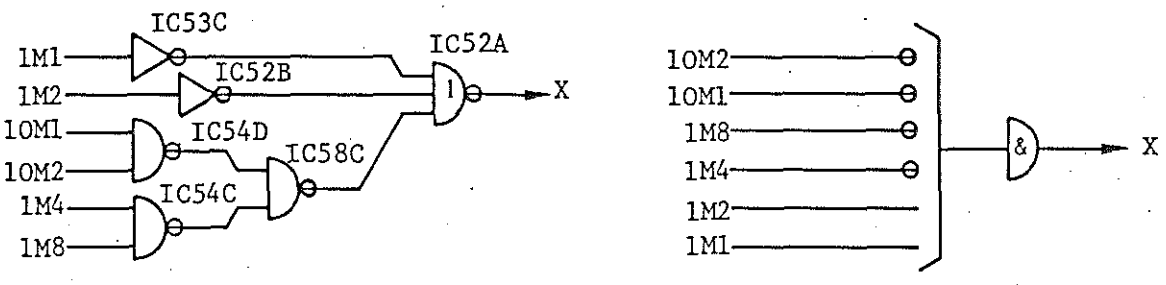
FIG (h) 1.4-1.99999MHz FILTER GATING



X = 1 FOR :-

10M2	10M1	1M1	1M2	1M4	1M8
0	0	0	1	0	0

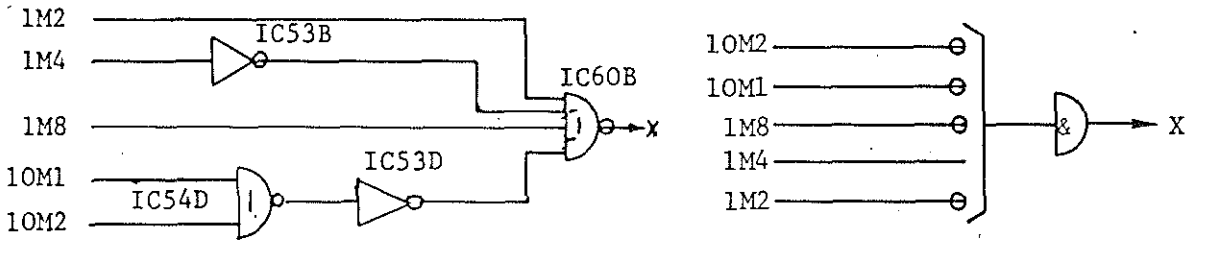
FIG (j) 2-2.99999MHz FILTER GATING



X = 1 FOR :-

10M1	10M2	1M1	1M2	1M4	1M8
0	0	1	1	0	0

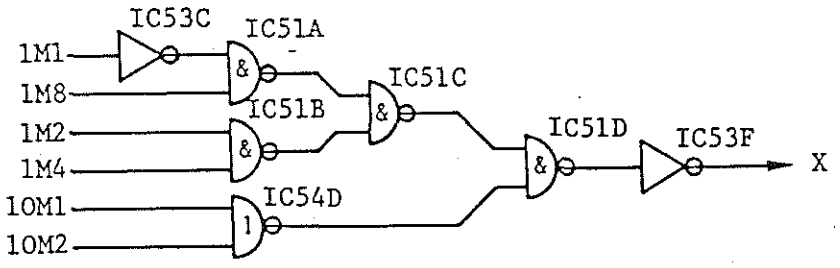
FIG (k) 3-3.99999MHz FILTER GATING

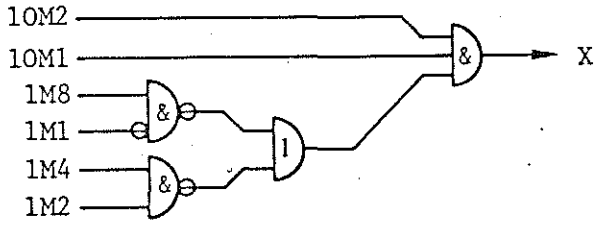


X = 1 FOR :-

10M1	10M2	1M2	1M4	1M8
0	0	0	1	0

FIG (1) 4-5.99999MHz FILTER GATING

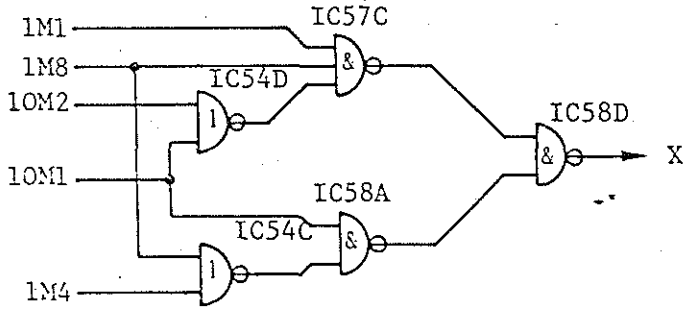


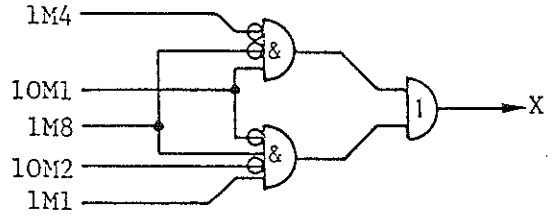


X = 1 FOR :-

1OM2	1OM1	1M1	1M2	1M4	1M8
0	0	0	1	1	0
0	0	0	0	0	1
0	0	1	1	1	0

FIG (m) 6-8.99999MHz FILTER GATING



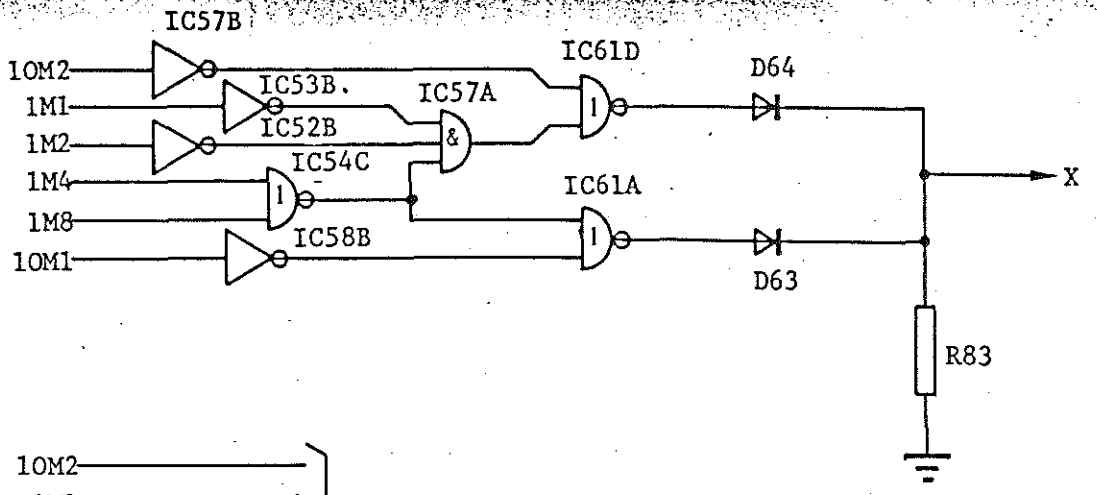


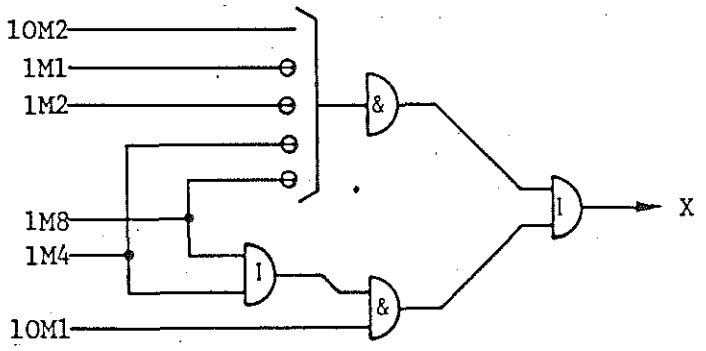
X = 1 FOR :-

1OM1	1OM2	1M1	1M4	1M8
0	0	1	X	1
1	X	X	0	0

X = 'DONT CARE'

FIG (n) 9-13.99999MHz FILTER GATING



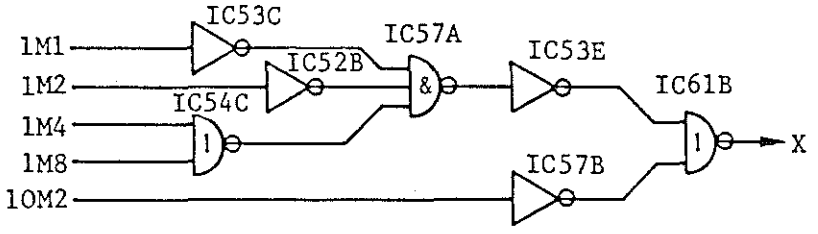


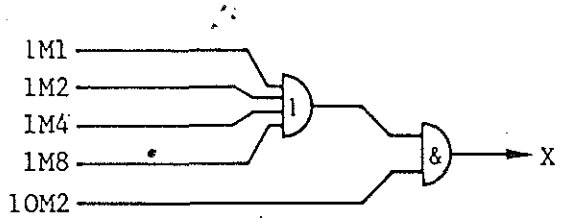
X = 1 FOR :-

10M2	10M1	1M8	1M4	1M2	1M1
X	1	X	1	X	X
X	1	1	X	X	X
1	X	0	0	0	0

X = 'DONT CARE'

FIG (p) 14-20.99999MHz FILTER GATING





X = 1 FOR :-

10M2	1M1	1M2	1M4	1M8
1	1	X	X	X
1	X	1	X	X
1	X	X	1	X
1	X	X	X	1

X = 'DONT CARE'

FIG (q) 21-29.99999MHz FILTER GATING

5.1.3 The circuit can be seen in Figure (r), which includes a truth table of outputs. The two groups of bistables each produce a 3-bit binary number output which is decoded by the controlled circuits.

5.2 Mode and Bandwidth Control - Circuit Description

5.2.1 The action of the Mode and Bandwidth control code generating circuits can be fully understood from the functional description. The six bistables shown in the functional diagram (Figure (r)) are identified there as A to F. The corresponding integrated circuits are:

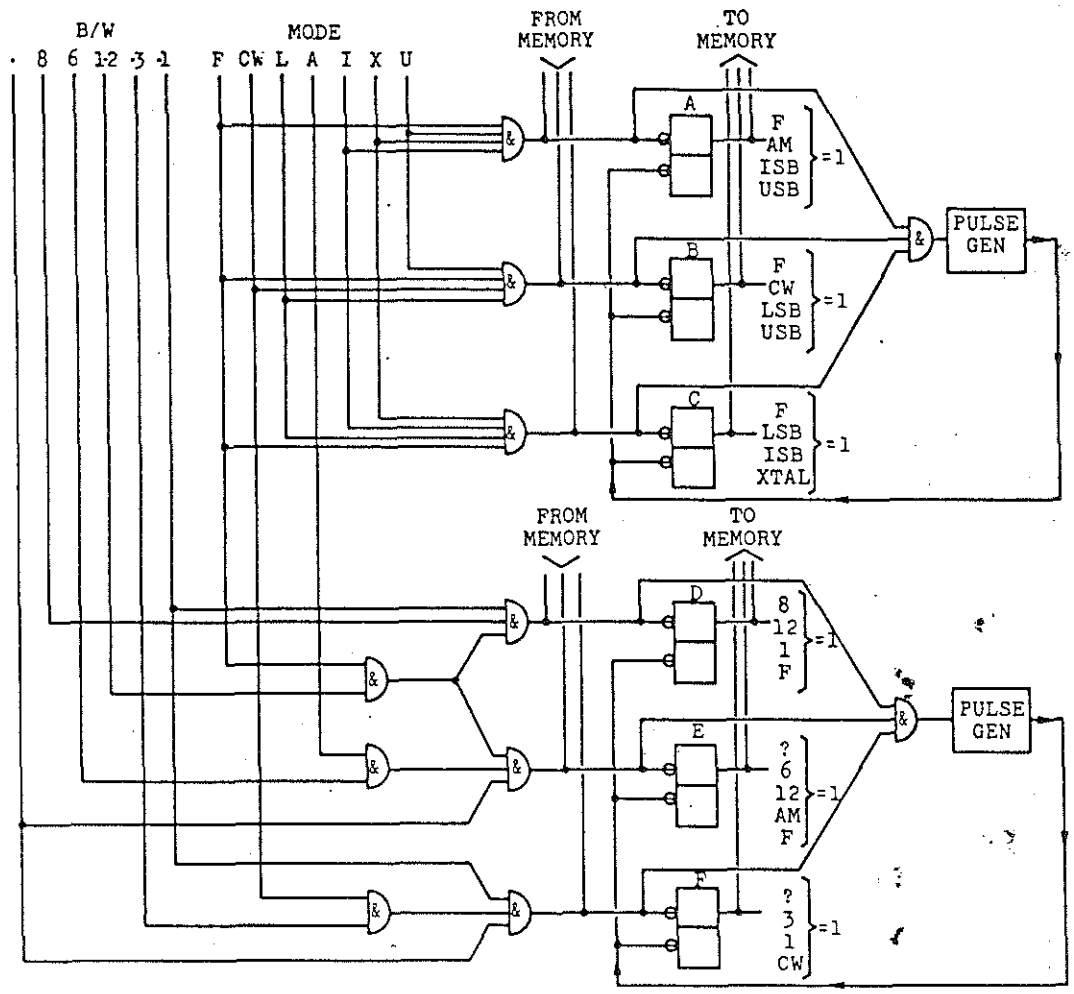
A : IC46C - IC46D	D : IC47D - IC47A
B : IC47B - IC47C	E : IC48D - IC48C
C : IC46B - IC46A	F : IC48A - IC48B

The resetting pulse generator from the A-B-C (mode) group of bistables is formed by IC38A, IC38C, and IC38D: that for the D-E-F (bandwidth) group of bistables is formed by IC59A, IC59C, and IC59D.

5.2.2 The functional diagram shown in Fig.(r) omits one input to the basic circuit; this input is an inhibit on bistables D, E, and F, which comes into operation when USB, LSB, or ISB mode is selected. Referring to Fig.4, it can be seen that the USB, LSB, and ISB mode LED driver outputs from IC55 are connected to the reset line of bistables IC74D, 74A; IC48D, 48C; IC48A, 48B (bistables D, E, and F in Fig.(r)) via an AND gate made up of D56, D57, D58, and R95. Selection of USB, LSB, or ISB mode sets the appropriate output from IC55 to '0'; this '0' level, via the AND gate, is applied as a permanent inhibit to the three bandwidth selection bistables for so long as the mode remains selected. Note that, if during USB, LSB, or ISB operation, a bandwidth button is pressed it will select the appropriate circuit but will only do so while the button is pressed; this is not a valid mode of operation and is only mentioned to avoid this effect being mistaken for a fault condition.

5.2.3 Each of the two groups of bistables supplies the inputs to a BCD-decimal decoder (IC49 and IC50). The output lines from each decoder are normally at '0'. One line level rises to '1' according to the inputs applied, as listed below. All inputs at '0' produces all outputs at '0'.

NUMERICAL VALUE	INPUT PINS				OUTPUT PINS						
	10	13	12	11	14	2	15	1	6	7	4
1	1	0	0	0	1	0	0	0	0	0	0
2	0	1	0	0	0	1	0	0	0	0	0
3	1	1	0	0	0	0	1	0	0	0	0
4	0	0	1	0	0	0	0	1	0	0	0
5	1	0	1	0	0	0	0	0	1	0	0
6	0	1	1	0	0	0	0	0	0	1	0
7	1	1	1	0	0	0	0	0	0	0	1



NOTE. LOGIC UP TO BISTABLE INPUTS IS '0' ACTIVE. ALL NON-OPERATED INPUT LINES ARE EFFECTIVELY PULLED UP TO '1'.

	BISTABLE			OUTPUTS		
	A	B	C	D	E	F
F	1	1	1	1	1	0
CW	0	1	0	0	0	1
LSB	0	1	1	X	X	X
AM	1	0	0	0	1	0
ISB	1	0	1	X	X	X
XTAL	0	0	1	X	X	X
USB	1	1	0	X	X	X
.	X	X	X	0	1	1
8	X	X	X	1	0	0
6	X	X	X	0	1	0
1.2	X	X	X	1	1	0
0.3	X	X	X	0	0	1
0.1	X	X	X	1	0	1

X = 'DONT CARE'

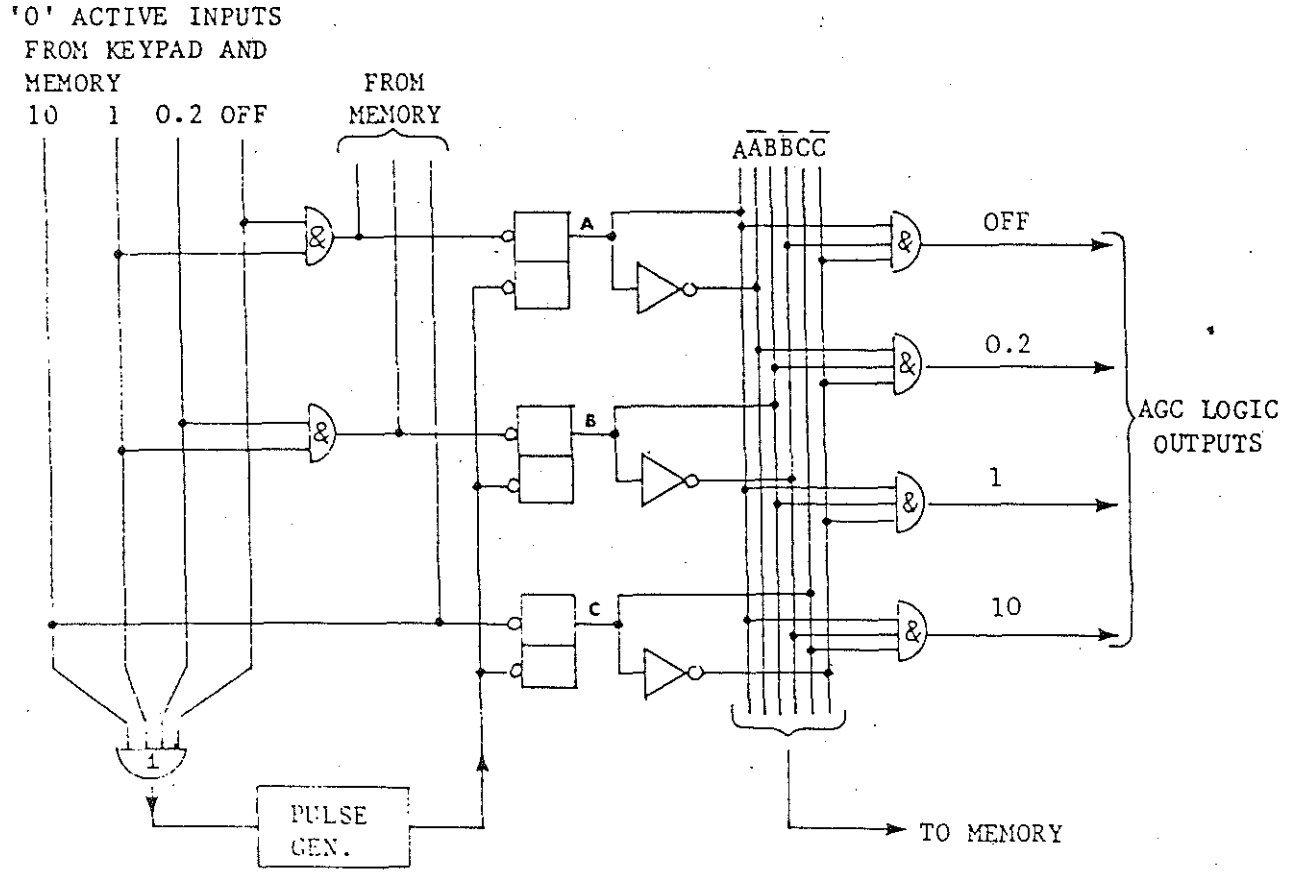
FIG.(r) BASIC MODE AND BANDWIDTH CONTROL LOGIC

5.2.4 The outputs from the decoders provide the controlling outputs to the mode and the bandwidth circuits, and are also fed via LED drivers IC55, TR3, and IC56 to operate front-panel LED indicators. The mode and bandwidth outputs to the memory circuits are taken in parallel with the inputs to the decoders.

6. AGC CONTROL - DESCRIPTION

6.1 AGC Control - Functional Description (Figure (s))

The AGC control circuit is a straightforward extension of the basic circuit shown in Figure (b). The BCD/Decimal decoder shown in Figure (b) is replaced by four AND functions.



A	B	C	OFF	0.2	1	10
1	0	0	1	0	0	0
0	1	0	0	1	0	0
1	1	0	0	0	1	0
0	0	1	0	0	0	1

FIG (s) BASIC AGC CONTROL LOGIC

6.2 AGC Control - Circuit Description

As in the Mode and Bandwidth control circuits, the AGC control circuit is a simple set of push-button setting bistables, as shown in Figure (s). The outputs of the bistables are decoded by a number of gates. The three bistables A, B, and C shown in the functional diagram (Figure (s)) are formed by IC35C-IC35D, IC42C-IC42D, and IC35B-IC35A. Decoding is carried out by IC36, IC41B, IC41C, IC41D, and IC37C. The decoded outputs are fed

to the controlled circuits and, via LED drivers IC43, to front-panel LED indicators.

7. LOCAL/REMOTE CONTROL - DESCRIPTION

7.1 Local/Remote Control - Functional Description

As in the Mode and AGC control circuits the Local/Remote circuit uses a pair of '0' active outputs from front-panel buttons to control a bistable. Q='1' for local, and '0' for remote. Two complementary outputs, LOCAL + and LOCAL -, are produced. The state of the bistable is indicated by two front-panel LEDs. When in remote, the '0' level from the Q output of the bistable is used to inhibit the output of the manual tuning circuits.

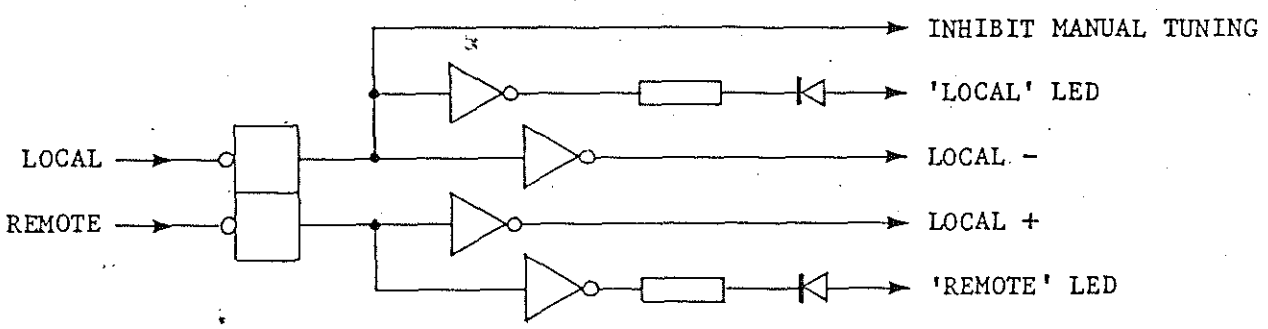


FIG (t) BASIC LOCAL/REMOTE CONTROL

7.2 Local/Remote Control - Circuit Description

The bistable is formed by IC33D and IC33C. Inverters TR2 and IC32C provide the complementary LOCAL + and LOCAL - outputs. Inverters IC32B and IC32F provide the indicator LED drivers. The inhibit control to the manual tuning is taken via D9 from the bistable Q output, and applied to IC34B.

8. OPERATE/STANDBY AND MEMORY CONTROLS

8.1 The front-panel OPERATE/STANDBY power switch and the three memory control buttons, SELECT, STORE, and RECALL, operate via a 'contact de-bounce' circuit situated in the small printed-circuit panel behind the internal loudspeaker. IC1 contains four separate 'de-bounce' circuits, one for each control. All four channels are controlled by a clock oscillator in IC1: frequency is set to 225Hz by C4. When a control is operated, the appropriate output of IC1 changes level from '1' to '0' four clock periods after the last 'bounce'. It remains at '0' until the next control operation, when it returns to '1' four clock periods after the last 'bounce'. The output levels from IC1 are inverted in IC2.

8.2 The memory channel select circuit is controlled by the front-panel SELECT button. Short-period operation of the button causes a single memory channel change, while longer period operation causes channel changes to occur at intervals of approximately one second so long as the button is held depressed. The action is cyclic, e.g. to select channel 10 from channel 11 it is necessary to go via channels 15 and 0. The selected channel is displayed on two 7-segment LED indicators.

8.2.1 Depressing the front-panel INCREMENT button S1 activates an oscillator consisting of IC1D, IC1C and associated components. The oscillator pro-

vides clockpulses to a 4-bit binary counter IC2B, which provides a 0 to 15 output (Q0 to Q3). The 0 to 15 output from IC2B is applied to a gating circuit IC4, which is controlled by operation of the front-panel SELECT button via a 'contact de-bounce' circuit IC1 (Fig.11). The gated output is used to address the memory.

8.2.2 The 0 to 15 output from IC2B is also applied to a '10 or over' detector circuit formed by IC5, IC1A and IC1B. An OR function is formed by IC5D, IC5E, and IC1B, and is fed by IC2B Q1 and Q2 outputs. The OR function output (IC1B pin 4) is applied to one input of an AND function formed by IC1A and all four elements of IC5; this produces a function with two output lines. The second input to the AND function is supplied by the Q3 output from IC2B. If the binary number represented by the Q outputs from IC2B is 10 or greater, then the two outputs from IC5 are '1', i.e. the circuit forms a 'ten or over' detector. If the two outputs from IC5 are '1' then a 1 will be displayed on the 'tens' display of the front-panel.

8.2.3 Two parallel outputs from the '10 or over' detector (IC5A and IC5F) are applied to a 4-bit full adder IC3, together with the 0 to 15 output from IC2B. The A input to IC3 can be anything from 0 to 15; the B0 and B3 inputs are both '0'. The B1 and B2 inputs are '0' when the output from IC2B is binary 0 to 9 and '1' when the binary output is 10 to 15. i.e. B inputs are either 0000 or 0110 (0 or 6). The inputs and output of the 4-bit full adder are shown in Table 1.

TABLE 1 : A AND B INPUTS TO IC3

A INPUTS TO IC3	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
B INPUTS TO IC3	0	0	0	0	0	0	0	0	0	0	6	6	6	6	6	6
IC3 OUTPUT	0	1	2	3	4	5	6	7	8	9	16	17	18	19	20	21

8.2.4 The two four-bit numbers applied to IC3 are added to produce a single 5-bit number, the C0 output being the 5th bit. As can be seen from Table 1, the output from IC3 for 10 and greater is 16 to 21. The carry function of IC3 is the M.S.B. For an IC3 output of 16, the individual outputs as shown below:

S0	S1	S2	S3	C0
0	0	0	0	1

The C0 output is not fed to the units display and so the display will show 0, to indicate that channel 10 has been selected.

Similarly, if the output of IC3 is 18, the individual outputs are as follows:

S0	S1	S2	S3	C0
0	1	0	0	1

The units display will not indicate 2 to show that channel 12 has been selected.

The outputs to display IC3 (units) and IC2 (tens) are shown in Table 2.

TABLE 2 : INPUTS TO UNITS AND TENS DISPLAY

IC2B OUTPUT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
UNITS DISPLAY IC3	0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5
TENS DISPLAY IC2	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

8.2.5 The output from the 4-bit full adder IC3, is applied via 7-segment decoder IC1 to the units display on the front-panel.

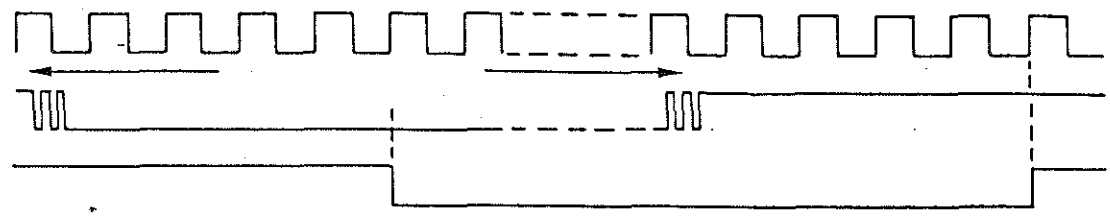


FIG (u) DE-BOUNCE CIRCUIT ACTION

9. METER CIRCUIT

The monitor meter circuit consists of a 100uA FSD micro-ammeter and a twelve-way rotary switch via which ten points in the receiver can be monitored. All monitored inputs are fed to the switch in a form suitable for direct application to the meter.

10. RF-IF GAIN, AUDIO GAIN, and VAR, BFO CONTROLS

These controls are standard potentiometers producing variable d.c. outputs. The circuits are self-explanatory.

11. ISB AUDIO, INHIBIT-OPERATE, and SPEAKER-ON-OFF CONTROLS

These controls are standard miniature rocker switches. The circuits are self-explanatory.

12. MODULE 10A

Module 10A forms the front-panel of a PR2251 receiver. It does not provide any control of tuning, mode, bandwidth or agc as these functions are slaved to the associated master PR2250 or PR2252 receiver. Consequently no logic circuit panel is fitted. The controls and items which are fitted on the front-panel of Module 10A are also identical with those of Module 10; these are:

(1) AF GAIN

(2) Internal loudspeaker

(3) SPEAKER ON-OFF switch

(4) LSB-ISB AUDIO switch

(5) Two headphone jack sockets

(6) Monitor meter and associated selector switch

13. MODULE 10B

13.1 Module 10B forms the front-panel of a PR2252 receiver. It does not provide local manual control facilities for tuning, mode, bandwidth or agc. Functionally, it only differs from Module 10 in respect of the omission of these controls, i.e. control of the receiver can only be exercised via the memory circuits of Module 11 or Module 12.

13.2 The logic circuitry of Module 10B is identical with that of Module 10 and therefore needs no separate description. It carries the same controls and items on the front-panel as those on Module 10A.

14. TEST DATA

14.1 The test procedure for Module 10 is covered in the overall test procedures given in Chapter 2, Section 5 of this manual. Therefore no additional test data is required.

14.2 The test procedure consists of checking the operation of the front panel controls and the associated LED indicators of Module 10. The LED indicators are driven via lamp drivers from the outputs of the individual control circuits, therefore an illuminated LED indicator may be considered as a final test of the control circuit and switch.

14.3 As Module 11 is employed when carrying out checks on the memory controls on the front-panel of Module 10, it is essential to ensure that there are no faults on Module 11, as this will give a false indication of the condition of Module 10.

15. COMPONENT LISTS

Main Assembly (Module 10 - 630/1/32990/001)
Panel Electronic Circuit (419/1/17992)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Panel Printed Circuit	Plessey	419/1/18000
-	Socket	Cambion 450-3704-1-03	508/4/22095
-	Socket Low Profile	Texas C931402 14-pin DIL	508/4/22096/002
-	Socket Low Profile	Texas C931602 16-pin DIL	508/4/22096/003
C1,8,11-14	Capacitor 100pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/011
C3	Capacitor 820pF ± 2.5% 30V	Suflex HSC 30	437/4/30011/030
C7,32	Capacitor 1000pF ± 5% 400V	Siemens B32560	435/4/90317/023
C6,17,19-21,25,29	Capacitor 0.01uF ± 5% 400V	Siemens B32560	435/4/90317/029
C40	Capacitor 0.1uF ± 5% 100V	Siemens B32560 100V	435/4/90317/014
C5	Capacitor 0.22uF ± 5% 100V	Siemens B32560 100V	435/4/90317/017
C2,31	Capacitor 0.1uF ± 20% 35V	ITT Tag	402/4/57057/001
C4,10,33	Capacitor 1.0uF ± 20% 35V	ITT Tag	402/4/57057/003
C26,34-38	Capacitor 2.2uF ± 20% 16V	ITT Tag	402/4/57057/007
IC22,38,44,54,59,61	Integrated Circuit	Motorola MC14001CP	445/4/02383/001
IC60	Integrated Circuit	Motorola MC14002CP	445/4/02383/002
IC15,24,25,33,34,35,39,42,45-48,51,58,63-66	Integrated Circuit	Motorola MC14011CP	445/4/02383/011
IC30	Integrated Circuit	Motorola MC14012CP	445/4/02283/012
IC26-29	Integrated Circuit	Motorola MC14015CP	445/4/02383/015
IC57	Integrated Circuit	Motorola MC14023CP	445/4/02383/023
IC36,37,52	Integrated Circuit	Motorola MC14025CP	445/4/02383/025
IC49,50	Integrated Circuit	Motorola MC14028CP	445/4/02383/028
IC32,43,55,56	Integrated Circuit	Motorola MC14049CP	445/4/02383/049
IC16,41,53	Integrated Circuit	Motorola MC14069CP	445/4/02383/069
IC40	Integrated Circuit	Motorola MC14093CP	445/4/02383/093
IC8-14	Integrated Circuit	Motorola MC14510CP	445/4/02383/510
IC1-7	Integrated Circuit	Motorola MC14511CP	445/4/02383/511
IC23	Integrated Circuit	Motorola MC14518CP	445/4/02383/518
IC31,62	Integrated Circuit	Motorola MC14528CP	445/4/02383/528
IC17-21	Integrated Circuit	National MM80C95	445/4/03053/005
R9,57	Resistor 100R ± 2% 0.25W	Electrosil TR4	403/4/05522/100
R101,102,108-111,113-116,160-172	Resistor 470R ± 2% 0.25W	Electrosil TR4	403/4/05522/470
R22-56,58-71,124	Resistor 1k ± 2% 0.25W	Electrosil TR4	403/4/05523/100
R122	Resistor 2.2k ± 2% 0.25W	Electrosil TR4	403/4/05523/220

Panel Electronic Circuit (Cont'd)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
R6,96-98	Resistor 10k ± 2% 0.25W	Electrosil TR4	403/4/05524/100
R7	Resistor 15k ± 2% 0.25W	Electrosil TR4	403/4/05524/150
R18,121,173	Resistor 22k ± 2% 0.25W	Electrosil TR4	403/4/05524/220
R89,128,129	Resistor 47k ± 2% 0.25W	Electrosil TR4	403/4/05524/470
R74-77	Resistor 56k ± 2% 0.25W	Electrosil TR4	403/4/05524/560
R1-5,8,13-17,19,72,73,78-88,90-95,100,103-107,117,118-120,123,125,127,130-155	Resistor 100k ± 2% 0.25W	Electrosil TR4	403/4/05525/100
R11,12,20,99	Resistor 1M ± 5%	Allen Bradley Type CB	403/4/04361/003
R10	Resistor 4.7M ± 5%	Allen Bradley Type CB	403/4/04361/470
D1-41,43-60,63-85,87-101	Diode	Texas 1N4148	415/4/05720
TR1,2,3	Transistor	Mullard BC109	417/4/01776
-	Sleeve Ident Yellow marked K	Hellerman	915/4/04042/030
-	Sleeve Ident Yellow marked L	Hellerman	915/4/04042/031
-	Sleeve Ident Yellow marked M	Hellerman	915/4/04042/032
-	Sleeve Ident Yellow marked N	Hellerman	915/4/04042/033
-	Sleeve Ident Yellow marked P	Hellerman	915/4/04042/035
-	Sleeve Ident Yellow marked Q	Hellerman	915/4/04042/036
-	Sleeve Ident Yellow marked R	Hellerman	915/4/04042/037
-	Sleeve Ident Yellow marked S	Hellerman	915/4/04042/038
-	Sleeve Ident Yellow marked T	Hellerman	915/4/04042/039
-	Sleeve Ident Yellow marked U	Hellerman	915/4/04042/040
-	Sleeve Ident Yellow marked V	Hellerman	915/4/04042/041
-	Sleeve Ident Yellow marked W	Hellerman	915/4/04042/042
-	Sleeve Ident Yellow marked X	Hellerman	915/4/04042/043
-	Sleeve Ident Yellow marked Y	Hellerman	915/4/04042/044
-	Sleeve Ident Yellow marked Z	Hellerman	915/4/04042/045

Flexi-Circuit Assembly Channel Select (419/1/18112)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Flexi-Circuit	Brybond	419/1/18113
D1	Diode, LED	Texas TIL209 Red	520/9/97665
-	Flexi-Circuit Assembly	Brybond	419/9/18114

Front Panel Assembly (630/1/32980)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Filter	Plessey	630/2/32970
-	Baffle Plate	Plessey	630/2/32972
-	Baffle	Plessey	630/2/32974
-	Bracket	Plessey	630/2/32978
-	Hinged Front Panel	Plessey	630/9/33039
-	Loudspeaker, Permanent Magnet	Elac 235T25, Electro Acoustic Ind.	409/4/11534
-	Switch Lever Rocker	Arrow 1100B Black	408/4/51496/001
-	Jack Telephone	Rendar R326-400-05	508/4/22103/001
-	Spacer Threaded	Harwin R6074 M3X10LC	999/9/32544/004
-	Plessey Presentation Badge	Plessey	980/4/08030/002
D25	Semi-conductor Device LED Yellow Diffused Lens	Hewlett Packard 5082-4550	520/4/97666
D24	Semi-conductor Device LED Green Diffused Lens	Hewlett Packard 5082-4950	520/4/97667
-	Flexi-Circuit Assembly	Brybond No 14	419/1/18096
-	Flexi-Circuit Assembly	Brybond No 13	419/1/18100
-	Flexi-Circuit Assembly	Brybond No 12	419/1/18105
-	Spacer	Plessey	630/2/32929
-	Screw Special	Plessey	630/2/32994
-	Incremental Encoder	Plessey	630/9/32933
-	Knob	Evans No 4325 D/4326 Modified Bore	630/9/32592
-	Knob	Evans No 4371 D/4372 Modified Bore	630/9/32951
-	Knob	Evans No 4371D	630/9/32950
-	Skirt	Evans No 4372 Mod	630/9/32949

Keyboard Assembly (630/1/32927)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Board Frame Assembly	Plessey	630/1/32939
-	Keyboard Frame Assembly	Plessey	630/1/32925
-	Variable B.F.O. Control Assembly	Plessey	630/1/32930
-	Memory Display and Switching Assembly	Plessey	630/1/35320
-	Switch, Rocker SPDT	Plessey	408/1/35511/110

Keyboard Assembly (continued)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Flexi-Circuit Assembly No 4	Brybond No 4	419/1/18071
-	Flexi-Circuit Assembly No 2	Brybond No 2	419/1/18079
-	Flexi-Circuit Assembly No 5	Brybond No 5	419/1/18083
-	Flexi-Circuit Assembly No 3	Brybond No 3	419/1/18088
-	Flexi-Circuit Assembly	Brybond No 1	419/1/18096
-	Spacer Threaded	Plessey	630/2/32928
-	Fixing Block	Plessey	630/2/32932
-	Spacer	Plessey	630/2/33019/001
-	Spacer Plate	Plessey	630/2/33051
-	Keycap Black marked 0	Plessey	630/9/32940/001
-	Keycap Black marked 1	Plessey	630/9/32940/002
-	Keycap Black marked 2	Plessey	630/9/32940/003
-	Keycap Black marked 3	Plessey	630/9/32940/004
-	Keycap Black marked 4	Plessey	630/9/32940/005
-	Keycap Black marked 5	Plessey	630/9/32940/006
-	Keycap Black marked 6	Plessey	630/9/32940/007
-	Keycap Black marked 7	Plessey	630/9/32940/008
-	Keycap Black marked 8	Plessey	630/9/32940/009
-	Keycap Black marked 9	Plessey	630/9/32940/010
-	Keycap Black marked .	Plessey	630/9/32940/011
-	Keycap Black marked Enter	Plessey	630/9/32940/012
-	Keycap Black marked Clear	Plessey	630/9/32940/013
-	Keycap Grey marked Sel	Plessey	630/9/32940/077
-	Keycap Grey marked INCR	Plessey	630/9/32940/076
-	Keycap Grey marked RCL	Plessey	630/9/32940/075
-	Keycap Grey marked Local	Plessey	630/9/32940/017
-	Keycap Red marked Remote	Plessey	630/9/32940/018
-	Keycap Grey marked Fast	Plessey	630/9/32940/019
-	Keycap Grey marked Slow	Plessey	630/9/32940/020
-	Keycap Grey marked Off	Plessey	630/9/32940/021
-	Keycap Grey marked Short	Plessey	630/9/32940/022
-	Keycap Grey marked Med	Plessey	630/9/32940/023
-	Keycap Grey marked Long	Plessey	630/9/32940/024
-	Keycap Grey marked Xtal	Plessey	630/9/32940/025
-	Keycap Grey marked Recom. Carr.	Plessey	630/9/32940/026
-	Keycap L. Grey marked 0.1	Plessey	630/9/32940/027
-	Keycap L. Grey marked 1.2	Plessey	630/9/32940/028
-	Keycap L. Grey marked 6	Plessey	630/9/32940/029
-	Keycap L. Grey marked 0.3	Plessey	630/9/32940/030
-	Keycap L. Grey marked 8	Plessey	630/9/32940/031
-	Keycap L. Grey marked AM	Plessey	630/9/32940/032
-	Keycap L. Grey marked CW	Plessey	630/9/32940/033
-	Keycap L. Grey marked USB	Plessey	630/9/32940/034
-	Keycap L. Grey marked LSB	Plessey	630/9/32940/035
-	Keycap L. Grey marked ISB	Plessey	630/9/32940/036
-	Keycap L. Grey marked F	Plessey	630/9/32940/037
-	Keycap L. Grey marked Store	Plessey	630/9/32940/045
-	Microammeter 100uA FSD	Wilbac Model 921mm Special Scale	682/9/01718

Keyboard Assembly (continued)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Switch Rotary	Lorlin Type Ck 12 Pin	408/9/51497
-	Switch Push	Cherry M61-0110	408/4/51494/001
-	Switch Toggle	Plessey	408/1/35511/110
-	Resistor Variable 1k	Plessey Type MH1 1k	404/9/08059/001
-	Resistor Variable 4.7k	Plessey Type MH1 4.7k	404/9/08059/002

Circuit Assembly, Auxiliary Panel (419/1/18096)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
C4	Capacitor 10nF ± 5% 400V	Siemens B32560-B3103J	435/4/90317/029
C1,2,3	Capacitor electrolytic 10uF ± 20% 16V	ITT TAG	402/4/57057/008
IC1	Integrated Circuit	Motorola MC14490FP	445/4/02383/490
IC2	Integrated Circuit	Motorola MC14049UBCP or RCA CD4049UBE	445/4/02383/049
R10	Resistor 100R ± 2% 0.25W	Electrosil TR4	403/4/05522/100
R5	Resistor 1.5k ± 2% 0.25W	Electrosil TR4	403/4/05523/150
R2	Resistor 3.9k ± 2% 0.25W	Electrosil TR4	403/4/05523/390
R7,8,9	Resistor 100k ± 2% 0.25W	Electrosil TR4	403/4/05525/100
D2,3,4,	Diode	Texas 1N4148	415/4/05720

Panel Frame Assembly (630/1/32929)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Frame Assembly	Plessey	630/1/33022
-	Panel Electronic Circuit	Plessey	419/1/17992
-	Spacer	Plessey	630/2/32739
-	Hinge Bar	Plessey	630/2/33028
-	Plastic Cee Section	Hellerman Type PS Beading	998/4/83105/001

Frame Assembly (630/1/33022)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Frame	Plessey	630/2/33021
-	Fastener, Spring Loaded	PEM PFC2-M3-40	991/4/11754/001
-	Nutsert M3 Brass zinc plated	Avdel 9528	999/9/32469/001

Variable BFO Control Assembly (630/1/32930)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Bracket Assembly	Plessey	630/1/33043
-	Ball Drive Unit	Jackson Bros. 4511/ DAF (Modified)	630/9/33046
-	Resistor Variable 4.7k	Plessey Type M.H1	404/9/08059/003

Bracket Assembly (630/1/33043)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Bracket	Plessey	630/2/33042
-	Pin	Plessey	630/2/33029

Bracket Assembly (630/1/33027)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Bracket	Plessey	630/2/33026
-	Press nut	Rosan M3	999/4/03261/005

Main Assembly (Module 10A, 630/1/32990/002)
Front Panel Assembly (630/1/32980/002)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Baffle Plate	Plessey	630/2/32972
-	Baffle	Plessey	630/2/32974
-	Hinged Front Panel	Plessey	630/9/32997
-	Loudspeaker Permanent Magnet	Elec 23ST25 Electro Acoustic Ind.	409/4/11534
-	Switch Lever Rocker	Arrow 1100B Black	408/4/51496/001
-	Jack Telephone	Rendar R3296-400-05	508/4/22103/001
-	Plessey Presentation Badge	Plessey	980/4/08030/002
-	Semi-Conductor Device LED Yellow Diffused Lens	Hewlett Packard 5082-4550 series	520/4/97666
-	Semi-Conductor Device LED Green Diffused Lens	Hewlett Packard 5082-4950 series	520/4/97667

Memory Display and Switching Assembly (630/1/35320)

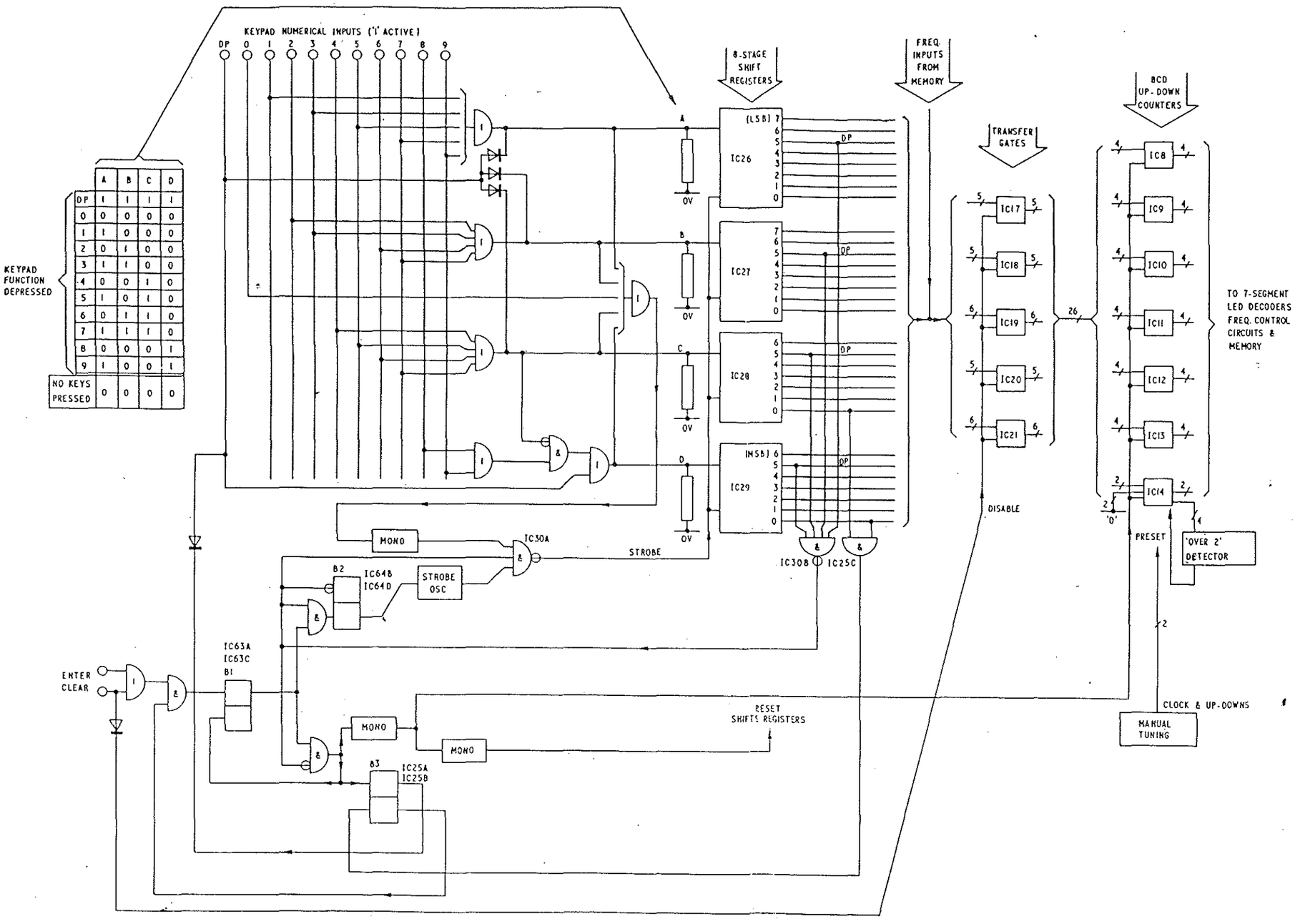
Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
PCB9	Memory Channel Select Board	Plessey	419/1/18148
PCB10	Memory Channel Select Board	Plessey	414/1/18150
-	Switch, Push	Cherry M61-0110	408/4/51494/001
-	Switch, Retaining Plate	Plessey	630/2/35321

Panel, Electronic Circuit (419/1/18148)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Panel Printed Circuit	Plessey	419/2/18149
	Socket Semi-Conductor Device	Texas C831402	508/4/22194/002
	Socket Semi-Conductor Device	Texas C831602	508/4/22194/003
C1	Capacitor 0.01uF ± 5% 400V	Siemens B32560-B3103J	435/4/90317/029
C3	Capacitor 0.1uF ± 5% 100V	Siemens B32560-B1104J	435/4/90317/014
C2	Capacitor 0.33uF ± 5% 100V	Siemens B32560-B1334J	435/4/90317/018
C4	Capacitor 10uF ± 20% 16V	ITT TAG 10/16	402/4/57057/008
IC1	Integrated Circuit	Motorola MC14011BCP	445/4/02383/011
IC2	Integrated Circuit	Motorola MC14520BCP	445/4/02383/020
IC3	Integrated Circuit	Motorola MC14008BCP	445/4/02383/008
IC4	Integrated Circuit	Motorola MC14081BCP	445/4/02383/081
IC5	Integrated Circuit	Motorola MC14049UBCP	445/4/02383/049
R1	Resistor 1k ± 2% 0.25W	Electrosil TR4	403/4/05523/100
R5	Resistor 10k ± 2% 0.25W	Electrosil TR4	403/4/05524/100
R2	Resistor 100k ± 2% 0.25W	Electrosil TR4	403/4/05525/100
R4	Resistor 1M ± 5% 0.25W	Allen Bradley CB	403/4/04361/003
R3	Resistor 10M ± 10% 0.33W	Mullard CR25	403/4/78482/105
D1-4	Diode	Texas 1N4148	415/4/05720

Panel, Electronic Circuit (419/1/18150)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
	Panel Printed Circuit	Plessey	419/2/18151
	Socket Semi-Conductor Device	Cambion 703-5314-01-04-12	508/4/22194/002
	Socket Semi-Conductor Device	Cambion 703-5316-01-04-12	508/4/22194/003
IC1	Integrated Circuit	Motorola MC14511BCP	445/4/02383/511
IC2,3	Light Emitting Diode Red	Hewlett-Packard 5082-7653	520/4/97672/001
R1-8, 11,12	Resistor 1k ± 2% 0.25W	Electrosil TR4	403/4/05523/100
R9	Resistor 10k ± 2% 0.25W	Electrosil TR4	403/4/05524/100
R10	Resistor 22k ± 2% 0.25W	Electrosil TR4	403/4/05524/220
TR1	Transistor	Ferranti ZTX502L	417/4/01876



MODULE 10. BASIC KEYPAD - DISPLAY LOGIC : FUNCTIONAL DIAGRAM

FIG. 1

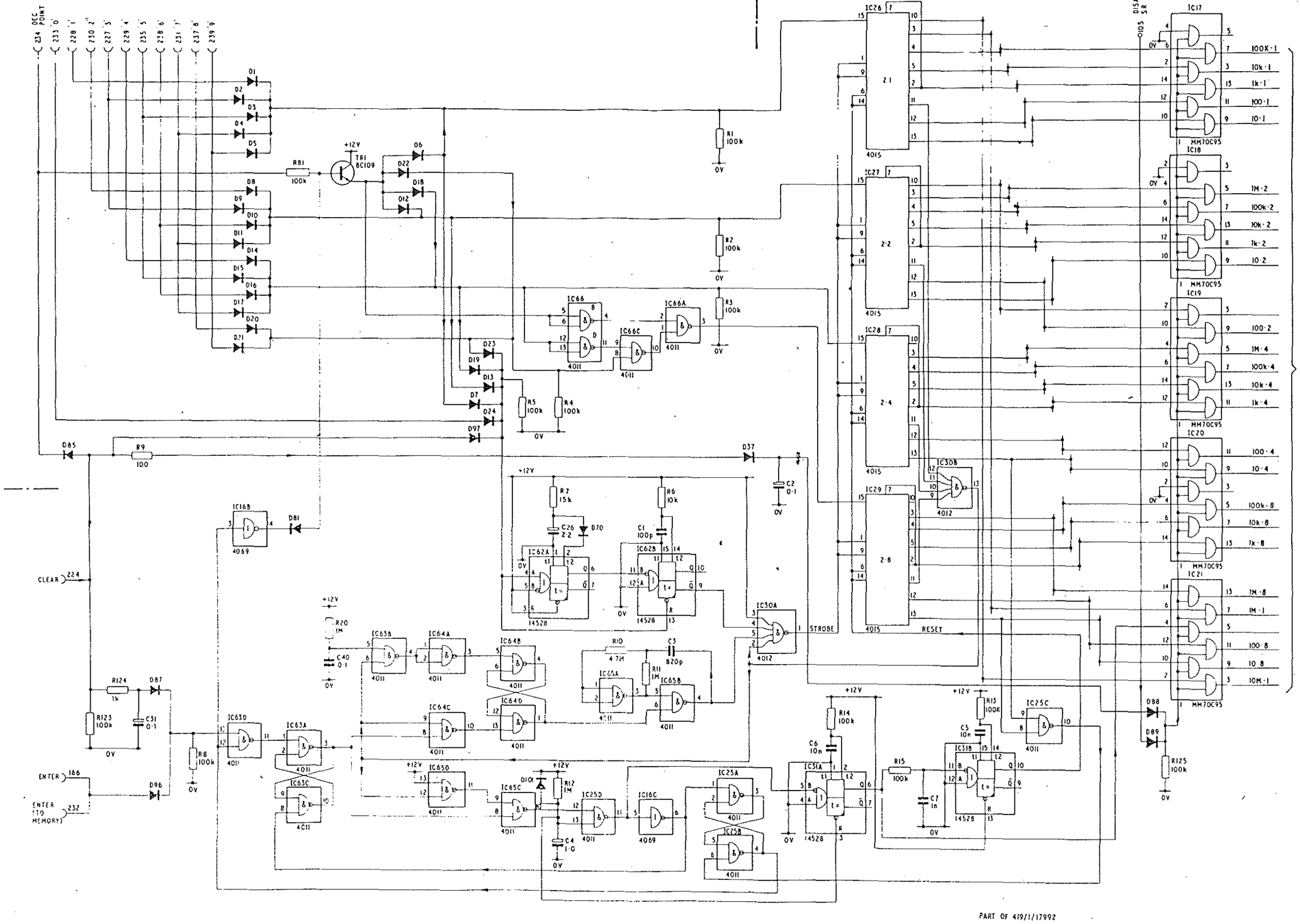
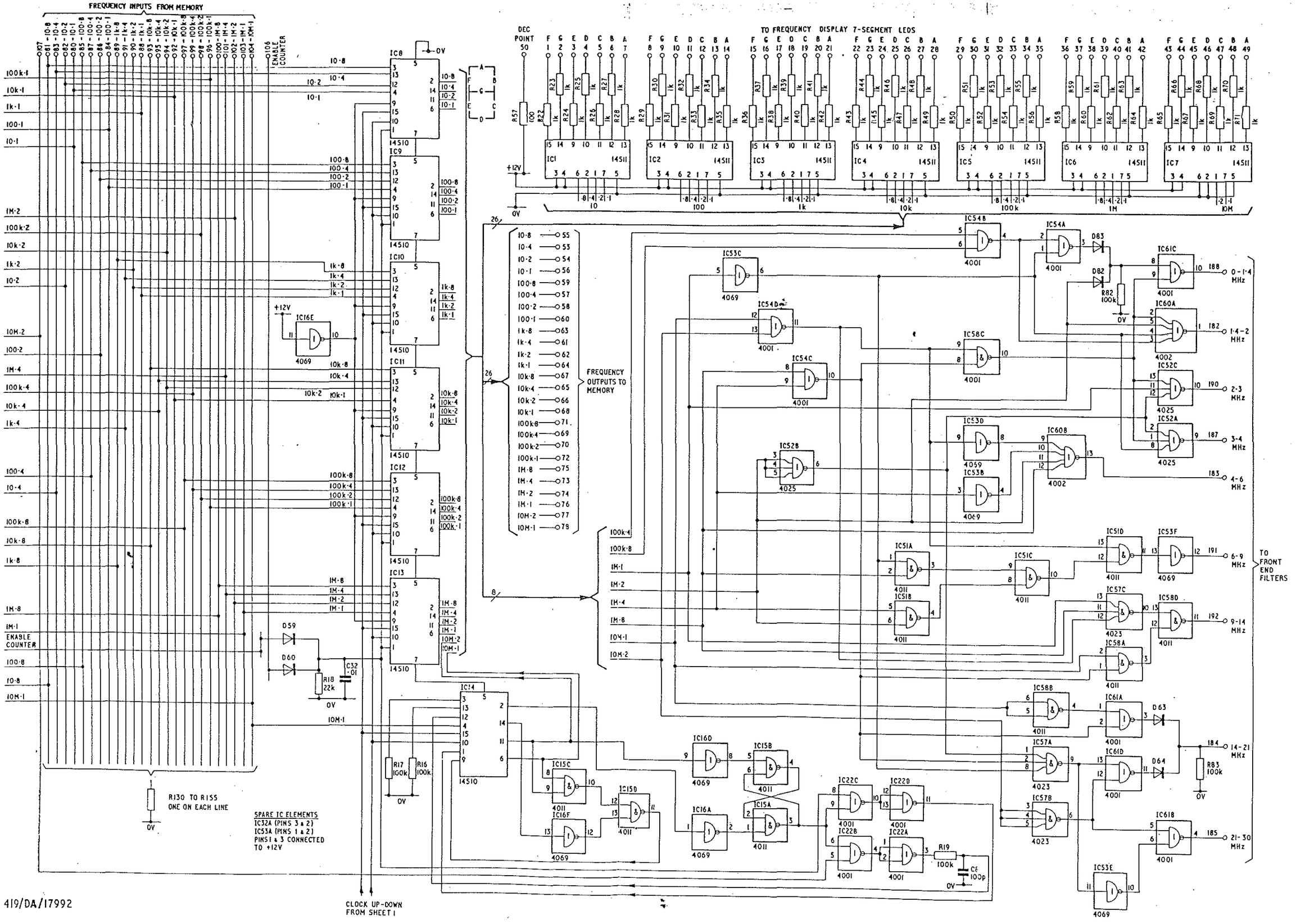


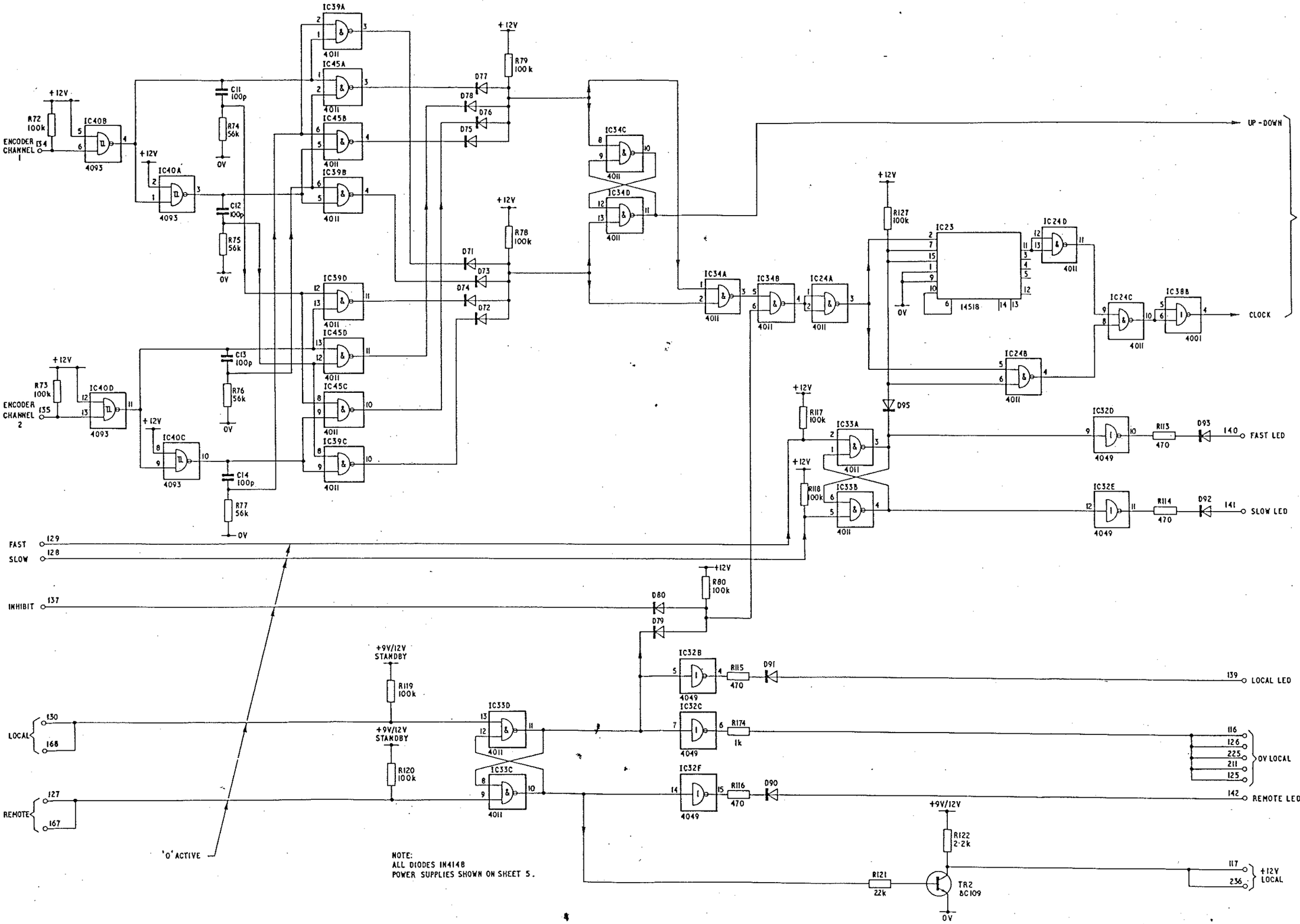
FIG 2

MODULE 10 KEYPAD CIRCUITS(a)



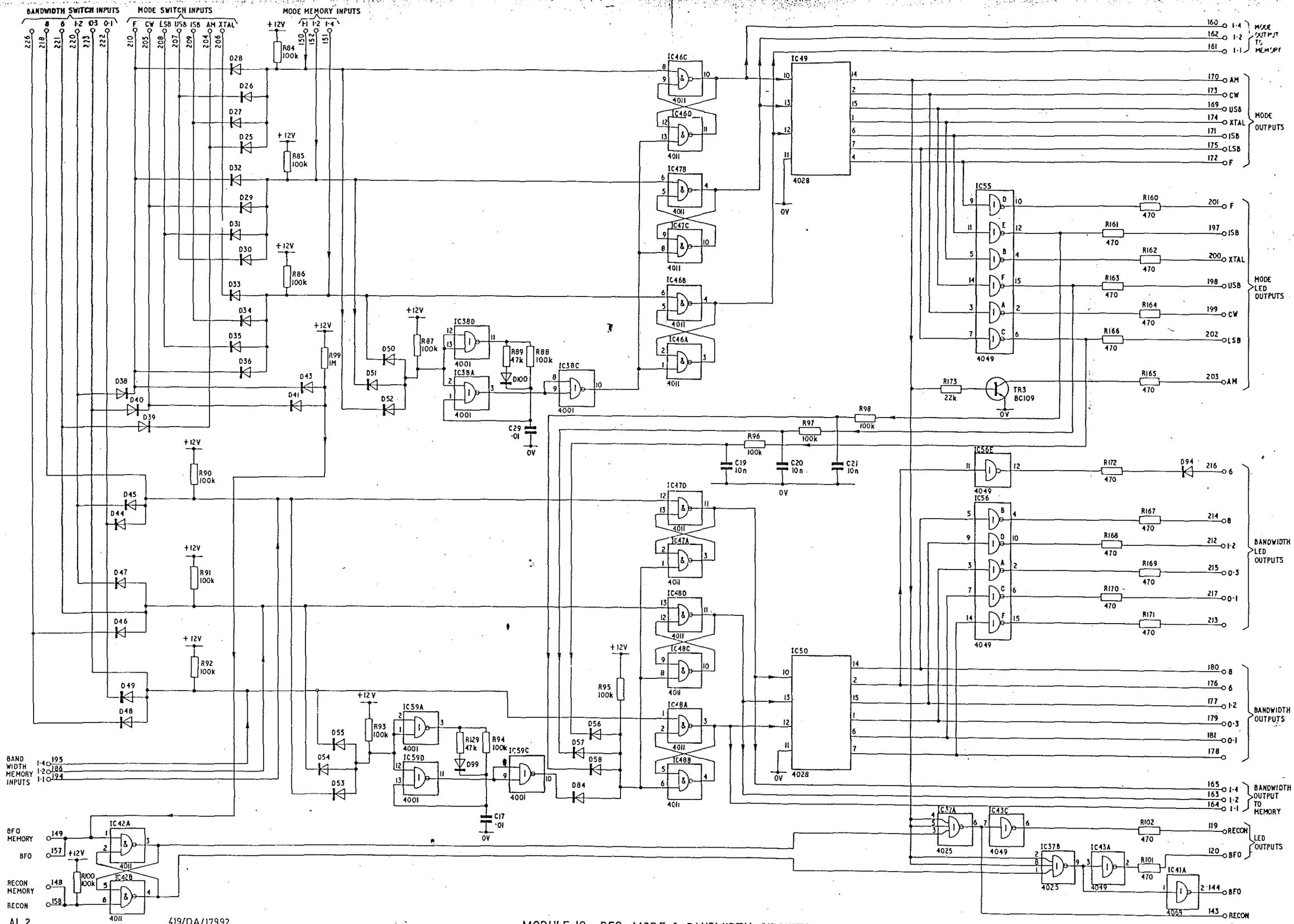
MODULE 10 : KEYPAD CIRCUITS (b)

FIG 2



MODULE 10 : MANUAL TUNING & LOCAL - REMOTE CIRCUITS

FIG 3



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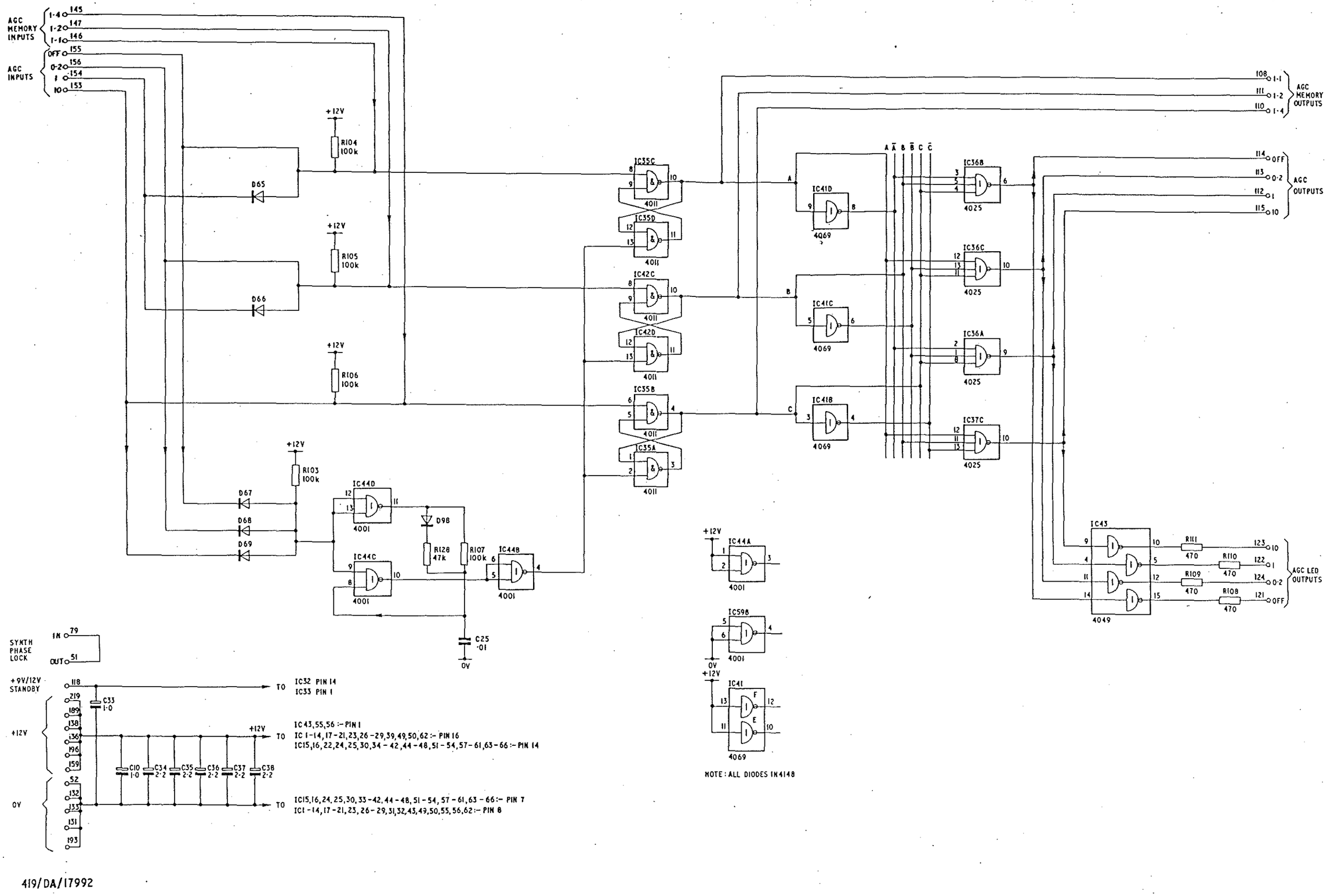
MODULE 10 : BFO, MODE & BANDWIDTH CIRCUITS

FIG 4



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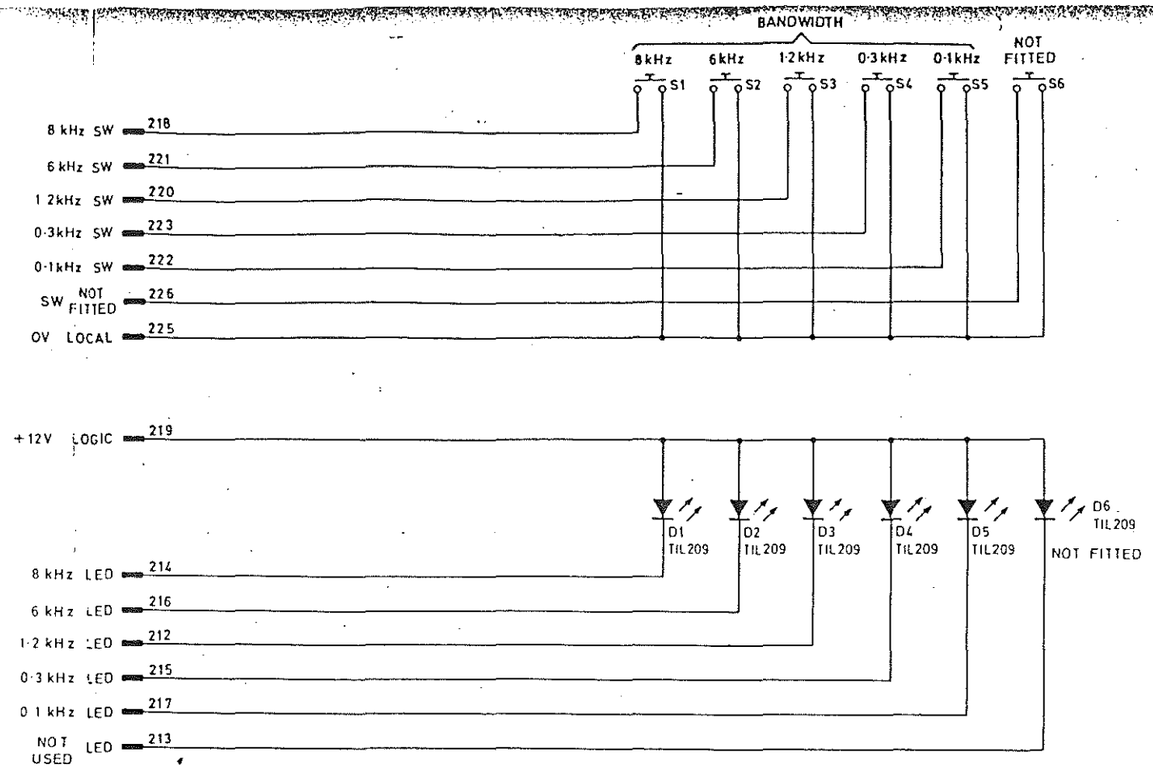
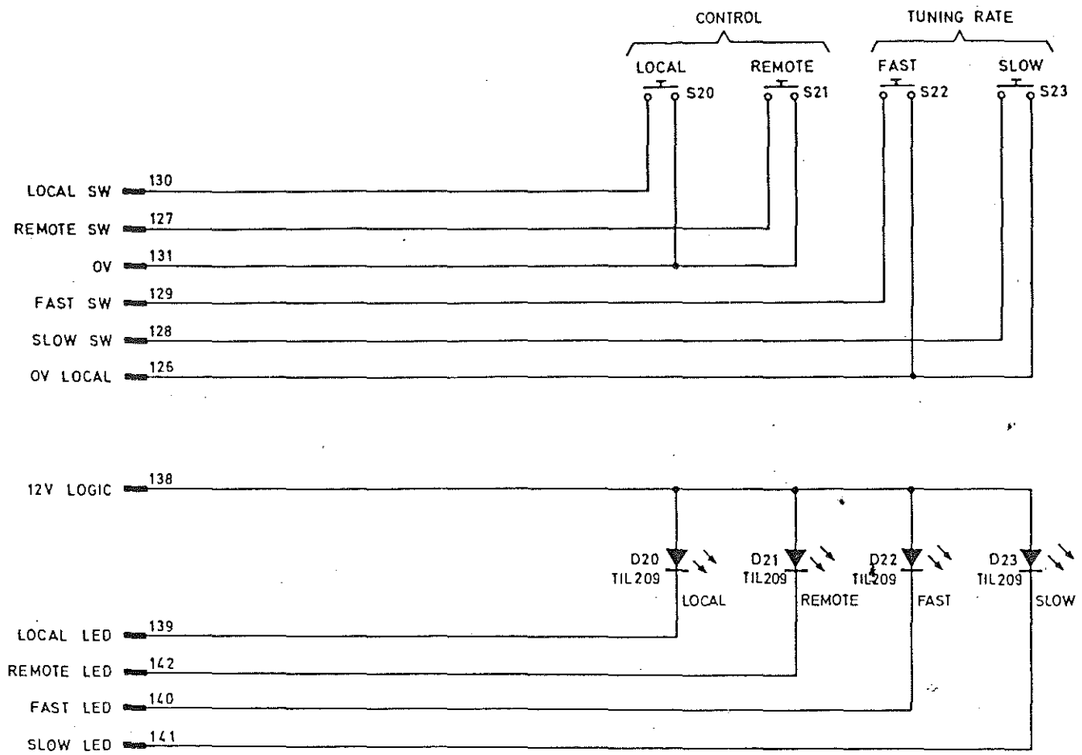
MODULE 10 : AGC & POWER CIRCUITS

FIG 5



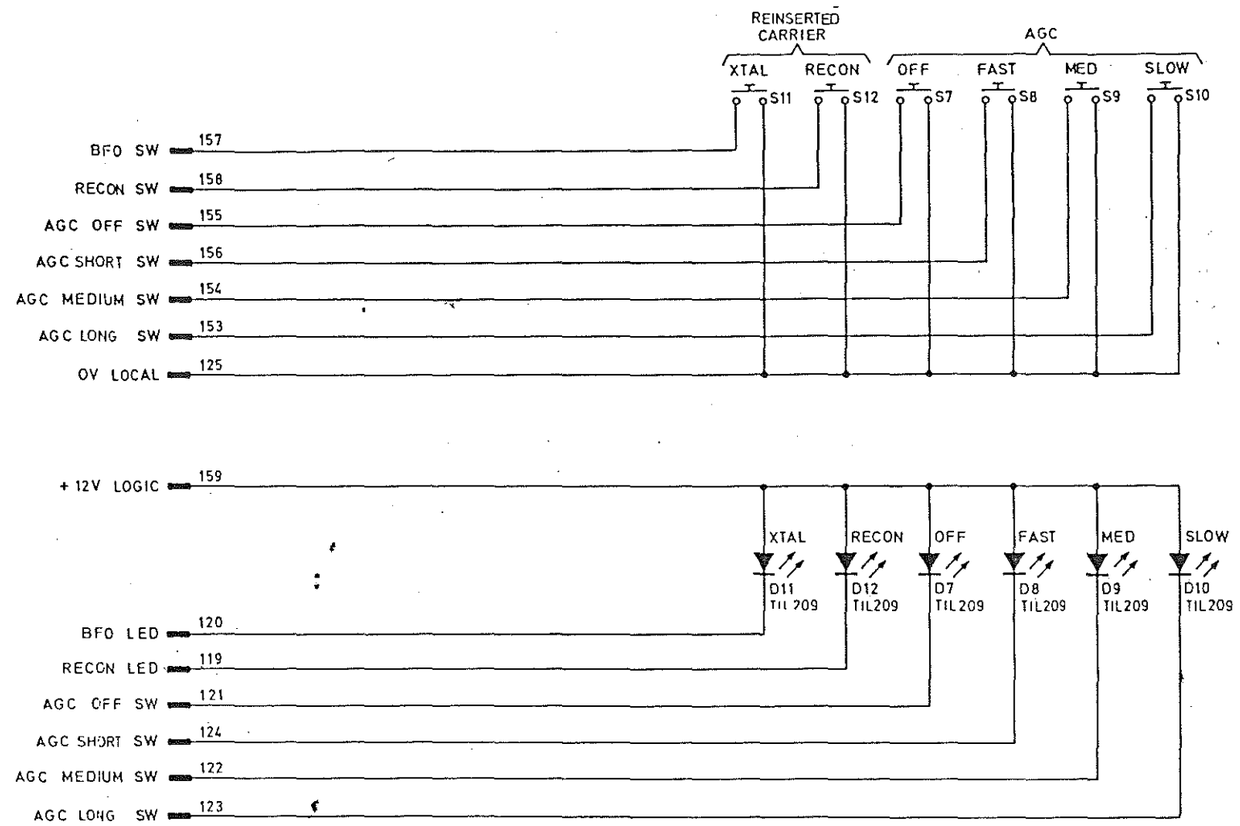
419/DA/18083

MODULE 10 : FRONT PANEL, KEYBOARD & BANDWIDTH CONTROLS CIRCUIT DIAGRAM FIG 6



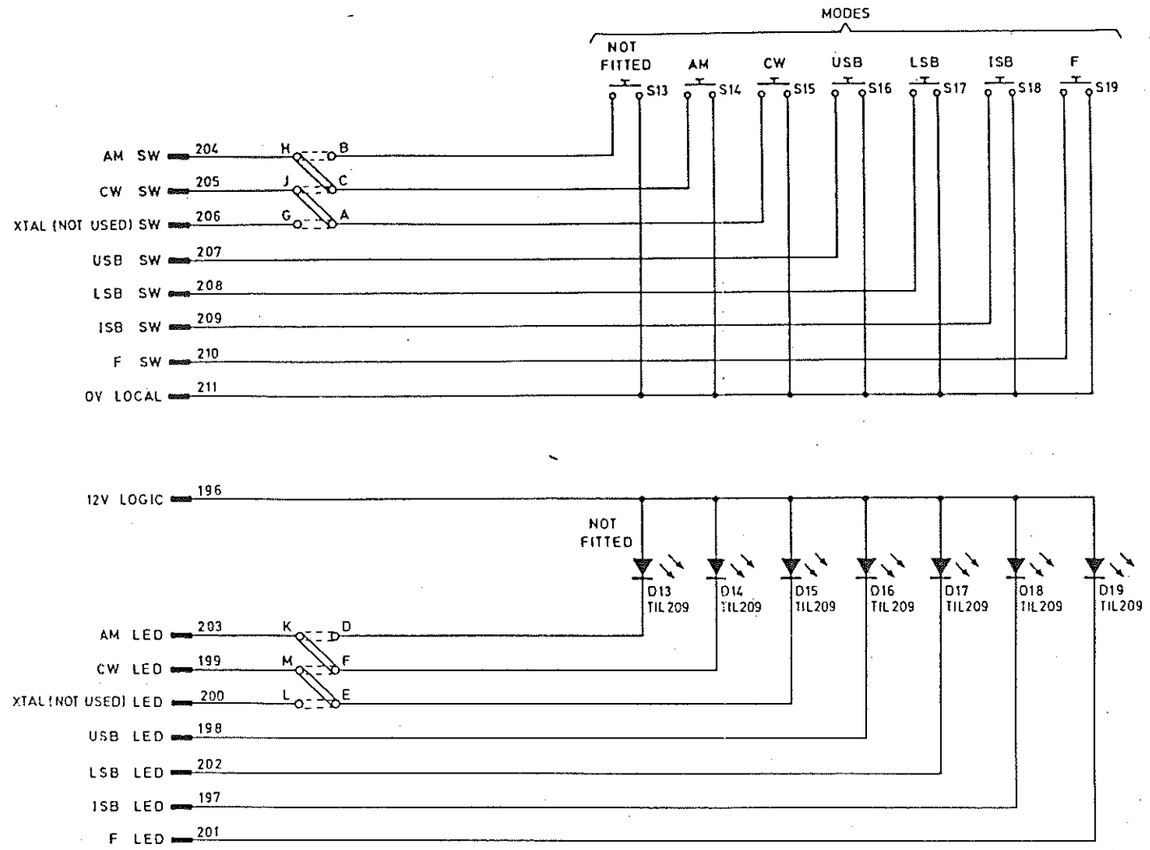
419/DA/18071

MODULE 10 : FRONT PANEL TUNING RATE AND CONTROL CIRCUIT DIAGRAM FIG 7



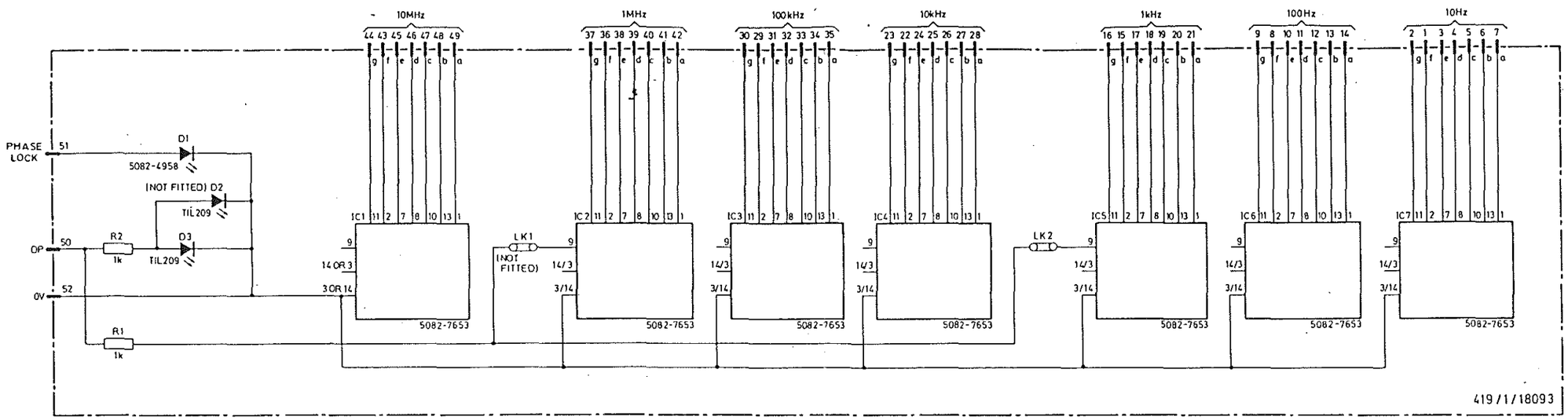
419/DA/!8079

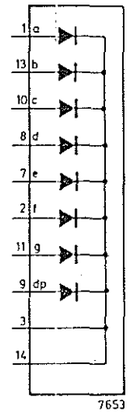
MODULE 10 : FRONT PANEL AGC CONTROL CIRCUIT DIAGRAM FIG 8



419/DA/18089

MODULE 10 : FRONT PANEL MODE CONTROL CIRCUIT DIAGRAM FIG 9

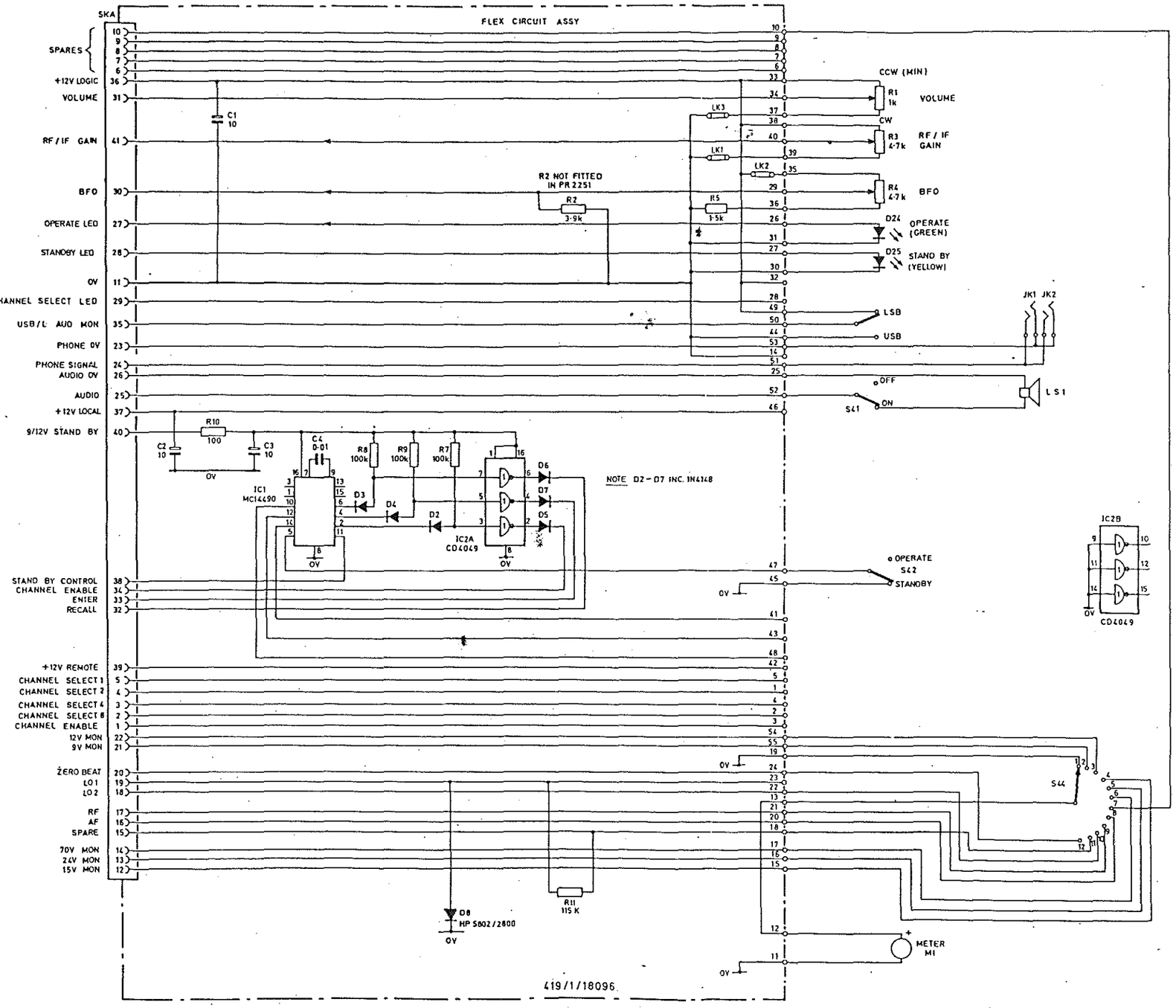




NOTE
LINK 1 DISPLAY kHz
LINK 2 DISPLAY MHz

MODULE 10 : DISPLAY CIRCUIT DIAGRAM

FIG 10



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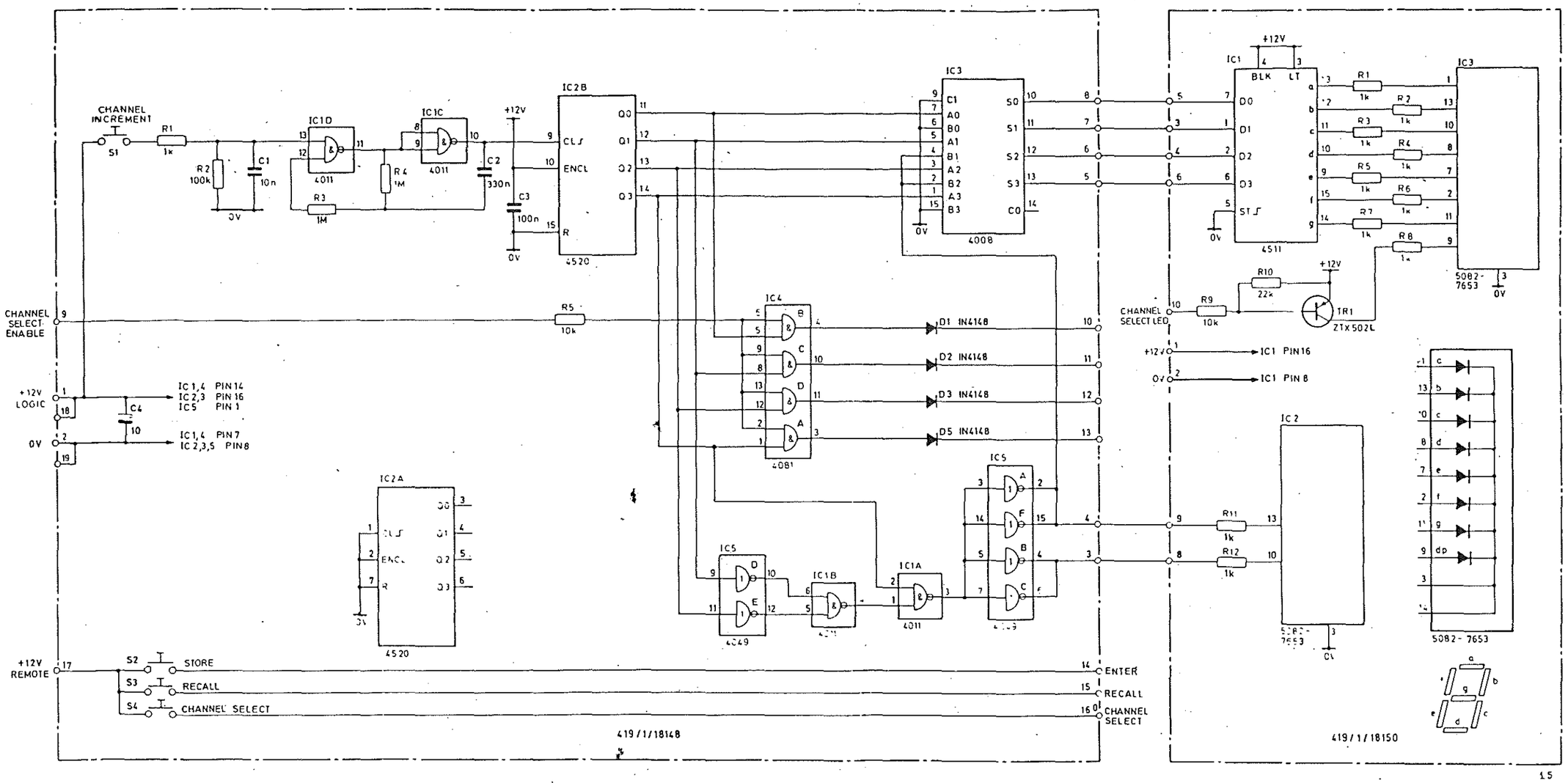
MODULE 10 : AUXILIARY PANEL CIRCUIT DIAGRAM

FIG 11



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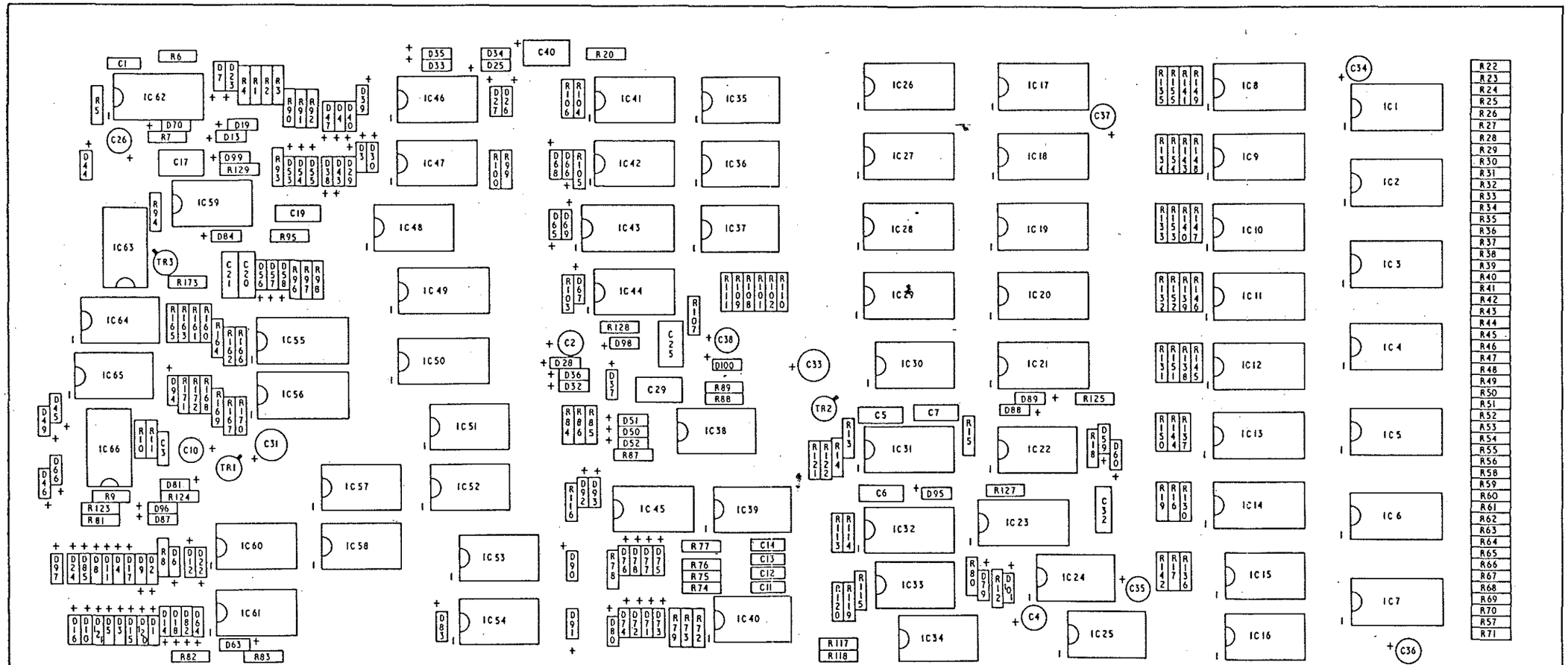
MODULE 10 : MEMORY CHANNEL SELECT CIRCUIT DIAGRAM

FIG 12



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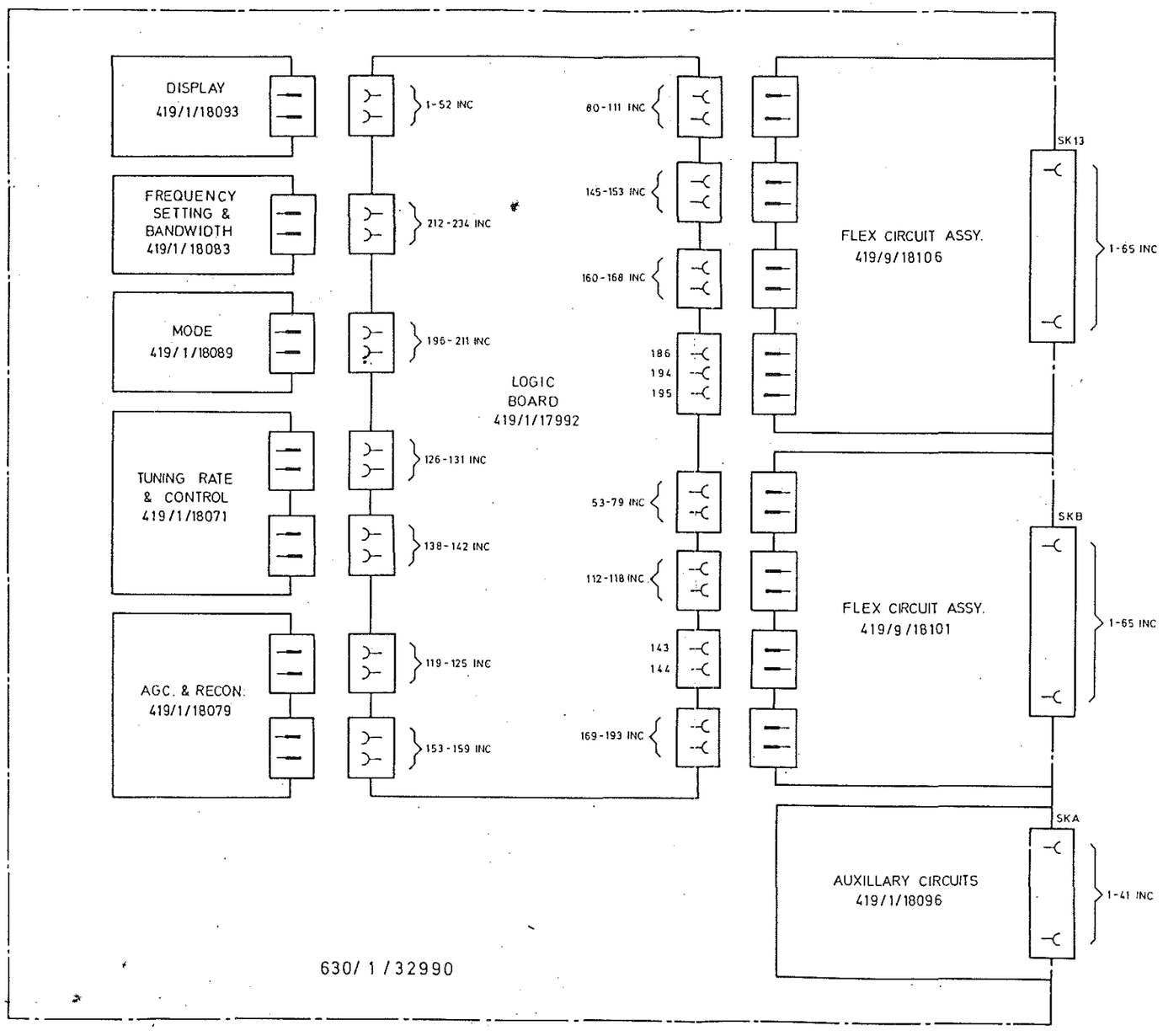
MODULE 10 LOGIC PANEL-COMPONENT LAYOUT

FIG. 13



630/DB/32990/001

MODULE 10 : INTERCONNECTION DIAGRAM

FIG 14

INTEGRATED CIRCUIT DEFINITIONS

This information forms a supplement to the circuit diagrams in respect of complex integrated circuits which are shown diagrammatically by a rectangular outline only.

MC 14015

Two separate 4-bit shift registers with outputs Q0 to Q3. Data to input D clocked in on positive-going edge at input CL provided that input R = '0'. Input R = '1' sets all Q outputs to '0'.

MC 14518 and MC 14520

Dual BCD counters

CL	ENC	R	ACTION
⌐	1	0	) Count
0	¬	0	) incremented
¬	X	0	)
X	⌐	0	) no
⌐	0	0	) change
1	¬	0	)
X	X	1	All outputs '0'

MC 14510

BCD up-down counter. Counts up or down from a preset value entered on P0, P1, P2, P3 when ENP = '0'. Count is up when UP-DOWN = '1', and down when UP-DOWN = '0'. Input R = '1' sets all Q outputs to '0'.

MC 14511

BCD input 7-segment LED decoder-driver. A BCD number between 0 and 9 is applied to D0 (LSB) D1, D2, D3 (MSB). Outputs 'a' to 'g' directly drive a 7-segment LED display to produce the corresponding number. Normal operation is produced with BLK and L TEST inputs both at '1'. BLK = '0' produces a blank display; L TEST = '0' produces an '8' display. An input BCD value greater than 9 produces a blank display.

MC 14028

BCD to decimal decoder. A 0 to 9 BCD input on D0 (LSB), D1, D2, and D3 (MSB) produces a '1' level on the corresponding one of outputs S0 to S9. A BCD input value greater than 9 sets all S output lines to '0'.

MC 14008

Four-bit full adder. Forms the sum of A+B+CIN where A and B are four-bit numbers.

S0, S1, S2, S3 and C0 are five-bit full sum. If S0-S3 is a 4-bit sum, C0 is carry.

C0 = '0' if the full sum is 15 or less.
C0 = '1' if the full sum is greater than 15.

CHAPTER 11

MODULE 11 MEMORY

CONTENTS

ILLUSTRATIONS

APPENDICES

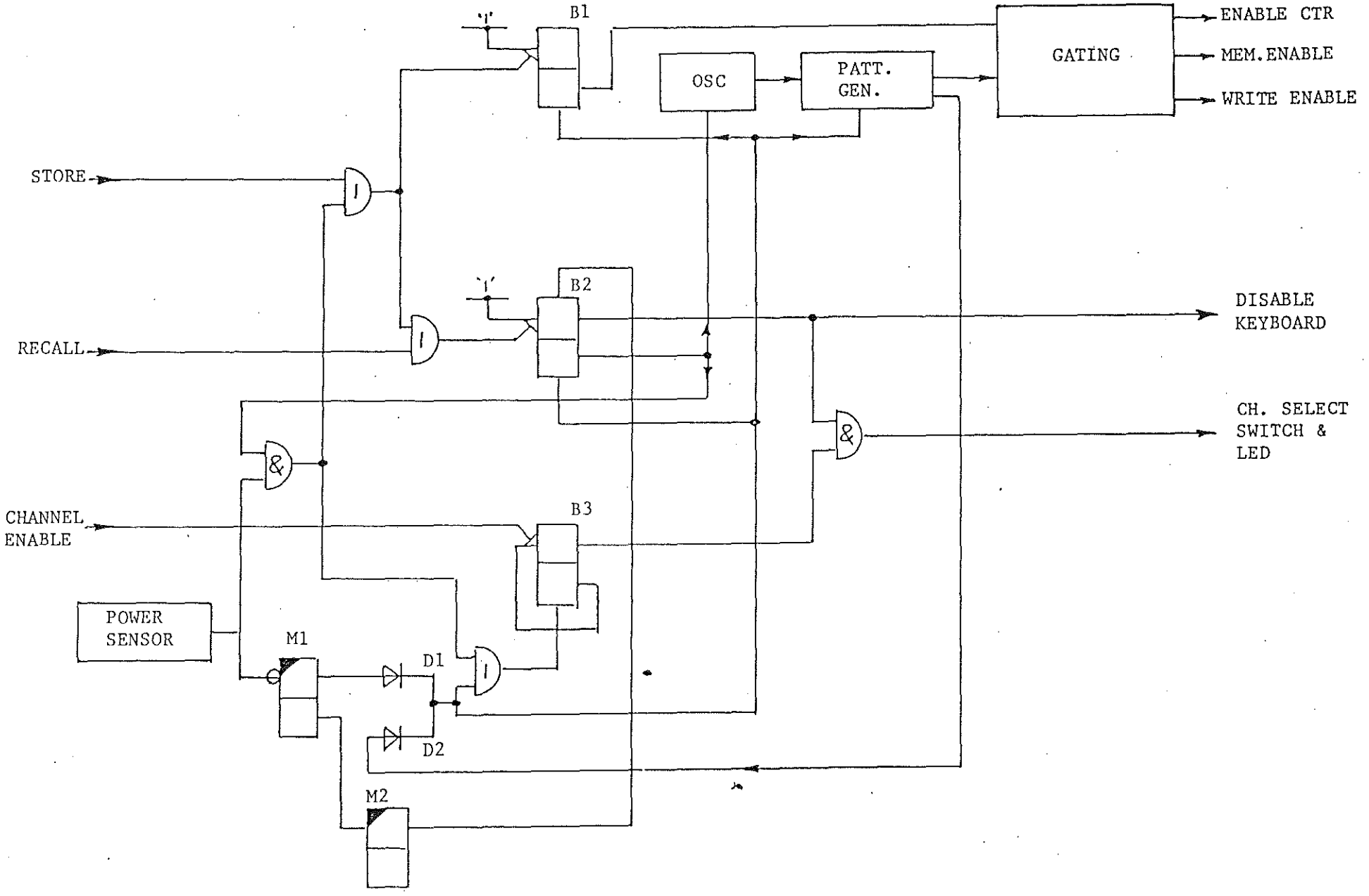


FIG (a) MODULE 11 FUNCTIONAL BLOCK DIAGRAM

MODULE 11 MEMORY

1. GENERAL

Module 11 contains a 16-channel 40-bit read-write memory and associated control circuits. Receiver control settings can be stored and recalled as required by the operator. The circuit is battery-maintained while power is disconnected. At switch-off, the settings in use are automatically stored. On switch-on, the settings last in use are automatically recalled.

2. FUNCTIONAL DESCRIPTION (Figure (a))

2.1 Power

Normally, power supply is drawn from the receiver PSU. While power is disconnected, Module 11 is powered by a rechargeable battery: this battery is trickle-charged when the receiver is connected to an a.c. supply and should not normally require any attention. A sensor circuit monitors continuously whether the receiver is on, in standby, or disconnected from a.c. power (and also covers PSU breakdowns, which it interprets as disconnections from a.c. power).

2.2 Memory

A 16-channel 40-bit read-write memory is fitted. 39 of the 40 bits are used. Inversion occurs between data input and data output. Channel selection is by means of a parallel 4-bit binary numerical input between 0 and 15. To read out, a '0' level is applied to the 'Memory Enable' input. To write in, a '0' level is applied to both the 'Memory Enable' and the 'Write Enable' inputs.

2.3 Memory Control (Figure (a))

2.3.1 'Power Off' State

During 'power off', Module 11 is battery powered, and this fact is recognised by the output from the power sensor standing at '1'. This state of affairs is static, and maintains the state into which the control circuit was set when the battery took over.

2.3.2 Switch-on

Switching from STANDBY to OPERATE changes the POWER Sensor output level from '1' to '0'. This 1-0 transition fires monostable M1, producing a reset pulse via D1 which resets the Q levels of all three bistables to '0' and also resets the pattern generator. At the end of the pulse from M1, the trailing edge fires monostable M2, which sets B2 Q level to '1'. This '1' level is fed out to disable the front-panel keyboard. Also, as $B3\overline{Q}$ level is '0', no supply is fed to the four effective switches of the front-panel Channel Select Switch: therefore, irrespective of switch position, all outputs are '0' and therefore memory channel 0 is selected.

2.3.3

The $B2\overline{Q}$ level at '0' allows the oscillator to run, so clocking the Pattern Generator. This then runs through a pattern and, at the end, produces a reset pulse. This reset pulse, via D2, acts exactly as does the reset pulse from monostable M1. $B2\overline{Q}$ level becomes '1', stopping the oscillator. The pattern output is gated with $B1\overline{Q}$ (at 1) to produce a '1-0-1' 'Memory Enable' output pulse and an 'Enable Counter latch' pulse. The first of these pulses produces a memory read-out of the channel 0

content, while the second allows the frequency control up-down counters in Module 10 to react to the input applied from the memory. An automatic sequence has therefore been initiated by switching on the receiver, in which the content of memory channel 0 has been applied to the receiver.

2.3.4 Power Loss or Switching to 'Standby'

Switching from OPERATE to STANDBY (or loss of power) changes the power sensor output level from '0' to '1'. The stable (quiescent) state after initial read-out from channel 0 is:

B1 Q = 0
B2 Q = 0
B3 Q = 0

B2$\overline{Q}$ level is therefore '1', and the AND function connected to the Power Sensor output is therefore able to apply the '0-1' power sensor output transition via further gating to clock both B1 and B2. B1$\overline{Q}$ then sets to '0', as does B2$\overline{Q}$. This allows the oscillator to run, causing the pattern generator to run through one pattern and then reset. The pattern output is gated with B1$\overline{Q}$ at '0' to produce '1-0-1' 'Memory Enable' and 'Write Enable' pulses. As B3Q level is '0' no supply reaches the Channel Select Switches, which therefore select channel 0. An automatic sequence has therefore been initiated by switching off the receiver, in which the receiver settings have been stored in memory channel 0.

2.3.5 'Store' Action

Store action will start from the end point of the actions described in 2.3.2 and 2.3.3, i.e.:

B1 Q : '0'
B2 Q : '0'
B3 Q : '0'
Oscillator : stopped

Operating the 'Store' button produces a '0-1-0' input pulse which via two OR functions, clocks B1 and B2. B1$\overline{Q}$ level becomes '0' and B2$\overline{Q}$ level also becomes '0'. The oscillator starts and the pattern generator cycles and resets. As B1$\overline{Q}$ level is '0', the gating produces a 'Write Enable' pulse. As B3Q level is '0', no supply is available to the Channel Select Switch and therefore the receiver settings are stored in channel 0.

2.3.6 If, instead of channel 0, another channel is to be used, that channel number is first set on the Channel Select Switch and the Channel Enable button is operated; this clocks B3, setting B3Q level to '1'. As B2Q is also '1', the Channel Select Switch receives a supply and the appropriate binary output is produced. Also, the Channel Enable LED is illuminated. Then, the 'Store' button is operated. If, in Channel Selection, an error is made before pressing the 'Store' button, a second operation of Channel Enable will reset B3.

2.3.7 Recall Action

Recall action will, like 'store' action, start from the end-point of the actions described in 2.3.2 and 2.3.3. Operating the 'Recall' button clocks B2 alone, setting B2Q to '1'. Again, this starts the oscillator, cycles the pattern generator, and resets. However, as in this case B1

has not been clocked, B1Q level is '1'. This reacts upon the gating so that only Memory Enable and Counter Enable output pulses are produced.

3. CIRCUIT DESCRIPTION

3.1 Memory

3.1.1 The 40-bit memory is made up from ten elements, IC14 to 22 and IC28. The Write Enable inputs of all elements are paralleled, as are the Read Enable inputs and the A-B-C-D channel selection inputs. Each element can store four parallel bits, inputs being applied on the D lines and outputs being obtained on the $\overline{S}$ lines. Inversion occurs, i.e. a '1' read in on D1 appears when read out as a '0' on $\overline{S1}$.

3.1.2 All D input lines are resistively connected to 0V by resistors which are mounted in IC packages, each containing fourteen. The frequency inputs from the front panel are applied via inverters to cancel the inversion inherent in the memory devices. Local-remote data comes in as one bit, and therefore is applied via inverter IC11D to the D3 input of IC28 as well as being directly applied to the D2 input: in this manner two separate output lines, 'local' and 'remote' are obtained.

3.2 Power

3.2.1 Under normal running conditions, power is supplied from the +9/12V output of Module 8 (PSU). This line is alive irrespective of whether the receiver is switched to 'OPERATE' or 'STANDBY'. It is fed directly to TR3 and TR4 only: all other circuits receive 9/12V power via D5 and D8. If the receiver is disconnected from the a.c. power supply, memory supply is maintained by a rechargeable 9V battery feeding via R17: under these conditions, TR3 and TR4 receive no supply.

3.2.2 Transistors TR3, 4, and 1 sense the power state. TR3 and TR4 are powered directly from the +9/12V line, and therefore can be in any one of three power states:

(a) No power (a.c. power off).

(b) +9V supply (standby)

(c) +12V supply (operate)

In the 'a.c. power off' state, TR3 emitter is at 0V, and therefore TR1 collector level is '1'. In the 'standby' state, insufficient voltage is developed across R16 to turn on TR4, and therefore TR3 is again non-conducting: TR1 collector level is therefore '1'. In the OPERATE state approximately 1V is developed across R16, and therefore TR4 and TR3 conduct: TR1 collector level is therefore '0'. The circuit senses whether or not the receiver is switched to OPERATE: it cannot differentiate between STANDBY state, a PSU failure, or removal or a.c. power.

3.2.3 If the receiver is switched from OPERATE to STANDBY, there is a delay (caused by the PSU) before the +9/12V level drops from +12V to +9V. As it is necessary to read the control settings into the memory immediately the receiver is switched to STANDBY it is not possible to wait for the +9/12V level to drop before doing so (TR1 collector level change from '0' to '1' initiates this read in). Therefore, the level at TR1 collector is OR connected by D2 and D3 with a line from the OPERATE-STANDBY switch which instantaneously changes level from '0' to '1' when the switch posi-

tion is changed from OPERATE to STANDBY; this change initiates the reading already referred to.

3.3 Memory Control

3.3.1 Switch-on

Switching the receiver from STANDBY to OPERATE changes the level at D2-D3 junction from '1' to '0'. This '1-0' transition fires monostable IC3A. The '0-1-0' Q output pulse resets IC1A, IC1B, IC2B (via IC7A), IC8A, and IC8B. The trailing edge of IC3A's Q output pulse fires monostable IC3B, producing a '0-1-0' Q output pulse which sets IC1B Q level to '1'. This Q level is fed out as DISABLE KEYBOARD and is also applied to IC6A. As IC2B Q level is '0', and is also applied to IC6A, CHANNEL SELECT COMMON level is '0'. The output from IC6A forms the supply to the front-panel CHANNEL SELECT push button: this push button is effectively four parallel single-pole switches which produce a parallel 4-bit binary equivalent of the number to which it is manually set. When IC6A output level is '0', the output from the CHANNEL SELECT push button is therefore binary '0', i.e., channel 0 (the temporary storage 'dump' channel) is automatically selected.

3.3.2 As IC1B $\overline{Q}$ level is '0', the oscillator formed by IC5A and IC5B is free to run. It clocks shift registers IC8A and IC8B, both of which function together as a pattern generator. After reset, all eight Q outputs are at '0'. They successively rise to '1' on each clock pulse. When Q3 or IC8B rises to '1' its connection back to the reset inputs causes all eight outputs to revert to '0' as shown in Figure (b). A typical resetting time is 100 nanoseconds.

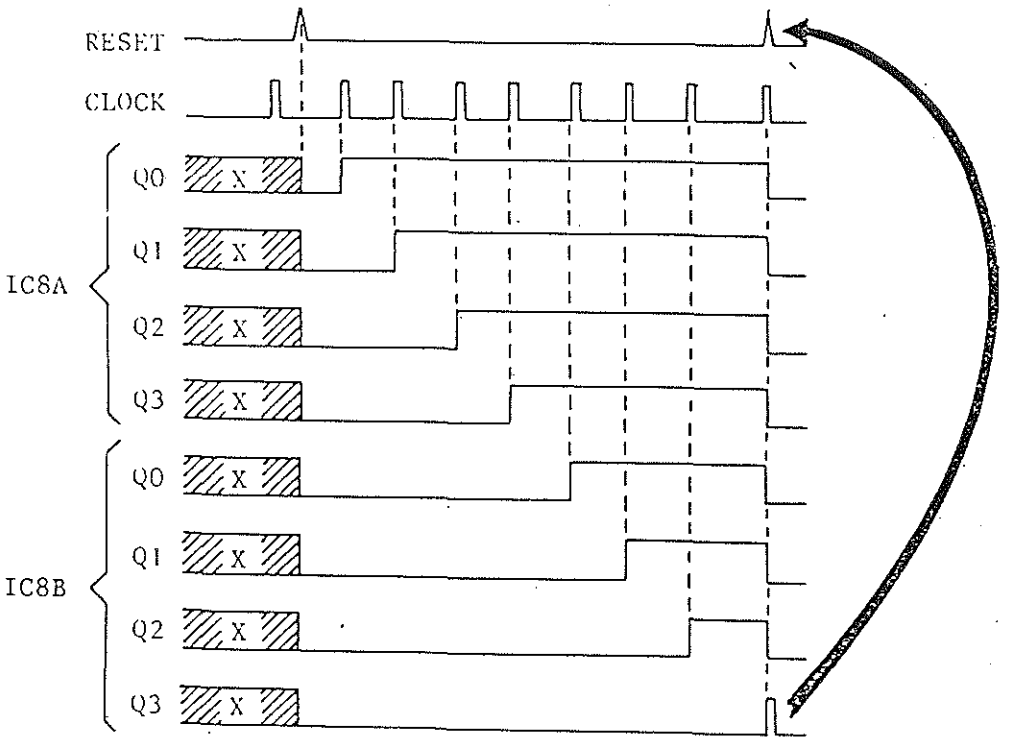


FIG (b) PATTERN GENERATOR ACTION

3.3.3 The reset pulse produced by IC8B-Q3 at the end of the pattern is OR connected (D4, D7, IC24E) with the Q output of monostable IC3A and therefore the effect of the IC8B-Q3 reset pulse is identical with that produced by

IC3A, namely, to reset IC1A, $\overline{IC1B}$, IC2B, as well as IC8A and IC8B. The resetting of IC1B produces a $\overline{Q}$ = 1 output which stops clock oscillator IC5A-IC5B.

3.3.4 The Q outputs of IC8 are gated with the Q and $\overline{Q}$ outputs of IC1A in IC4A, IC4B, IC4D, IC5C, IC5D, and IC6B as shown in Figure (c).

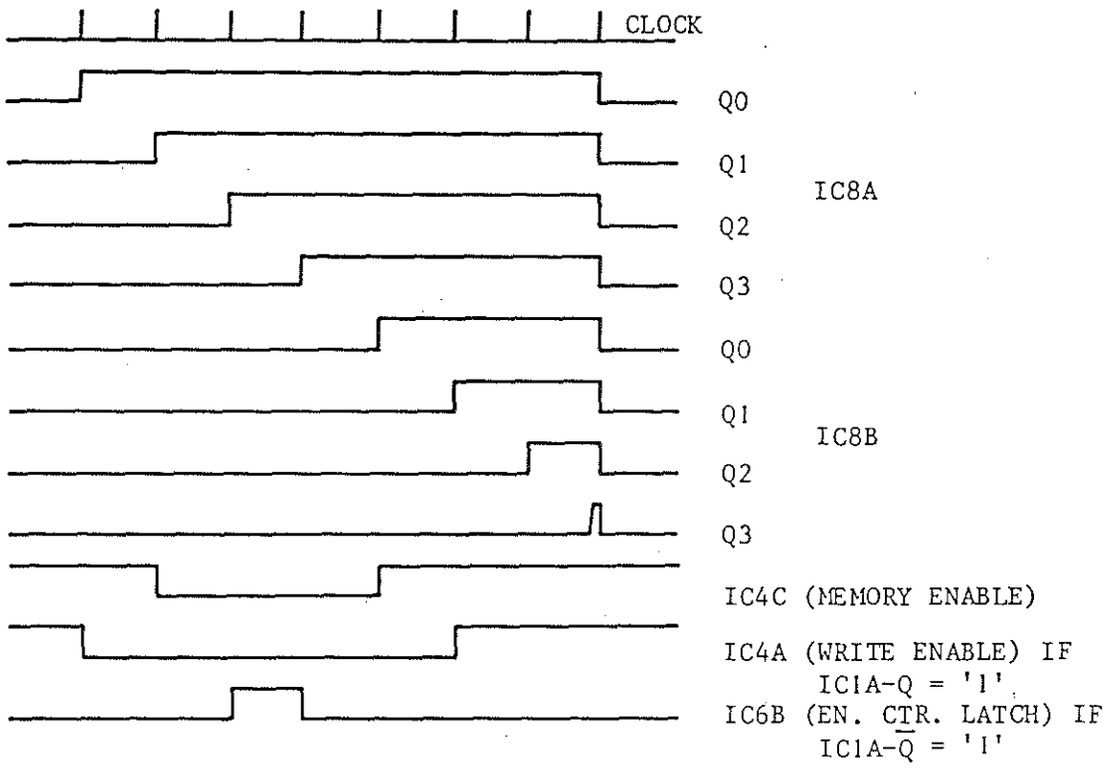


FIG (c) GATED OUTPUTS FROM IC8

As IC1A Q level is '0', only the MEMORY ENABLE and ENABLE COUNTER LATCH pulses are produced. The first, applied to the memory ICs, produces a memory read-out to Module 10. The second, applied to the frequency control up-down counters of Module 10, allows them to react to the frequency data produced by the memory read-out.

3.3.5 Power Loss or Switching to STANDBY

Switching the receiver from OPERATE to STANDBY (or any power failure which removes the +9/12V supply) changes the level at D2-D3 junction from '0' to '1'. The stable (quiescent) state after the initial read-out described in paras.3.3.1 to 3.3.4 includes the Q levels of IC1A, IC1B, and IC2B at '0'. IC1B $\overline{Q}$ level is therefore '1': this '1' level is applied to IC6C, allowing the '0-1' transition at D2-D3 junction to:

(a) clock IC1A via IC7B

(b) clock IC1B via IC7B and IC7C

Monostable IC3A is unaffected, therefore IC2B state does not change. As IC1A and IC1B D lines are connected to +12V, both Q outputs are clocked to '1'. The resultant '0' level at IC1B $\overline{Q}$ allows oscillator IC5A-IC5B to run, clocking pattern generator IC8. Both MEMORY ENABLE and WRITE ENABLE pulses are produced (see Figure (c)).

3.3.6 As IC2B is '0' no supply reaches the CHANNEL SELECT switches (i.e. IC6A output = '0'). A write-in to memory channel 0 therefore takes place.

3.3.7 Store Action

Store action starts from the same stable state as does the action described in paras.3.3.5 and 3.3.6. Operating the STORE button produces a '0-1-0' input pulse which, via IC7B and IC7C, clocks IC1A and IC1B. The two $\overline{Q}$ levels then become '0', and a pattern cycle is produced by IC8 as previously described (para.3.3.2 et. seq.). A WRITE ENABLE pulse is produced and, provided no input has been applied to the CHANNEL ENABLE input, data is written into channel 0 as IC2B Q level at '0' holds IC6A output at '0'.

3.3.8 If instead of channel 0 it is desired to write into another channel, the number of that channel is first set on the CHANNEL SELECT switch: when IC6A output level becomes '1', the selected number will appear in 4-bit parallel binary form on the A-B-C-D inputs of the memory ICs. After operating the CHANNEL SELECT switch the CHANNEL ENABLE button is pressed. This produces a '0-1-0' input pulse which clocks IC2B. As IC2B $\overline{Q}$ has been previously set to '1' (para.3.3.1), the clockpulse sets the Q level to '1'. As IC1B Q level is now also '1', IC6A receives a '1-1' input and therefore the CHANNEL SELECT switch receives a supply from edge-pin 15A. The appropriate binary output to the memory A-B-C-D inputs is now produced and the Channel Enable LED is illuminated.

3.3.9 Next, the STORE button is operated but, if an erroneous channel selection has been made, it can be cancelled by a second operation of CHANNEL ENABLE. This will again clock IC2B and return $\overline{Q}$ to '1'. The action produced by the STORE button has already been described (para.3.3.7).

3.3.10 Recall Action

Recall action commences from the same starting point as store action. Operation of the RECALL button clocks IC1B alone, setting the Q level to '1'. The oscillator runs, and a pattern cycle is produced by IC8. As IC1A has not been clocked, the Q level is '1' and no WRITE ENABLE pulse is produced.

4. TEST DATA

4.1 The test procedure for Module 11 is covered by the overall test procedures given in Chapter 2, Section 5 of this manual. Therefore no additional test data is required.

4.2 The test procedure consists of checking the operation of the memory controls and the associated LED indicators on the front-panel of Module 10. The LED indicators are driven via lamp drivers from the outputs of the control circuits, therefore an illuminated LED indicator may be considered as a final test of the control circuit and switch.

4.3 As Module 10 is employed when carrying out the checks on Module 11, it is essential to ensure that there are not faults on Module 10, as this will give a false indication of the condition of Module 11.

5. COMPONENT LISTS

Main Assembly (630/1/32991)
Panel Electronic Circuit (419/1/7994)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Panel Printed Circuit	Plessey	419/2/17995
-	Socket, Semi-Conductor	Texas 14L DIL C931402	508/4/22096/002
-	Socket, Semi-Conductor	Texas 16L DIL C931602	508/4/22096/003
C6	Capacitor 1nF ± 5% 400V	Siemens B32560	435/4/90317/023
C7	Capacitor 0.01uF ± 5% 400V	Siemens B32560	435/4/90317/029
C8	Capacitor 0.1uF ± 5% 250V	Siemens B32560	435/4/90317/014
C5	Capacitor 1uF ± 20% 35V	ITT TAG	435/4/57057/004
C9	Capacitor 2.2uF ± 20% 16V	ITT TAG	435/4/57057/007
IC5	Integrated Circuit	Motorola MC14001CP	445/4/02383/001
IC1,2	Integrated Circuit	Motorola MC14013CP	445/4/02383/013
IC4	Integrated Circuit	Motorola MC14023CP	445/4/02383/023
IC9-13	Integrated Circuit	Motorola MC14049CP	445/4/02383/049
IC7	Integrated Circuit	Motorola MC14075CP	445/4/02383/075
IC6	Integrated Circuit	Motorola MC14015CP	445/4/02383/015
IC8	Integrated Circuit	Motorola MC14528CP	445/4/02383/528
IC3	Integrated Circuit	Motorola MC74C89N	445/4/03083/
IC23-26	Resistor Package 16 lead	D.I.L. 898-1-100K	404/9/08061/001
R17	Resistor 270R ± 2%	Electrosil TR4	403/4/05522/270
R16	Resistor 330R ± 2%	Electrosil TR4	403/4/05522/330
R14	Resistor 470R ± 2%	Electrosil TR4	403/4/05522/470
R4,15	Resistor 1.5k ± 2%	Electrosil TR4	403/4/05523/150
R5,6	Resistor 10k ± 2%	Electrosil TR4	403/4/05524/100
R11,13	Resistor 22k ± 2%	Electrosil TR4	403/4/05524/220
R7	Resistor 47k ± 2%	Electrosil TR4	403/4/05524/470
R9,12	Resistor 100k ± 2%	Electrosil TR4	403/4/05525/100
R10	Resistor 1M ± 5%	AB Type CB	403/4/04361/003
D2-5,7,8	Diode	Texas 1N4148	415/4/05720
D1	Diode	Mullard BZY88 6V8	415/4/05738/012
TR1,2	Transistor	Mullard BC107	417/4/01777
TR3	Transistor	Mullard BC109	417/4/01776
TR4	Transistor	Mullard BC179	417/4/01860

Cableform Assembly (702/1/33359)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Cable Tie	Insulok Type T18R MS	915/4/98775/000
-	Sleeve Ident, Black 0	Hellerman 0.75mm x 3mm	915/4/04042/000
-	Sleeve Ident, Brown 1	Hellerman 0.75mm x 3mm	915/4/04042/001
-	Sleeve Ident, Red 2	Hellerman 0.75mm x 3mm	915/4/04042/002
-	Sleeve Ident, Orange 3	Hellerman 0.75mm x 3mm	915/4/04042/003
-	Sleeve Ident, Yellow 4	Hellerman 0.75mm x 3mm	915/4/04042/004
-	Sleeve Ident, Green 5	Hellerman 0.75mm x 3mm	915/4/04042/005
-	Sleeve Ident, Blue 6	Hellerman 0.75mm x 3mm	915/4/04042/006
-	Sleeve Ident, Violet 7	Hellerman 0.75mm x 3mm	915/4/04042/007
-	Sleeve Ident, Grey 8	Hellerman 0.75mm x 3mm	915/4/04042/008
-	Sleeve Ident, White 9	Hellerman 0.75mm x 3mm	915/4/04042/009

Clamp Battery Assembly (630/1/21997)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Clamp Battery	Plessey	630/2/32998
-	Press Nut	Rojan M3	999/4/03201/005
-	Spacer, Threaded	Harwin R6076 M3X27LG	630/2/31526/006
-	Mounting Bracket	Plessey	630/2/32953
-	Label	Plessey	630/2/34137
PL13	Plug, Electrical	Socopox 65-way 127-65 -XM27C5	508/4/22098
-	Battery Dry	Medicharge Type R9 B80-9V 80 mAH	999/4/32776/005
-	Lead, Electrical	Eagle BH9	

INTEGRATED CIRCUIT DEFINITIONS

This information forms a supplement to the circuit diagrams in respect of complex integrated circuits which are shown diagrammatically by a retangular outline only.

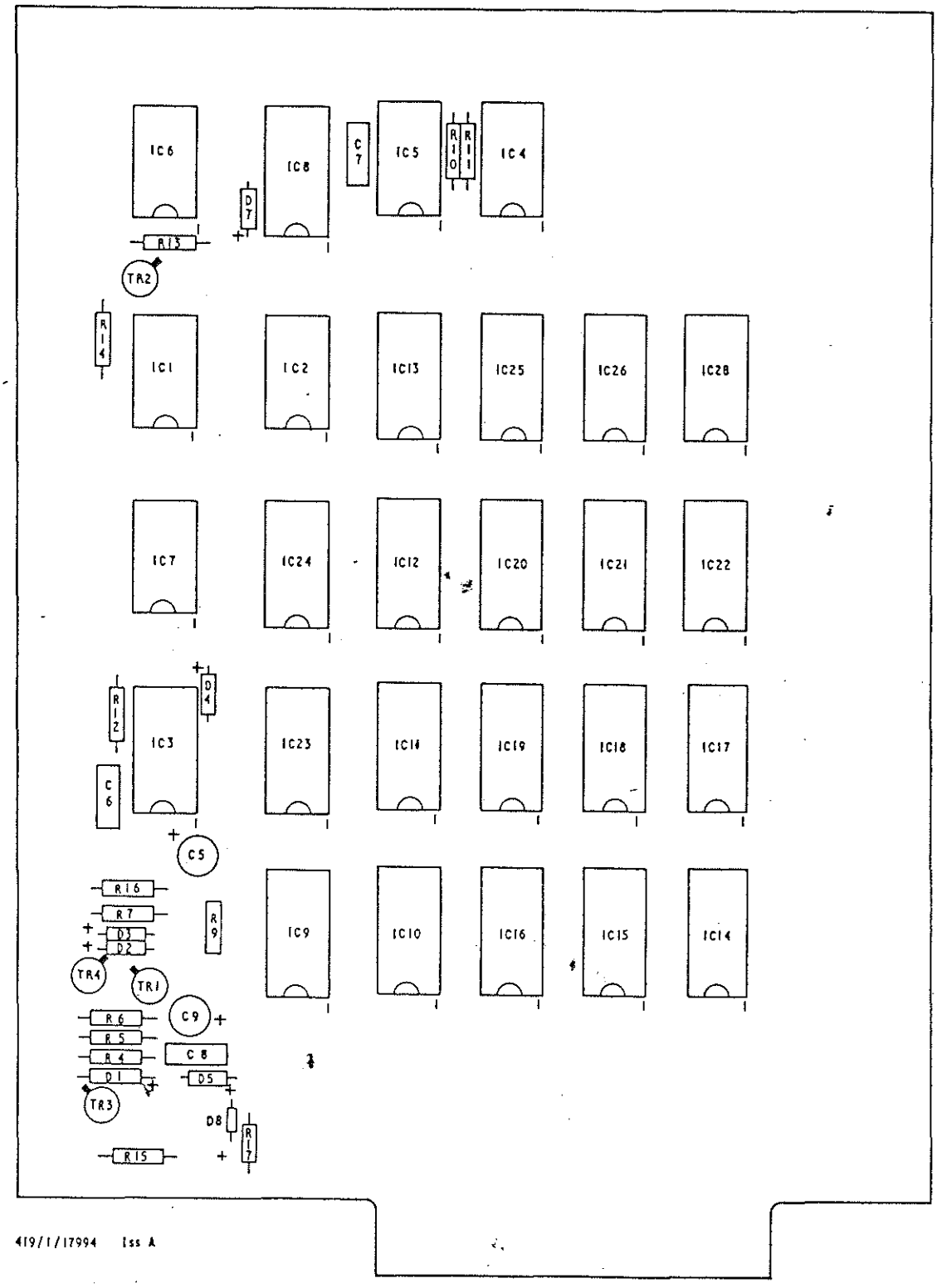
MC 14015

Two separate 4-bit shift registers with outputs Q0 to Q3. Data to input D clocked in on positive-going edge at input CL provided that input R = '0'. Input R = '1' sets all Q outputs to '0'.

MM 74C89

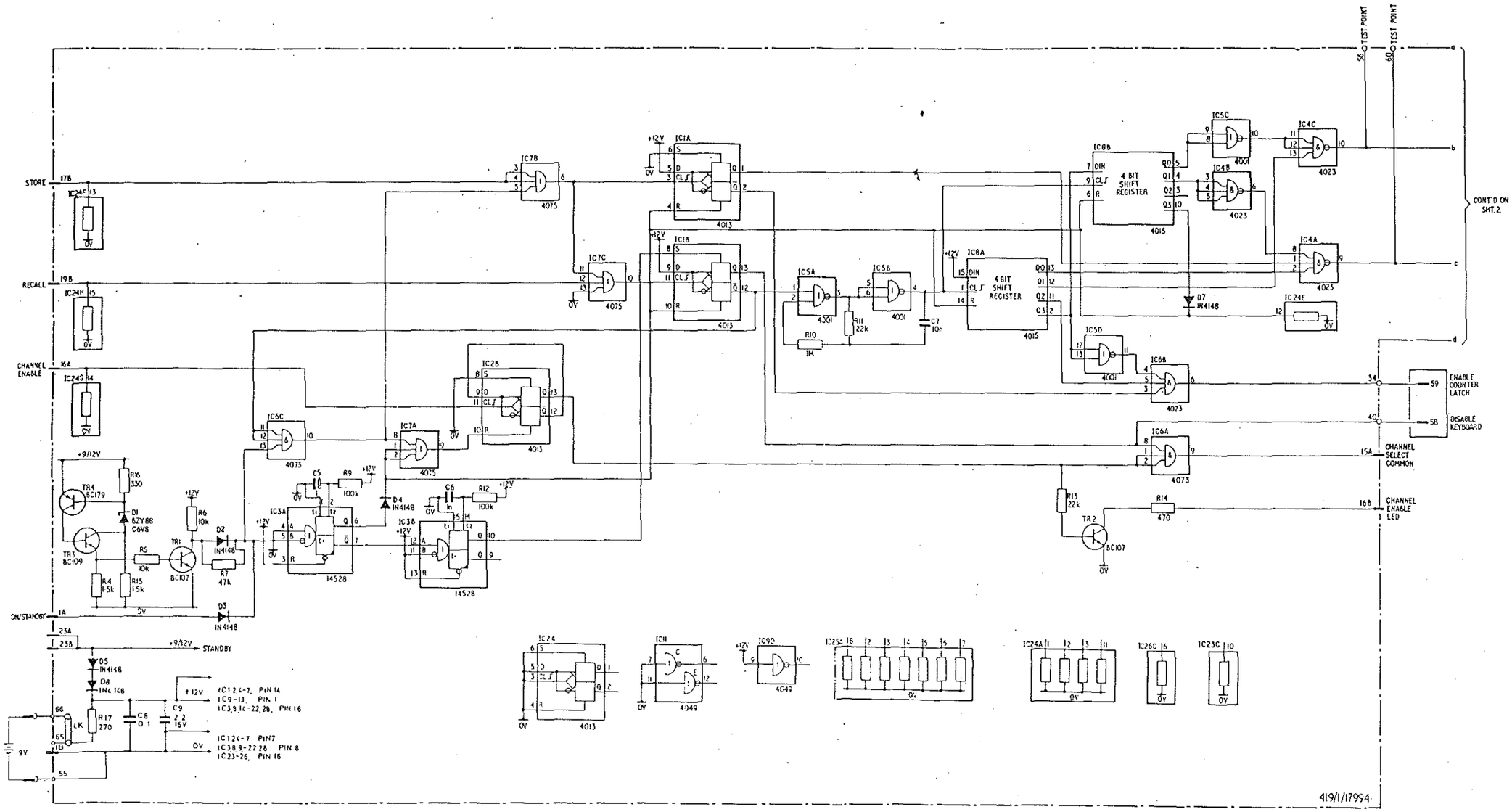
4-bit x 16 tri-state random-access read-write memory. Address input applied to ADDRESS INPUT A, B, C, and D. Data input applied to DATA INPUT 1, 2, 3, and 4. Outputs obtained on DATA OUTPUT 1, 2, 3, and 4.

$\overline{ME}$	$\overline{WE}$	OPERATION	OUTPUTS
0	0	Write	High-Z
0	1	Read	Selected word complement
1	0	Inhibit storage	High-Z
1	1	Inhibit storage	High-Z



MODULE II PANEL - COMPONENT LAYOUT

FIG. 3



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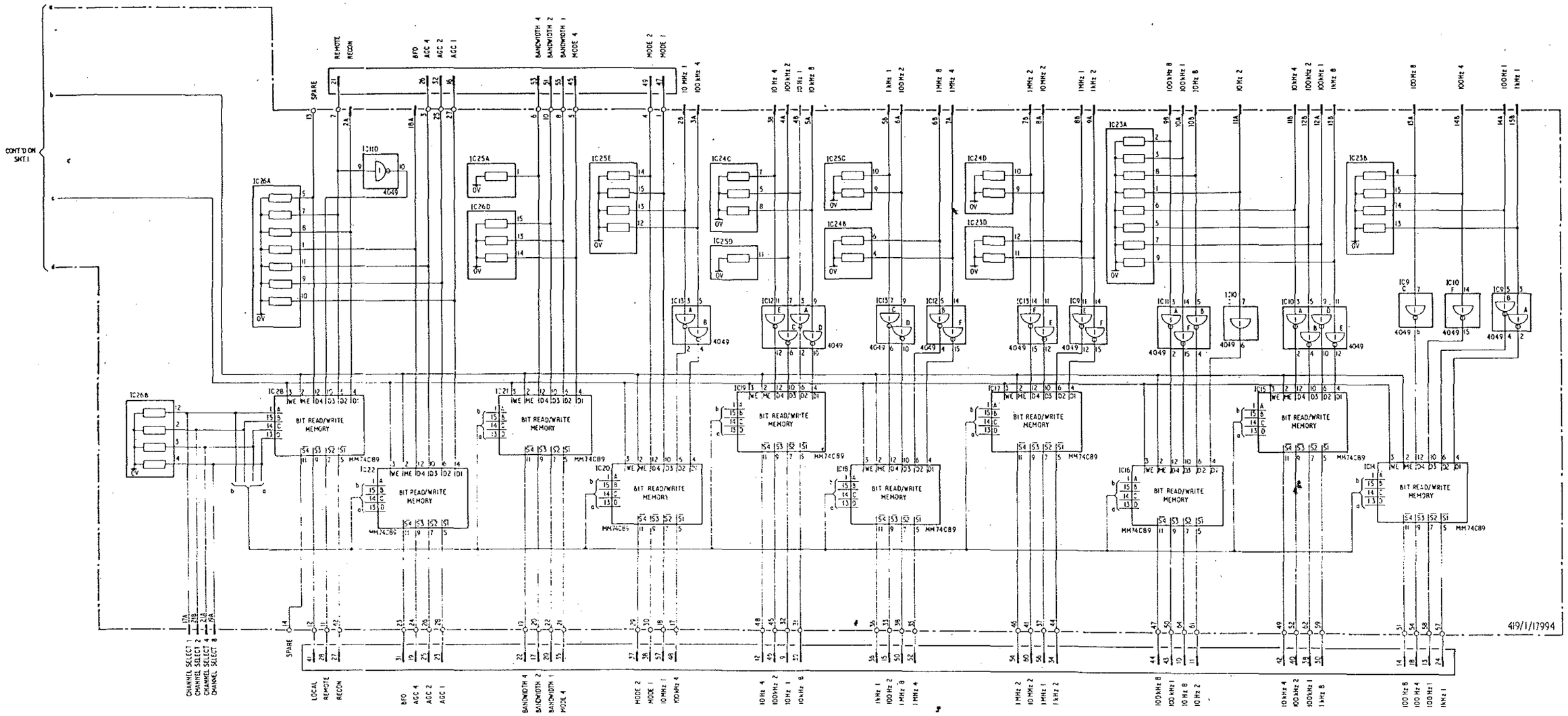
MODULE II : MEMORY CONTROL CIRCUIT DIAGRAM

FIG 2



MODULE II : MEMORY CIRCUIT DIAGRAM

FIG 1

WARNING

1. Module 12 microprocessor circuits incorporate a 'power-up' reset generator which, on application of a.c. power to the receiver, generates a 'clear' pulse input to the microprocessor.

   (i) Before removing Module 12 from a receiver, SWITCH OFF THE A.C. POWER SUPPLY.

   (ii) Before replacing Module 12 in a receiver, ENSURE THAT A.C. POWER IS OFF.

2. It is considered good practice, although not absolutely essential, to switch off a.c. power when removing or replacing any module.

CHAPTER 12

MODULE 12 - REMOTE CONTROL

CONTENTS

APPENDIX

TABLES

ILLUSTRATIONS

MODULE 12 - REMOTE CONTROL

1. INTRODUCTION

Module 12 is a microprocessor-based control module which also incorporates the memory functions of Module 11. It provides full remote control of the receiver via a serial digital data input stream. Module 12 is fitted to PR2250B, D, and F, and all PR2252 receivers. It is also fitted to PR2256 receivers.

2. MICROPROCESSORS

2.1 Introduction

2.1.1 This description assumes that the reader has no previous knowledge of microprocessors (MPUs). It is intended to give an outline of working only. Detailed description of the internal workings of a microprocessor is not needed by a maintainer, and is in any case the province of an appropriate text book.

2.1.2 A microprocessor is a general-purpose integrated-circuit device which can be used to replace a large number of TTL or CMOS logic elements which might otherwise perform a particular task. The microprocessor is 'tailored' to a particular task by means of a sequence of instructions known as a 'program'; these instructions are held in a non-volatile memory which has been programmed by the designer of the system. It is quite possible for the same type of microprocessor to perform the functions of a pocket calculator, a traffic light controller, or a 'TV Tennis' game: what the device does is decided by the program stored in the memory associated with it. Normally, all the available MPU facilities are not used in any one application: for example, as a traffic light controller a short and simple program would suffice, whereas as a calculator a more complex program using more of the MPU facilities would be necessary.

2.1.3 The focal point of any system is the MPU itself. It controls the system by reading instructions from the memory, interpreting them, and manipulating the system buses so as to carry out the orders of the human programmer. The device has no 'mind of its own': it cannot assess the wisdom or otherwise of the instructions to which it works.

2.2 Microprocessor Action

2.2.1 A basic microprocessor (MPU) system can be seen in Figure (a). The system splits into four functions,

(1) The microprocessor itself, which is capable of performing aritmetic and logic manipulation of data fed into it. This is done under the control control of a sequence of program instructions.

(2) The program store, which in its simplest form is a 'programmable read-only memory' (PROM). This store holds a fixed set of instructions which control the actions of the MPU.

(3) The data store, which consists of a random access 'read-write' memory (RAM). This store is used for holding input data, output data, and intermediate results.

(4) The input-output channels (or 'ports'). These are binary channels which transfer data in the form of parallel words. An eight-bit channel, for example, could represent 0-255 binary, 0-99BCD, the

settings of eight independent switches, or the segment pattern to display a number on a 7-segment LED display. Equally, it could supply logic level control commands to another circuit.

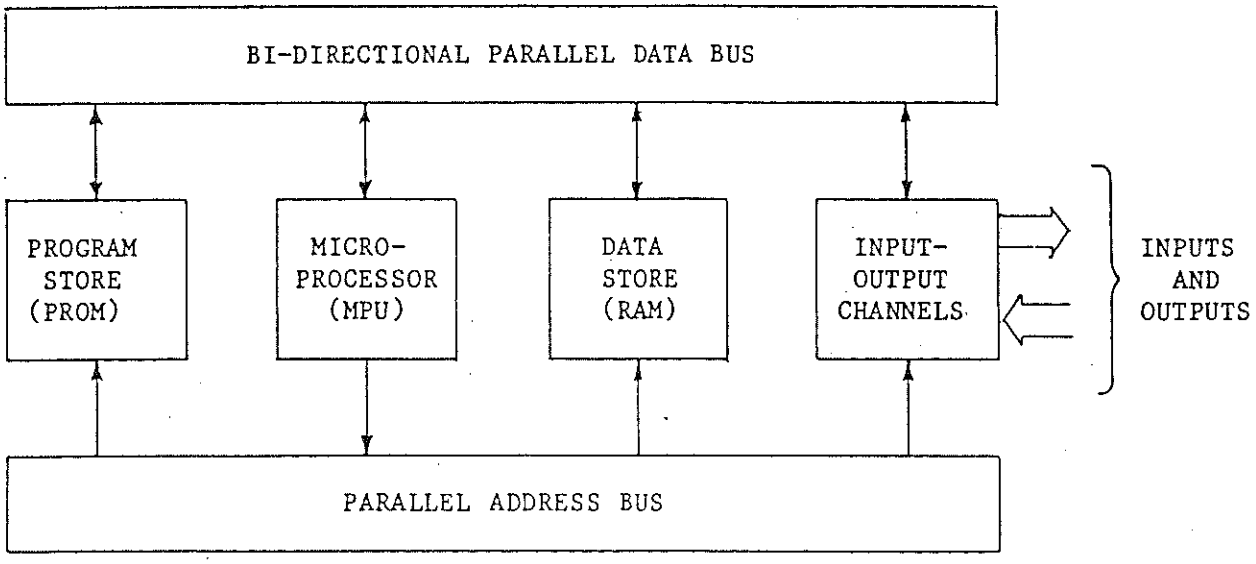


FIG (a) BASIC MICROPROCESSOR SYSTEM

2.2.2 The action can be seen in outline from the following simple example in which the MPU is assumed to handle only one bit at a time, and is required to perform the logic operation $\overline{(A.B) + C}$. This operation could be performed by gates connected as shown in Figure (b).

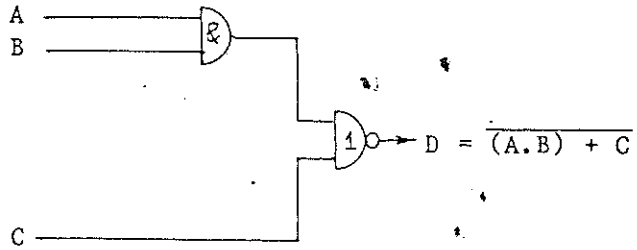


FIG (b) GATE LOGIC FOR $\overline{(A.B) + C}$

2.2.3 To carry out $\overline{(A.B) + C}$, a nine-step program would be necessary, as shown in Table 1.

TABLE 1 : PROGRAM FOR $\overline{(A.B) + C}$

STEP	ABBREV. INST.	ACTION	RESULT
1	RD0	Read data at input channel '0' (i.e. 'A')	
2	ST	Store RD0 data in data store	A
3	RD1	Read data at input channel '1' (i.e. 'B')	
4	AND	Perform AND function on ST and RD1 data	
5	ST	Store result of step 4	(A.B)
6	RD2	Read data at input channel '2' (i.e. 'C')	
7	OR	Perform OR function on ST and RD2 data	(A.B) + C
8	COMP	Form complement of step 7 result	$\overline{(A.B) + C}$
9	WRI	Present result of step 8 on output channel 1	$\overline{(A.B) + C}$

2.2.4 The nine-step sequence of instructions defined in Table 1 is stored in the PROM, and is available for use at any time. It is called up for use by an internal program in the MPU. A microprocessor has to read the PROM instructions in the absence of specific external commands, and therefore has its own internal program through which it continuously cycles: this program, called the FETCH-EXECUTE cycle, causes the MPU to read the PROM program and carry out its instructions in an orderly manner. The FETCH-EXECUTE cycle is carried out at least once for each instruction in the PROM programme; the phrase 'at least once' is used because most PROM programs include multiple-word instructions which have to be read ('fetched') from the PROM one word at a time.

2.2.5 In the example given in Table 1, it is apparent that the nine-step program would take longer to execute than the time taken to get the same result with gates. Typical times would be 20 nano-sec. for gates and 20 micro-sec. for the MPU, but the example assumed that only one bit was processed at a time. In practice up to sixteen bits are processed at once and, with a 2 MHz clock rate, it can be seen that the data-processing capability of a microprocessor is considerable.

2.2.6 Where a microprocessor is required to perform arithmetic calculations, the number of bits it can process at one (or 'word length') is of importance. If word length is four bits, then in one word there are $2^4 = 16$ possible combinations; the best definition possible is therefore 1/16, about 6%. If, however, word length is sixteen bits then there are $2^{16} = 65536$ possible combinations; the best definition possible is therefore $\frac{1}{65536}$, about 0.000015%. Note that it is nevertheless possible to achieve sixteen-bit accuracy with a four-bit word length by cascading four successive four-bit manipulations: the only loss is in the time taken to achieve a result.

2.3 CDP1802 Microprocessor IC

2.3.1 The RCA CDP1802 microprocessor integrated-circuit is used in Module 12. It is a sixteen-bit word general-purpose computing or control device intended for a wide variety of uses. Its basic function in Module 12 is that of a process-controller. In addition to the features described in the preceding text, a CDP1802 contains an array of sixteen 'scratch-pad' registers for temporary internal storage of data. The content of any one of these registers can be directed on to any one of three paths, namely:

(1) To the external memory (RAM) via the data bus. May be used to address a memory location via the address bus.

(2) To an internal register associated with the internal arithmetic logic unit.

(3) To an increment-decrement circuit where the content of a register can be incremented or decremented by 1 and then returned to the register from whence it came.

These three paths, depending on the nature of the instruction, may operate independently or in various combinations.

2.3.2 Instructions from the associated PROM to the CDP1802 consist of two 8-clockpulse cycles which together form a FETCH-EXECUTE cycle. If necessary, a third 8-clockpulse cycle can be employed in the form of a second EXECUTE cycle.

2.3.3 The operations which CDP1802 microprocessor can carry out are listed in Table 2.

TABLE 2 : CDP1802 OPERATIONS

TYPE	OPERATION
Register	Increment content Decrement content
Logic	OR Exclusive OR AND Shift right or left Shift right or left with carry
Arithmetic	Add Add with carry Subtract Subtract with borrow

2.3.4 As used in Module 12, the CDP1802 connections listed in Table 3 are employed. Each is defined in the table.

TABLE 3 : CDP1802 CONNECTIONS

TITLE	PIN	DESCRIPTION
CLOCK	1	Input for externally-generated single-phase clock.
$\overline{\text{CLEAR}}$	3	With pin 3 at '0' the device resets. With pin 3 at '1' the device runs. Used to produce correct start state on applying power.
BUS0 BUS1 BUS2 BUS3 BUS4 BUS5 BUS6 BUS7	15 14 13 12 11 10 9 8	8-bit bi-directional data bus lines. Used to transfer data between the memory, the microprocessor, and the input-output devices.
N0 N1 N2	19 18 17	Issued by an input-output instruction to signal the input-output control logic of a data transfer between memory and input-output ports. Can be used to issue command codes to the input-output ports (this is used in Module 12).
$\overline{\text{EF1}}$ $\overline{\text{EF2}}$ $\overline{\text{EF3}}$ $\overline{\text{EF4}}$	24 23 22 21	Levels which enable the input-output controllers to transfer status information to the processor. As 'flags', they can be used by input-output ports to 'call the attention' of the microprocessor.
TPA TPB	34 33	Positive timing pulses occurring every FETCH-EXECUTE cycle. TPB follows TPA. Used to interpret codes and to time inter-action with the data bus.

TABLE 3 (Cont'd)

TITLE	PIN	DESCRIPTION
MA0 MA1 MA2 MA3 MA4 MA5 MA6 MA7	32 31 30 29 28 27 26 25	8 memory-address lines. Those bits required by the memory system are strobed into external address latches by timing-pulse TPA.
$\overline{\text{MWR}}$	35	Write pulse. A negative pulse appearing in a 'memory-write' cycle after the address lines have stabilised.
Q	4	A single-bit output which can be set or reset under program control. Used as a serial data output in Module 12.
$\overline{\text{INTER-}}$ $\overline{\text{RUPT}}$	36	A software-maskable input used to interrupt the current program and switch to another. Use in Module 12 to initiate storing of front-panel settings when power fails.

3. FUNCTIONAL DESCRIPTION

3.1 General

This description is intended to be read in conjunction with the functional block diagram shown in Figure (c). It is necessary to realise that, while knowledge of the working of the circuit is valuable, the ability of a maintainer to diagnose faults to component level is very limited in Module 12. While 'peripheral' faults can be dealt with in the normal manner, faulty operation of the microprocessor controlled part of the circuit is another matter. To diagnose faults in this area, it is necessary to employ a suitably programmed computer which can be plugged into the appropriate socket in place of the microprocessor integrated circuit in order to 'talk' to the remainder of the circuit. If such equipment is not available, faults in this area are best dealt with by returning Module 12 to the manufacturer for repair.

3.2 Action

3.2.1 Module 12 operates the receiver controls under the command of externally generated data supplied to the EF input of the microprocessor (MPU). This data is in the form of serial code, and is supplied by a remote control position. This control position may be some form of computer-based automatic equipment or may be a manually controlled panel. For the purpose of this explanation a manually controlled panel is assumed.

3.2.2 One control panel may well serve to control a number of receivers. The control inputs to all receivers will be paralleled on to the same data bus. The data output from the control position will therefore be applied simultaneously to all controlled receivers but, as it contains an 'address' specific to a particular receiver, only one receiver will respond.

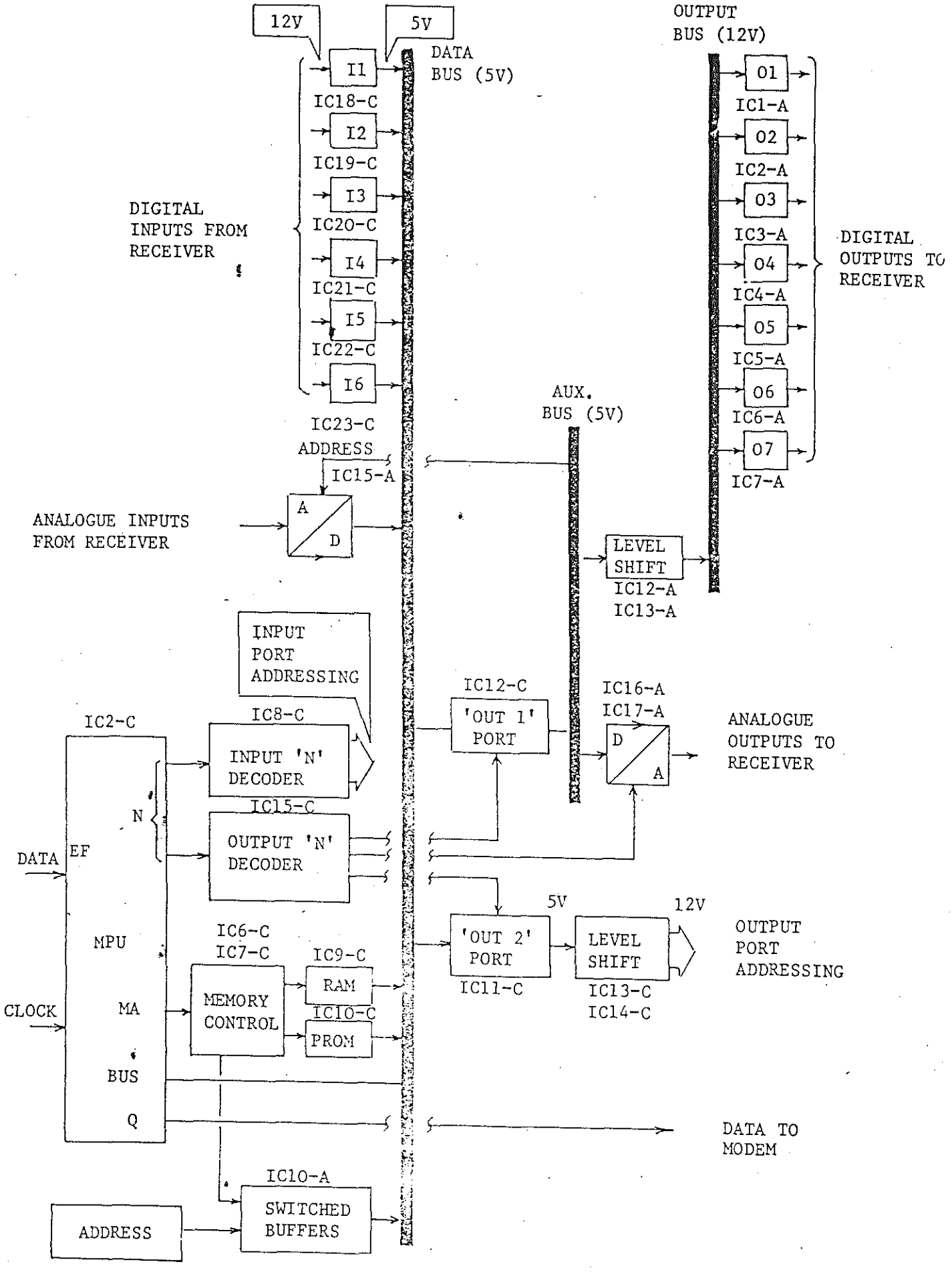


FIG (c) Module 12 Mk II Functional Block Diagram

It would in fact be possible, if required, to organise matters so that a number of receivers responded simultaneously: however, this text assumes that only one is required to respond at any one time.

3.2.3 Module 12 'talks' to the receiver via six input ports, seven output ports, an analogue-digital converter, and two digital-analogue converters. The general logic circuitry of the receiver works on +12V/0V levels, while the MPU and associated circuitry employs +5V/0V levels; consequently the input and output ports must also (either internally or in conjunction with other devices) perform level-changing functions. Each port and converter can be separately addressed by the MPU via the 'N' Decoders; the input ports are directly addressed by one 'N' Decoder, while the output ports are addressed via the internal 'Out 2' port and a 5V/12V level shifter.

3.2.4 A three-bus system is employed to transfer data. The input ports and the MPU (together with the associated PROM and RAM) connect directly to the 5V Data Bus. The Data Bus communicates with the 5V Auxiliary Bus via an internal port designated 'Out 1'. The Auxiliary Bus is directly connected to the 12V Output Bus via a 5V/12V level shifter. Operations on the Data Bus occur at MPU clock rate, but it is not always possible or desirable to tie output port actions to the MPU clock rate: therefore, the 'Out 1' and 'Out 2' internal ports (which include stores) accept data at MPU clock rate and present it at their outputs independent of clock rate. This allows the output port addressing and data transfer to be independent of the MPU clock.

3.2.5 Module 12 must, in addition to commanding the receiver, produce a continuous 'status report' of the receiver control settings for use at the remote control position. If, for example, the operator changed the MODE setting, it is not sufficient that he has an indication that he has done so; he must also have a positive indication that the receiver has in fact responded correctly. Commands to the receiver are issued via Module 12 output ports, and the status of the receiver controls is monitored via Module 12 input ports. The receiver control status data is fed back to the remote control position in serial form from the Q output of the MPU.

3.2.6 A locally-controlled receiver stores its current control settings automatically in channel '0' of its Module 11 memory, and can store fifteen further sets of control positions in the fifteen selectable Module 11 memory channels. Module 12 provides the same facility in a remotely controlled receiver by employing part of the RAM to carry out the necessary memory functions. As with Module 11, setting storage is automatic if a receiver power failure occurs.

3.2.7 The actions of the system are best seen by following through the affects of a command, from its generation by the remote control position to the application of a 'status report' by Module 12 to the remote operator's panel. The sequence of actions is essentially the same for any command.

3.2.8 To change a control setting on a particular receiver, the remote operator will first operate some form of 'select receiver' control and then make the appropriate setting on his control panel. Temporarily, his control panel has in effect become the front panel of the controlled receiver. These actions will produce a serial data output to the bus connecting the EF inputs of all receivers in parallel.

3.2.9 On receiving a data input, the MPUs of all receivers will examine it and ascertain if it contains their address. If it does not, they ignore it:

the one which finds that it corresponds to its 'wired-in' address reacts. From here on, we will consider the actions which take place in the addressed receiver.

3.2.10 The MPU checks the address in the data input against its wired-in address by closing the circuit of the switched buffer for just long enough to read the wired-in address. This is always the first action on receiving an EF data input.

3.2.11 The serial data applied to the EF input of the MPU causes the MPU to call up the relevant program from the PROM via the MA output. Under instructions from the program, the MPU generates suitable output commands for application to the receiver and, via the BUS output, applies them to the Data Bus. It also generates an 'N' output to the output 'N' Decoder, which produces separate sequential port addresses to both 'Out 1' and 'Out 2' internal ports. The 'Out 1' port now transfers the output commands to the Auxiliary Bus from where, via the level shifter,they appear on the output bus. The 'Out 2' port then addresses the relevant output port, so allowing the commands to reach the appropriate receiver circuits.

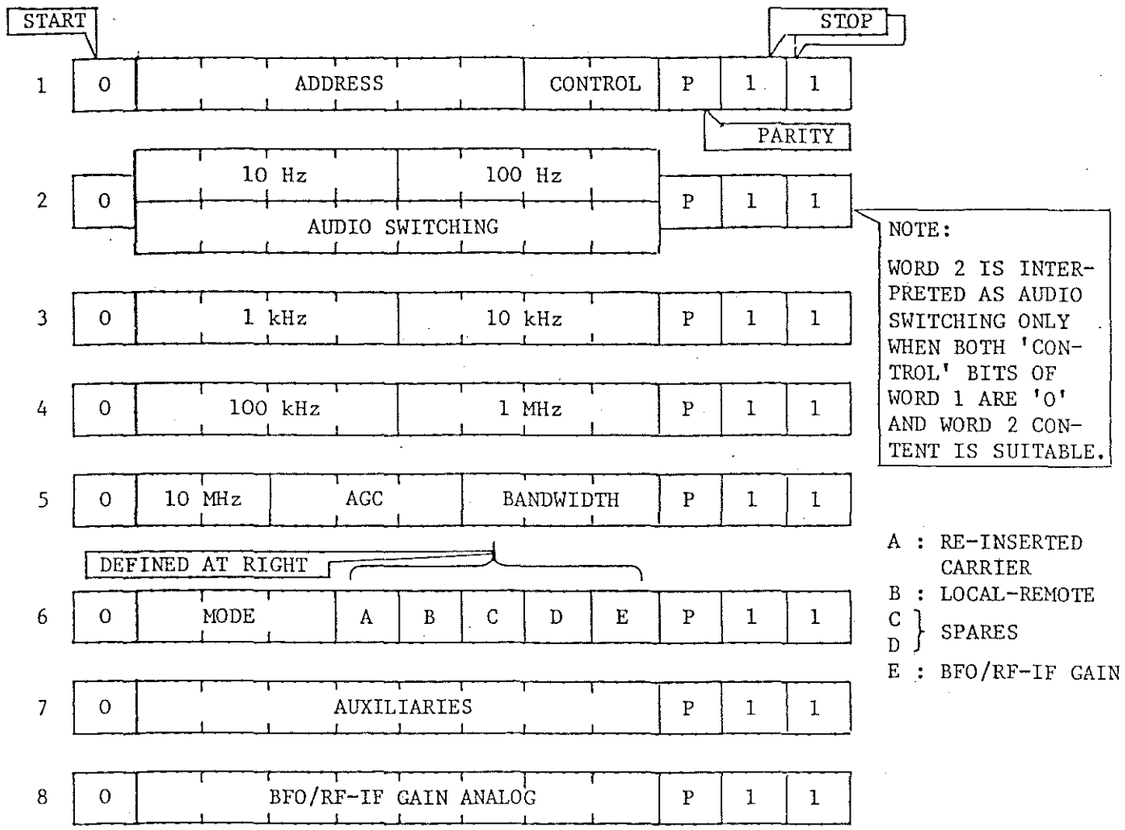
3.2.12 When the receiver has responded to the command, the MPU addresses the input ports, and a complete receiver control 'status report' is fed on to the data bus. The MPU stores this data in part of the RAM, and also processes it into serial form. The storage in the RAM is 'Channel 0' memory dump storage from the operator's standpoint. The serial data appears at the Q output of the MPU, and is fed back to the remote control position to indicate on the operator's panel that the receiver has in fact responded to his command.

3.2.13 On completion of this cycle the MPU has come to the end of the PROM program to which it was working; it then resets the whole system into the quiescent state in which it rested before it receiver the initial data input.

3.2.14 The description in paragraphs 3.2.7 to 3.2.13 assumes that the sequence of actions is essentially the same for any command. This is true, but not exact in respect of the operation of the analogue RF GAIN and BFO controls via the D-A converters: no feedback data from Module 12 is provided for these two controls, as the audible result of their operation at the remote control position is in itself adequate evidence that the receiver has responded to the control movement. Similarly, the ZERO BEAT and RF METER remote monitoring via the A-D converter only involves the use of an input as it is essentially a 'one-way' operation.

3.2.15 Module 12 uses the RAM associated with the MPU to provide a 16-channel memory system identical with that of Module 11. However, when working with remote control, only the 'Channel 0 Dump' memory facility is available in a limited fashion; settings are automatically stored if power fails, and restored on re-application of power. It is expected that the remote-control equipment will contain such memory facilities as may be considered necessary. When a Module 12 equipped receiver is working in local control (i.e. from its own front panel) then Module 12 provides full 16-channel memory facilities: this is only applicable to PR2250 series receivers, as PR2252 series receivers do not carry full front-panel controls.

COMMAND INPUTS



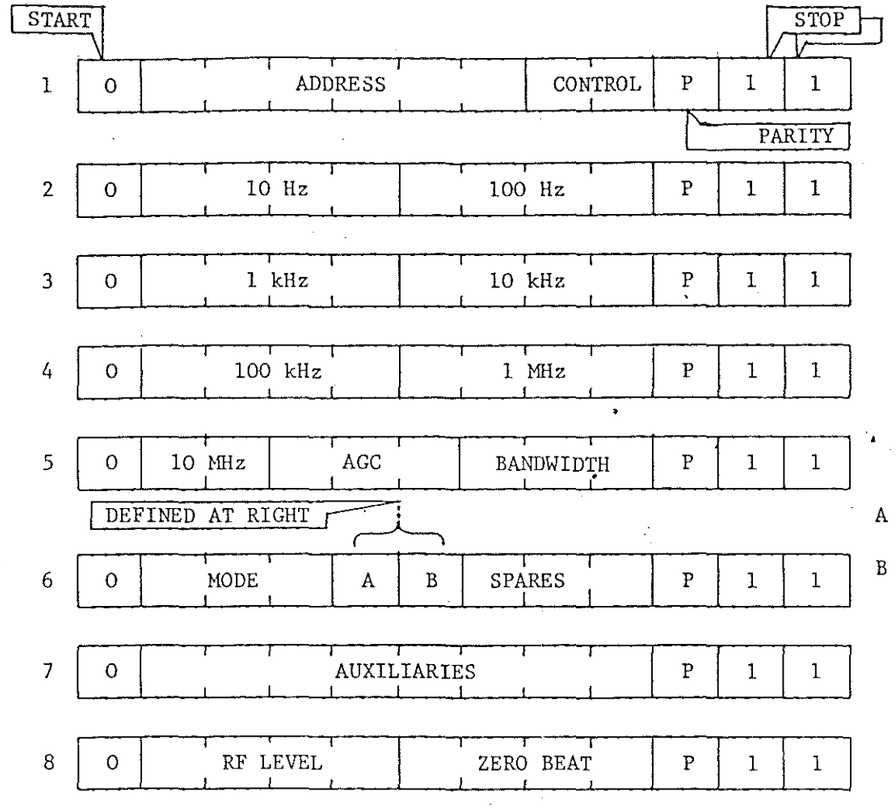
NOTE:

WORD 2 IS INTERPRETED AS AUDIO SWITCHING ONLY WHEN BOTH 'CONTROL' BITS OF WORD 1 ARE '0' AND WORD 2 CONTENT IS SUITABLE.

A : RE-INSERTED CARRIER
B : LOCAL-REMOTE
C, D } SPARES
E : BFO/RF-IF GAIN

NOTE: EACH BLOCK OF DATA IS TRANSMITTED LSB FIRST

STATUS REPORT OUTPUTS



A : RE-INSERTED CARRIER
B : LOCAL-REMOTE

NOTE: EACH BLOCK OF DATA IS TRANSMITTED LSB FIRST

START BITS	: '0'
PARITY BITS	: '0' OR '1' TO MAKE THE TOTAL NUMBER OF '1' BITS IN THE WORD AN ODD NUMBER.
STOP BITS	: '1'
ADDRESS	: RECEIVER ADDRESS IN HEXADECIMAL.
CONTROL (COMMAND INPUT)	: 0-0, WORDS 1 & 2 ONLY, AND INTERPRET WORD 2 AS AUDIO SWITCHING IF SUITABLE. 1-0, WORDS 1, 2 & 3 ONLY. 0-1, ALL WORDS. 1-1, METER READING ONLY.
CONTROL (STATUS REPORT OUTPUT)	: 0-1, ALL WORDS 1-1, WORDS 1 & 8 ONLY.
FREQUENCY BLOCKS	: FREQUENCY VALUES IN B.C.D.
AGC	: 0-1-1, OFF 1-0-1, SHORT 0-0-1, MED 1-1-0, LONG
BANDWIDTH	: 0-1-1, 8 kHz 1-0-1, 6 kHz 0-0-1, 1.2 kHz 1-1-0, 300 Hz 0-1-0, 100 Hz
MODE	: 0-1-1, AM 1-0-1, CW 0-0-1, USB 1-0-0, LSB 0-1-0, ISB 0-0-0, F
RE-INSERTED CARRIER	: 1, BFO 0, RECON. CAR.
LOCAL-REMOTE	: 1, LOCAL 0, REMOTE
BFO/RF-IF GAIN	: 1, BFO 0, RF-IF GAIN
AUXILIARIES	: EACH BIT DEDICATED TO ONE OUTPUT. 0 = O/P LOW, 1 = O/P HIGH
BFO/RF-IF GAIN ANALOG	: TRUE BINARY VALUE

RF LEVEL (S/R OUTPUT) : TRUE BINARY
ZERO BEAT (S/R OUTPUT) : TRUE BINARY
AUDIO SWITCHING (CMD. INPUT) :

1	2	3	4	5	6	7	8	
AUDIO LINE ADDRESS				0	0	1	1	AUDIO LINE ON & REVERT
NOT USED				0	1	0	1	
				TO				
				1	1	1	1	AUDIO LINE OFF & REVERT
				EXCLUDING				
				0	0	1	1	

3.3 Data Format

3.3.1 A serial data format is employed for both the commands from the remote-control position and for the 'status report' output to the remote-control position. Each word (or byte) consists of 12 bits: the first is a start bit, the second to ninth carry data, and the tenth is a parity bit. The eleventh and twelfth bits are stop bits.

3.3.2 The input data is applied from the remote-control position to the EF input of the MPU. The status report data is applied by the Q output from the MPU to the remote-control position. Both lines stand at a '1' level when not transmitting data.

3.3.3 The detailed format can be seen in Figure (d). Word 1 is always transmitted in both command and status report data, as it contains the address and two 'control' bits: these two control bits define the length of the 'sentence' to be transmitted. The command sentence can be word 1 alone, words 1 and 2, words 1, 2 and 3, or all seven words. The status report sentence is either all seven words, or words 1 and 7.

3.3.4 When the two control bits of Command Input Word No.1 are both '0', the content of Command Input Word No.2 can be interpreted either as frequency data or as audio switching commands, depending upon its content. To represent frequencies, bits 1 to 8 of Word 2 must consist of two successive 4-bit BCD numbers each of which is 9 or less. Should bits 5 to 8 form a BCD number greater than 9, Word 2 is interpreted as audio switching commands in the format given in Fig.(d).

3.3.5 The various possible combinations of command and status report are listed below in Table 4.

TABLE 4 : COMMAND AND STATUS REPORT COMBINATIONS

COMMAND SENT		STATUS REPORT PRODUCED	
WORDS	DATA CONTENT	WORDS	DATA CONTENT
1	Address Send meter reading	1 and 7	Address Meter reading
1 and 2	Address 10Hz and 100Hz frequency	NONE	
1, 2 and 3	Address 10Hz, 100Hz, 1kHz and 10kHz freq.	NONE	
1 to 7	Address All commands	1 to 7	Address Full report

3.3.6 When all seven command words are transmitted to the receiver, this does not necessarily imply that every command will change a receiver control. It is necessary to send all seven words to change any one of the receiver controls except the 10Hz, 100Hz, 1kHz and 10kHz frequency settings. If a control has not been changed since the last transmission of command data, then the data for that control is sent unchanged.

3.3.7 The input command data voltage levels applied to Module 12 are fed to the MPU EF input via a buffer circuit, and may be any voltage between '0' = +3V, '1' = 0V and '0' = +30V, '1' = -30V. The voltages which represent '1' and '0' need not be equal. The output status report levels are fed out from the Q output of the MPU via a level-changing buffer circuit which requires the application of a negative d.c. supply from an external source. This voltage is -12V maximum, but can be of any desired value between 0V and -12V. If the negative d.c. supply level is -xV, then the output levels are '0' = +12V, '1' = -xV, i.e. '0' is always +12V, but '1' may be any value between 0V and -12V.

3.3.8 It is expected that Module 12 will normally be worked at a data rate of either 600, 1200 2400, or 4800 bauds. If required, it is capable of working at any data rate up to 4800 bauds.

3.3.9 Eight miniature rocker switches contained in a single IC package are mounted on a small p.e.c. (shown as panel 419/DA/18053 on Fig.2), and are accessible on the upper outer surface of the module. These switches set sync. selection, parity and baud rate by applying logic levels (in conjunction with the pull-up resistors of IC24-C) to input port IC17-C. The switches are numbered 1 to 8, switch 1 being the rearward item. Switch settings are as tabulated below and labelled on the module case.

0 = OFF, GIVING '1' OUTPUT

● = ON, GIVING '0' OUTPUT

SWITCH					
1	2	3	4	5	6
0	0	0	0	0	
NO PARITY	EVEN PARITY	INT. SYNC	600 BD		0 NORMAL
			0	●	
			1200 BD		
●	●	●	●	0	●
			2400 BD		
PARITY	ODD PARITY	EXT. SYNC	●	●	REMOTE OVER-RIDE
			4800 BD		

3.3.10 The command data input to Module 12 and the status report data from Module 12 may be linked to the remote-control position by any suitable means, e.g. land-line, radio link, etc.

3.4 Receiver Control Outputs

The control outputs from Module 12 to the receiver proper are identical with those produced in other variants of the receiver by Module 11.

4. CIRCUIT DESCRIPTION

4.1 Introduction

4.1.1 The circuits of Module 12 can be divided into two parts, the microprocessor-controlled portion and the peripheral circuits which handle various data and control inputs and outputs. No full description of the MPU-controlled part of the circuit is given, for two reasons:

(1) As stated in paragraph 3.1, extremely specialised equipment is essential to achieve anything of value in this area.

(2) The action of this part of the circuit can be varied by the program held in the PROM.

The remainder of the circuit is described in the usual manner.

4.1.2 Module 12 circuits are mounted on two printed-circuit panels, the 'CPU Panel' (419/1/18063) and the 'Analogue Panel' (419/1/18061). The CPU Panel is entirely occupied by MPU-controlled circuits. The Analogue Panel contains a small part of the MPU-controlled circuits, but is mainly occupied by peripheral circuits as mentioned in paragraph 4.1.1.

4.2 Input and Output Connections

4.2.1 Data interface with receiver

Module 12 is connected to the receiver via PL13 and via various printed-circuit panel edge pins which physically form an edge-connector which mates with a socket on the receiver.

4.2.2 Data to and from remote control point

The 'command' (data from modem) and 'status report' (data to modem) serial code data is applied and taken via printed-circuit panel edge pins, to pins of the CONTROL socket at the rear of the receiver as defined in Table 5.

TABLE 5 : SERIAL DATA CONNECTIONS

CONTROL SOCKET PIN NO.	FUNCTION
22	DATA TO MODEM
23	DATA FROM MODEM
24	EXTERNAL NEGATIVE SUPPLY
17	0V
25	Tx CLOCK
26	Rx CLOCK

4.2.3 Address data

The receiver address data is applied via printed-circuit panel edge pins from the CONTROL socket at the rear of the receiver as defined in Table 6. A pin connected to 0V gives logic '0'; a pin left open-circuit gives logic '1'.

TABLE 6: ADDRESS DATA CONNECTIONS

CONTROL SOCKET PIN NO.	BINARY VALUE	CONTROL SOCKET PIN NO.	BINARY VALUE
27	1	30	8
28	2	31	16
29	4	32	32

4.3 MPU - Controlled Circuit

4.3.1 The circuitry is physically located on two printed-circuit panels, the 'CPU Panel' and the 'Analogue Panel'. It is necessary to largely ignore this physical boundary in the interests of coherent circuit description; for example, one sentence may well refer to items on both panels. Therefore, for the purposes of this description only the various component identities have a suffix added, either C (CPU Panel) or A (Analogue Panel): IC4-C is therefore IC4 on the CPU panel, and IC4-A is therefore IC4 on the Analogue Panel. This does not apply to the identities of edge connectors or plugs.

4.3.2 The circuit is controlled by MPU IC2-C, which interfaces with a PROM (IC10-C) and a RAM (IC9-C). Memory control is exercised via decoding circuits IC6-C and IC7-C. The address data is produced by a combination of '1' levels from the resistors contained in IC11A-A and the 0V levels connected to selected Analogue Panel edge-connector pins 10B, 11A, 12A, 12B and 13A: these 0V levels are wired in to the receiver bay, as described in para.4.2.3. IC10-A is in effect a set of switched buffers which are enabled by the RX ADDRESS DISABLE output from the MPU (IC2-C) via the memory address circuits (IC6-C, IC7-C, IC16C-C).

4.3.3 Some early models of Module 12 are fitted with IC9 as a composite item of three integrated circuits in place of an RCA integrated circuit CDP1823S or D. The CDP1823S and D were not available for these early models, and type CDP1823 was employed. The CDP1823 can react unpredictably to various slow input slew states which may occur on initial application of power, and therefore has inputs applied via the Schmitt trigger elements of two further integrated circuits. The three integrated circuits which make up this version of IC9 are mounted in sockets on a small printed-circuit panel carrying a DIL plug which mates with the IC9 socket on Module 12 CPU Panel. The composite item can be seen in the circuit diagram of Fig.5, and is directly interchangeable with a CDP1823D device.

4.3.4 The Data Bus is formed by lines D0 to D7 connecting both p.c. panels. It connects directly to:

(a) The MPU (IC2-C).

(b) The PROM (IC10-C).

(c) The RAM (IC9-C).

(d) The Analogue/digital converter (IC15-A).

(e) The Address buffers (IC10-A).

(f) The six input ports (IC18-C to IC23-C).

(g) The internal 'Out 1' port (IC12-C).

(h) The internal 'Out 2' port (IC11-C).

4.3.5 The Auxiliary Bus is formed by lines D00 to D07. It connects directly to:

(a) The 'Out 1' port output.

(b) The Digital/Analogue converter inputs (IC16-A, IC17-A).

(c) Level shifter (IC12-A and IC13-A) input.

The Auxiliary bus forms an interface, via the 'Out 1' port between the Data bus and the 12V Output Bus.

4.3.6 The Output Bus is formed by the QA, QB, QC and QD outputs of level-shifter IC12-A and IC13-A. It connects directly to the inputs of the seven output ports IC1-A to IC7-A.

4.3.7 All part addressing originates from the 'N' output lines of the MPU. The data on these outputs is decoded as appropriate by either the Input 'N' decoder IC8-C or the Output 'N' decoder IC15-C. The Input 'N' decoder controls the input ports (IC17-C to IC23-C), while the Output 'N' decoder controls the internal 'Out 1' and 'Out 2' ports and the two digital/analogue converters. The input selector associated with the analogue/digital converter is addressed by an output from the 'Out 1' port, produced by MPU-supplied data via the Data Bus. The seven output ports (IC1-A to IC7-A) are also addressed by an output from the 'Out 2' port, produced by MPU-supplied data via the Data Bus. The PROM, RAM and Address Buffers are addressed directly by the MPU MA outputs via memory control decoders IC6-C and IC7-C.

4.4 MPU - Clock

The MPU is clocked by an internal oscillator circuit controlled by an externally connected 1.9968 MHz crystal between pins 1 and 39. An output is taken from this oscillator via a 'divide-by-four' circuit formed by IC3B-C and IC3A-C to produce a 499.2 kHz ADC clock output on PL1-C pin 12. Where data is applied to the MPU from a modem, the accompanying modem clock input is taken either from the output of buffer stage TR2-A or TR1-A on the Analogue Board; selection is carried out by switching gate IC18-A, the output of which is applied via inverting Schmitt trigger IC4D-C as COMMON CLOCK to the MPU.

4.5 MPU Serial Data Input

The serial code data input from the remote-control position is applied via buffer stage TR3-A on the Analogue Board. Input level limits are as defined in para.3.3.6. The output from TR3-A switches between +5V and OV and the inversion produced by TR3-A is cancelled by IC4C-C.

4.6 Serial Data Output

4.6.1 The serial data from the MPU 'Q' output (IC2-C pin 4) is applied via pin 18 of PL1 on the Analogue panel to the B (pin 10) control input of switching device IC18-A; a '0' level B input connects Y0 to Y, while a '1' level input connects Y1 to Y. A digital input to the B input switches Y between +VDD (5V) and OV, the Y output being applied to the X1 input. The X0 input is connected to the base bias voltage of transistors TR4-A and TR5-A.

4.6.2 The X0-X1 switch element is controlled by the A input, supplied by the ENABLE SDL output from OUT 2 port IC11-C. With the A input level at '0', X0 is connected to X; this sets bases and emitters of TR4-A and TR5-A to the same potential, thus rendering them non-conducting. With the A input level at '1', X1 is connected to X and the MPU 'Q' input appears (via R31) on the emitters of TR4-A and TR5-A.

4.6.3 TR4-A and TR5-A drive TR7-A and TR6-A. TR6-A emitter is returned to whatever externally applied voltage is applied to Analogue panel edge pin 14B; this voltage may be of any desired value between -12V and 0V. A positive level (approx. +5V) on R31-A renders TR6-A conducting, and a 0V level on R31-A renders TR7-A conducting: The SERIAL DATA output from Analogue panel edge pin 15B is therefore either connected to +9/12V or to 0V according to the logic level on the X output of IC18-A.

4.6.4 When IC18-A connects X0 to X, under the control of ENABLE SDL, all four output stage transistors are non-conducting and SERIAL DATA OUTPUT takes up a 'tristate' high impedance state. The output stage is supplied by the 9/12V power line, which is 9V when the receiver is in STANDBY and is 12V when the receiver is in OPERATE: in either state, RLA is energised but, should a.c. power fail, RLA de-energises and open-circuits the SERIAL DATA output line.

4.7 AGC/ZERO BEAT Analogue/Digital Converter

4.7.1 The analogue 'A.G.C.' and 'ZERO BEAT' receiver monitor inputs are applied to converter IC15-A; a third 'Analogue Auxiliary' input line is also applied. All three inputs may be continuously present, but only the one selected by levels applied by the D0, D1, and D2 lines of the Auxiliary Bus appears as an input to the A-D converter part of the device. Successive A/D conversions occur as demanded by the remote control equipment, typically at about ten per second; the ADC CLOCK frequency is not related to the sample rate. The digital outputs are in parallel 8-bit binary form, 0V being represented by binary 0 and +5V being represented by binary 255 ('all 1s'). The device is linear in its response to input voltage; e.g. if binary 0 is 0V and binary 255 is +5V, then +2.5V is represented by binary 127.

4.7.2 The ZERO BEAT input signal is applied via a 5 Hz low-pass active filter formed by IC14D-A and associated components: an explanation of active filters can be found in Chapter 5 of Section 4 of this publication. This filter is incorporated to ensure that the cyclic variations of the analogue input concerned cannot reach the converter at frequencies which can cause false indications; these frequencies are those where the period of the input signal variation is near that of the converter sampling intervals. At such frequencies, the converter can produce an output varying at a much lower rate than the input signal variations.

4.7.3 The two un-filtered analogue inputs are fed via potentiometer chains in order that adjustment may be made to bring the maximum positive value of the input signal to a voltage equal to the reference potential applied to pin 12 of IC15-A.

4.8 REMOTE RF/IF GAIN and REMOTE BFO Digital/Analogue Converters

4.8.1 Two counters are used, one for RF/IF GAIN and one for BFO. They differ only in respect of the circuits employed to process the converter outputs. Each converter (IC16-A and IC17-A) receives an 8-bit binary input from the Auxiliary bus, representing an analogue d.c. level; 'all '0'' represents 0V, while 'all '1'' represents a voltage equal to the +2.5V reference potential at pin 6. A control input, $\overline{EN}$, is applied to each; when at '0', data is entered to 8 internal latches. When $\overline{EN}$ level becomes '1', the latches retain the data. An output d.c. level is produced on pin 5 which is proportional to the binary value of the applied input. Successive sampling, controlled by $\overline{EN}$, is necessary to produce a varying output: sample rate is controlled by the N outputs from the MPU.

4.8.2 The analogue output from IC16-A is fed via voltage-follower output buffer IC14-A. Any variation of output voltage due to loading, etc, is corrected by the feedback circuit. Capacitor C11-A removes any digital input 'spikes' which appear on the analogue output.

4.8.3 The analogue output from IC17-A is fed via a similar voltage follower output circuit. In this case an offset is produced by R24-A and R25-A, i.e. a 0V output is applied to IC14B-A as $\frac{33}{56x33} \times VR$ volts. So long as the voltage at IC14B-A output remains below 5.8V, diode D5-A is reverse-biased and the presence of IC14C-A has no effect; IC14B-A gain is fixed by R28-A, R29-A and R30-A. When IC14B-A output voltage exceeds 5.8V (as set by R26-A), the level on the inverting input of IC14C-A causes D5-A to conduct; R27-A is then effectively in parallel with R28-A, changing IC14B-A gain. The output characteristic produced is as shown in Fig.(e), matching the non-linearity of the BFO input circuits.

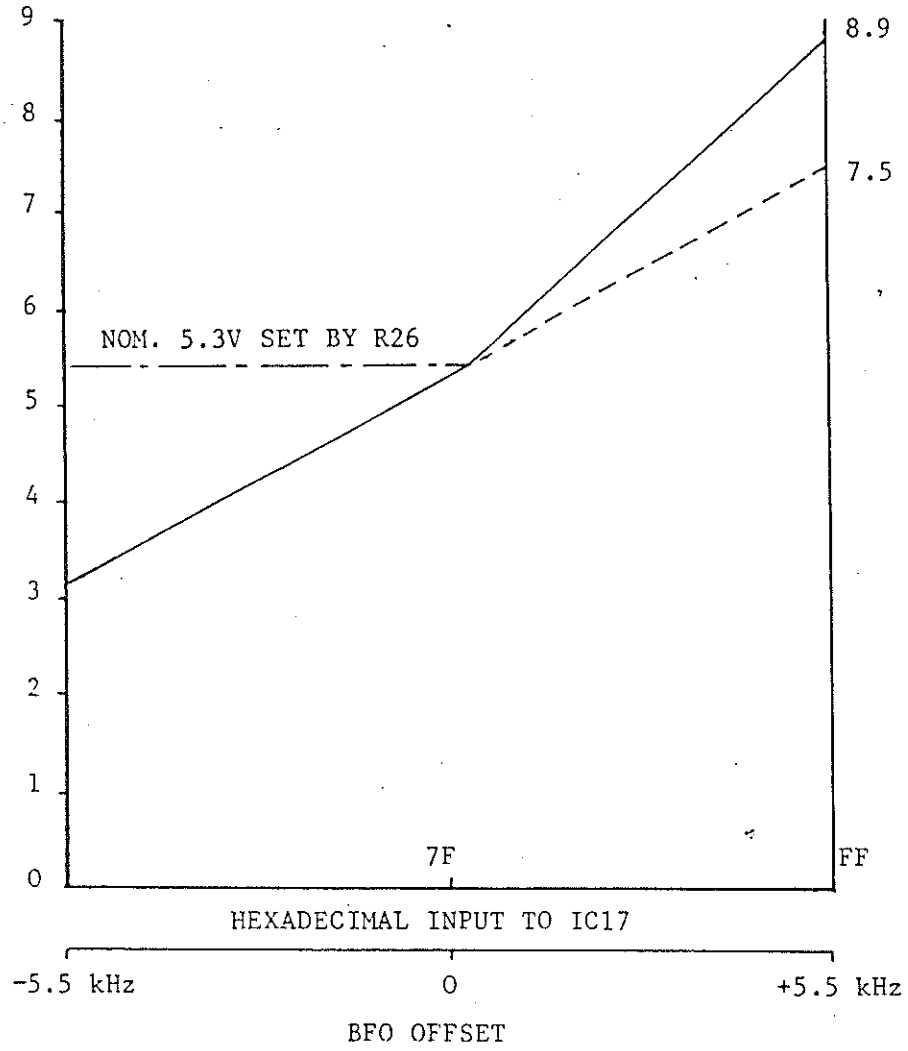


Fig.(e) IC14B-A Output Circuit Characteristic

4.9 Power State Sensor

4.9.1 Should the receiver be switched from OPERATE to STANDBY or should it experience an a.c. power failure when switched to OPERATE, the MPU stores the current front-panel control settings in part of the RAM. On switching from STANDBY to OPERATE, or on restoration of a.c. power after a failure when switched to OPERATE, the MPU restores the original front-panel settings. The a.c. power state is sensed by TR2-C and associated

components and, if a.c. power is lost, the RAM is powered by a battery until power is restored.

4.9.2 The 5V RAM power is normally supplied from the output of regulator IC1-C via hot carrier diode D2-C. The 4.5V battery normally charges from the +9/12V line via R1-C and D1-C; under these conditions D3-C is reverse-biased by about 0.5V. Should a.c. power fail, the +9/12V supply drops to 0V; the battery is then the only available power source, and supplies the RAM via D3-C and R2-C in parallel. The presence of R2-C minimises voltage drop between the positive terminal of the battery and the RAM; current in the quiescent RAM state is in the order of 10 uA.

4.9.3 Switching the receiver from OPERATE to STANDBY or vice-versa is sensed by the MPU $\overline{EF1}$ input from IC5A-C. An a.c. power failure is sensed by TR2-C and associated components: in such a failure, the power unit reservoir capacitors ensure that the supply voltages fall relatively slowly. The +5V VDD potential is produced by regulator IC1-C, and will remain unchanged until the +9/12V line drops significantly below +9V. As the emitter of TR2-C is returned to VDD, in a failure situation the base potential will drop significantly towards 0V before the collector/emitter potential drops. Therefore in an a.c. power failure TR2-C will conduct and produce via IC4B-C a '1-0' step input to the $\overline{INT}$ input of the MPU; this step will activate the 'interrupt' sub-routine and cause storage of the current front-panel settings before the VDD output of regulator IC1-C falls significantly. At the same time as IC4B-C output level drops from '1' to '0', IC4A-C output level also drops from '1' to '0'.

4.9.4 On initial application of power the output from IC4A-C is at '0'; about 100 mS later, it rises to '1'. On removal of a.c. power, the output from IC4A-C drops to '0' as soon as the +9/12V line level drops significantly. The '0' level from IC4A-C during power-up and power-down acts as a reset with wide reaching effects. The MPU (IC2-C), the Out 1 port (IC12-C), the Out 2 port (IC11-C), and level-changer IC13-C are all directly cleared. The RAM (IC9-C) is inhibited via its CS4 input. Clearing the Out 1 port clears the Auxiliary Bus and Out- put Bus lines to '0'. Clearing the outputs of IC13-C to high impedance produces an effective 'all '1' set of outputs due to R13-C, R14-C, R15-C and R16-C; these '1' levels clear output ports 6 and 7 to 'all '0' by strobing in the '0' outputs of the Out 1 port (IC12-C).

5. TEST DATA

5.1 Test Equipment Required

Module 12 can only be tested to a limited extent, and then only in a remotely-controlled receiver with the co-operation of the remote-control operator and his equipment: in this context, the remote-control equipment is assumed to be a Plessey PR2260 in correct working order within the manufacturer's test specification tolerances in all respects. The following test equipment is required:

(1) An oscilloscope capable of displaying a 2 MHz square-wave signal of 12V peak-to-peak amplitude.

(2) A high impedance input d.c. voltmeter capable of reading up to +12V with an accuracy of at least $\pm$ 10 mV.

5.2 Alignment and Functional Tests

5.2.1 MPU clock waveform

Carry out the following procedure:

(1) Connect Module 12 to the receiver by the extenders provided in the servicing kit.

(2) Set the receiver STANDBY-OPERATE switch to OPERATE.

(3) Connect the oscilloscope between pin 1 of IC2 on the CPU panel and 0V. Observe the displayed waveform. Check that a sine wave of approx.4V peak-to-peak amplitude is displayed.

5.2.2 Output setting of D/A converters (Analogue Panel)

This procedure is only required after a D/A converter IC (either IC16 or IC17 on the Analogue Panel) has been replaced by a new item. It is not required in any other circumstances.

(1) Connect Module 12 to the receiver by the extenders provided in the servicing kit. Viewing the module from the front, remove the right-hand side panel and the CPU panel behind it to allow access to the preset controls. Allow the CPU panel to rest flat on the bench while connected to the Analogue panel by the flat flexible connector cable.

(2) Set the receiver STANDBY/OPERATE switch to OPERATE and, on PR2250 receivers only, set the receiver to remote control.

(3) Request the remote control operator tc take control of the receiver concerned, and to set his PR2260 controls as follows:

AGC : OFF
BFO : Fully clockwise
RF/IF GAIN : Fully anticlockwise

(This produces an 'all 1s' situation on the Module 12 Aux. bus lines).

(4) Set R26 on Module 12 Analogue panel to max., i.e. slider furthest from 0V.

(5) Connect the voltmeter between IC14 pin 7 and 0V.

(6) Set R30 to produce a voltmeter reading of +7.5V.

(7) Adjust R26 to produce a voltmeter reading of +8.9V.

(8) Connect the voltmeter between IC14 pin 1 and 0V.

(9) Adjust R41 to produce a voltmeter reading of +9V.

(10) Disconnect all test equipment and re-assemble Module 12.

5.2.3 A/D converter input settings

This procedure is only required if the voltage regulator (IC1 on the CPU panel) has been replaced by a new item, as such a replacement can (due to

IC manufacturer's tolerances) produce a change in reference potential to the converters of up to 0.25V.

(1) Connect Module 12 to the receiver by the extenders provided in the servicing kit. Viewing the module from the front, remove the right-hand side panel and the CPU panel behind it to allow access to the preset controls. Allow the CPU panel to rest flat on the bench while connected to the Analogue panel by the flat flexible connector cable.

(2) Set the receiver STANDBY/OPERATE switch to OPERATE and, on PR2250 receivers only, set the receiver to remote control.

(3) Connect the voltmeter between pin 5A of Module 12 Analogue panel and 0V.

(4) Request the remote-control operator to take control of the receiver concerned, and to set his PR2260 controls as follows:

AGC	: OFF
RF/IF GAIN	: to produce a voltmeter reading of 8V between pin 5A of Module 12 Analogue panel and 0V
METER	: RF

(5) Set R2 on Module 12 Analogue panel to produce a PR2260 RF meter reading of 80 dBm.

Note that, except in special applications, the circuit of which preset R5 form a part is unused. Therefore no setting-up procedure is given for R5 in this publication, but will be supplied as required in installations which employ the AUX ANAL. input to IC15 of Module 12 Analogue panel.

5.3 MPU - Controlled Circuits

As has been stated elsewhere in this chapter, we do not advocate that maintainers attempt to carry out any diagnosis or repair in the MPU-controlled part of Module 12 circuits, i.e. the MPU, PROM, RAM, address circuits, and input-output ports. However, faults may occur which produce symptoms strongly suggesting the failure of a particular integrated circuit: in such cases it can be of value to carry out a 'repair by substitution' of the suspect integrated circuit. No tools are required, as these items are fitted in plug-in DIL sockets. All CMOS handling precautions must be observed, and any integrated circuit not fitted in its socket must be always shorted out by a piece of conducting foam material. It is also good practice never to handle a CMOS component with the fingers; always use IC insertion/removal tongs which short together all pins while the component is handled.

6. COMPONENT LISTS

6.1 Module 12 Assembly (un-programmed) (630/1/32992)

Circuit Ref.	Description & Tolerance	Manufacturer & Ref.	Part No.
-	Panel, Electronic Cct., Analogue Panel	Plessey	419/1/18061
-	Panel, Electronic Cct., CPU Panel	Plessey	419/1/18063
-	Panel, Electronic Cct., Switch Panel	Plessey	419/1/18053
-	Battery, re-chargeable, 4.5V, 80 mAH, 24 mA	Medicharge R4.5880	999/4/32776/002

6.2 Module 12 Assembly (programmed) (630/1/32992/001)

Circuit Ref.	Description & Tolerance	Manufacturer & Ref.	Part No.
-	Module 12 Assy. (un-programmed)	Plessey	630/1/32992
IC10	Integrated Cct., programmed	Plessey program	445/1/10672/001

6.3 Panel, Electronic Cct., Analogue Panel (419/1/18061)

Circuit Ref.	Description & Tolerance	Manufacturer & Ref.	Part No.
PL1	Connector Assembly	Plessey	705/1/12583/002
with IC14	Socket, IC, 14-pin DIL	Texas C831402	508/4/22194/002
with IC9, 12,13,16, 17,18	Socket, IC, 16-pin DIL	Texas C831602	508/4/22194/003
with IC1-7, 10	Socket, IC, 20-pin DIL	Texas C832002	508/4/22194/009
with IC15	Socket, IC, 28-pin DIL	Texas C832802	508/4/22194/007
PL13	Connector, PC, 65 contact	Socapex 127-65-B1061	508/4/22218/001
	Resistors, 0.25W, ± 2% as follows:	Electrosil TR4	
R38	100 ohm		403/4/05522/100
R35,37	330 ohm		403/4/05522/330
R22,23	390 ohm		403/4/05522/390
R42	470 ohm		403/4/05522/470
R7,8,31	1k ohm		403/4/05523/100
R32,33	2.2k ohm		403/4/05523/220
R34,36	6.8k ohm		403/4/05523/680
R9,43	10k ohm		403/4/05524/100
R13,18,21	22k ohm		403/4/05524/220
R1,3,4,6	27k ohm		403/4/05524/270
R25,40	33k ohm		403/4/05524/330
R10,24	56k ohm		403/4/05524/560
R27,28	62k ohm		403/4/05524/6
R12,14-17, 19,20,25, 29,35	100k ohm		403/4/05525

6.3 Panel, Electronic Cct., Analogue Panel (419/1/18061) continued ...

Circuit Ref.	Description & Tolerance	Manufacturer & Ref.	Part No.
	Resistors, 0.25W, ± 2% as follows:	Electrosil ZR4	
R11	150k ohm		403/4/05525/150
R2,5,26,41	Resistor, variable, 10k ohm ± 20%, 0.75W	AB Type 90H	404/9/05047/005
R30	Resistor, variable, 47k ohm ± 20%, 0.75W	AB Type 90H	404/9/05047/006
IC11	9 x 100k ohm resistors, ± 2%, 2.7W	Beckman 785-1-R100K	403/4/07080/008
C9	Capacitor, 22 pF ± 10%	Erie Redcap 3121M-100-220-004	400/9/19467/006
C4,6,11,14, 17,20-23	Capacitor, ceramic, 10 nF, 100V d.c.	ITT.WPH5K210NDZS	400/9/20626
C7	Capacitor, plastic, 330 nF ± 5%, 100V d.c.	Siemens B32560-B1334J	435/4/90317/012
C8	Capacitor, plastic, 1 uF ± 5%, 100V d.c.	Siemens B32561-B1105J	435/4/90827/005
C10,12,13	Capacitor, electrolytic, 1 uF, 35V d.c.	ITT.TAG1.0/35	402/4/57057/003
C1,2,3,5, 16,18,19	Capacitor, electrolytic, 10 uF, 16V d.c.	ITT.TAG10/16	402/4/57057/006
RLA	Relay, sealed D/P C/O, 4.3V, 220 ohm	Thorn Bendix RS-6	507/4/98271
D1	Diode, switching, high-speed	H-P.5082-2800	415/4/98532
D2-7	Diode, switching, high-speed	1N4148	415/4/05720
IC8,9	Integrated circuit	(Motorola MC14050BCP) (RCA SD4050BE)	445/4/02383/050
IC1-7,10	Integrated circuit	Nat'l MM74C373N	445/4/02430/373
IC12,13	Integrated circuit	(Mullard) HEF (Synetic) 4104 BP	445/4/03123
IC14	Integrated circuit	RCA CA224G	445/4/03067
IC18	Integrated circuit	(Motorola MC14053BCP) (RCA CD4053BE)	445/4/02383/053
IC15	Integrated circuit	Nat'l ADC0809CCN	445/4/03121
IC16,17	Integrated circuit	Ferranti ZN428J-8	445/4/03122
TR1-4,6,8	Transistor, NPN, 0.3W, 0.15 GHz	Ferranti ZTX302L	417/4/01875
TR5,7	Transistor, PNP, 0.3W, 0.15 GHz	Ferranti ZTX502L	417/4/01576

6.4 Connector Assembly (705/1/12583/002)

Circuit Ref.	Description & Tolerance	Manufacturer & Ref.	Part No.
-	Connector, PCB, Male	Thomas & Betts 609-6003	508/4/22253/011
-	Connector, PCB, Female	Thomas & Betts 609-6001M	508/4/22254/011
-	Cable, ribbon, 250mm long	Thomas & Betts 172-60	998/4/83574/012

6.5 Panel, Electronic Cct., CPU Panel (419/1/18063)

Circuit Ref.	Description & Tolerance	Manufacturer & Ref.	Part No.
PL1	Connector, PC, 60 contact	Ansley 6B-602E	508/4/22247/011
with IC10	Socket, IC, 24-pin DIL, raised	Liflock 54601-S	508/4/22248/007
with IC3-5, 16	Socket, IC, 14-pin DIL	Texas C831402	508/4/22194/002
with IC7,8, 13-15,SKA	Socket, IC, 16-pin DIL	Texas C831602	508/4/22194/003
with IC9, 11,12	Socket, IC, 24-pin DIL	Texas C832402	508/4/22194/006
with IC2	Socket, IC, 40-pin DIL	Texas C834002	508/4/22194/008
with IC6, 17-23	Socket, IC, 20-pin DIL	Texas C832002	508/4/22194/009
	Resistors, 0.25W, ± 2% as follows:	Electrosil TR4	
R3	470 ohm		403/4/05522/470
R4	3.9k ohm		403/4/05523/390
R2,5	4.7k ohm		403/4/05523/470
R6	6.8k ohm		403/4/05523/680
R1	10k ohm		403/4/05524/150
R17	22k ohm		403/4/05524/220
R11,12	68k ohm		403/4/05524/680
R7,8,10, 13-16	100k ohm		403/4/05525/100
R9	Resistor, 10M ohm ± 5%, 0.25W	Erie 00026-012	403/4/04361/004
IC37	9 x 22k ohm resistors, ± 2%, 2.7W	Beckman 785-1-R22K	403/4/07080/013
IC24,26,28, 30,32,34, 36	9 x 100k ohm resistors, ± 2%, 2.7W	Beckman 785-1-R100K	403/4/07080/008
IC25,27,29, 31,33,35	8 x 100k ohm resistors, ± 2 ohm, 1.5W	Beckman 785-1-R100K	403/4/07080/008
C8,9	Capacitor, 22 pF ± 10%	Erie Redcap 8121M-100-220-COG	400/9/19467/006
C1,6,10, 12-14	Capacitor, ceramic, 10 nF, 100V d.c.	ITT.WPH5K210N0ZS	400/9/20626
C7,11	Capacitor, electrolytic, 1 uF, 35V d.c.	Union Carbide K1R0 E35	402/4/57057/003
C2,5	Capacitor, electrolytic, 10 uF, 16V d.c.	ITT Tag 10/16	402/4/57057/008
L1	Inductor, 22 uH ± 10%, 231 mA	Plessey 030M	406/4/31753/028
XL1	Crystal, 1.9968 MHz, 'D' can	ITT 4208	WL/18063/038
D1,3	Diode, switching, high-speed	1N4148	415/4/05720
D2	Diode, switching, high-speed	HP 5082-28000	415/4/98532
D4	Diode, zener, 10V, 0.4W	Mullard BZY88C10V	415/4/02792/015
IC1	Integrated circuit, voltage regulating	Motorola MC7805	445/9/03051/001
IC11,12	Integrated circuit	RCA CDP18521	445/4/10497/001
IC3	Integrated circuit	Motorola MC14013	445/4/02383/013
IC2	Integrated circuit	RCA CDP1802D	445/4/10498/001

6.5 Panel, Electronic Cct., CPU Panel (419/1/18063) continued ...

Circuit Ref.	Description & Tolerance	Manufacturer & Ref.	Part No.
IC4	Integrated circuit	(Motorola MC14093BCP) (RCA CD4093BE)	445/4/02383/093
IC5	Integrated circuit	(Motorola MC14069BCP) (RCA CD4069BE)	445/4/02383/069
IC9	Integrated circuit	RCA CDP1823SD	445/4/10499
IC6,17-23	Integrated circuit	Nat'l MM74C373N	445/4/02430/373
IC7,8	Integrated circuit	Nat'l MM74C42N	445/4/02430/042
IC13,14	Integrated circuit	(Mullard) HEF (Signetic) 4014 SP	445/4/03123
IC15	Integrated circuit	RCA CDP1853D	445/4/10623/001
IC16	Integrated circuit	(Motorola MC14072BCP) (RCA CD4071BE)	445/4/02383/071
IC10	See para.6.2	-	-
TR1	Transistor, NPN, 0.3W, 0.15 GHz	Ferranti ZTX302L	417/4/01875
TR2	Transistor, PNP, 0.3W, 0.15 GHz	Ferranti ZTX502L	417/4/01876

6.6 Panel, Electronic Cct., Switch Panel (419/1/18053)

Circuit Ref.	Description & Tolerance	Manufacturer & Ref.	Part No.
IC1	Switches, rocker, 8 x SPST in DIL pack	Augat DSS-C8	408/4/51540/008

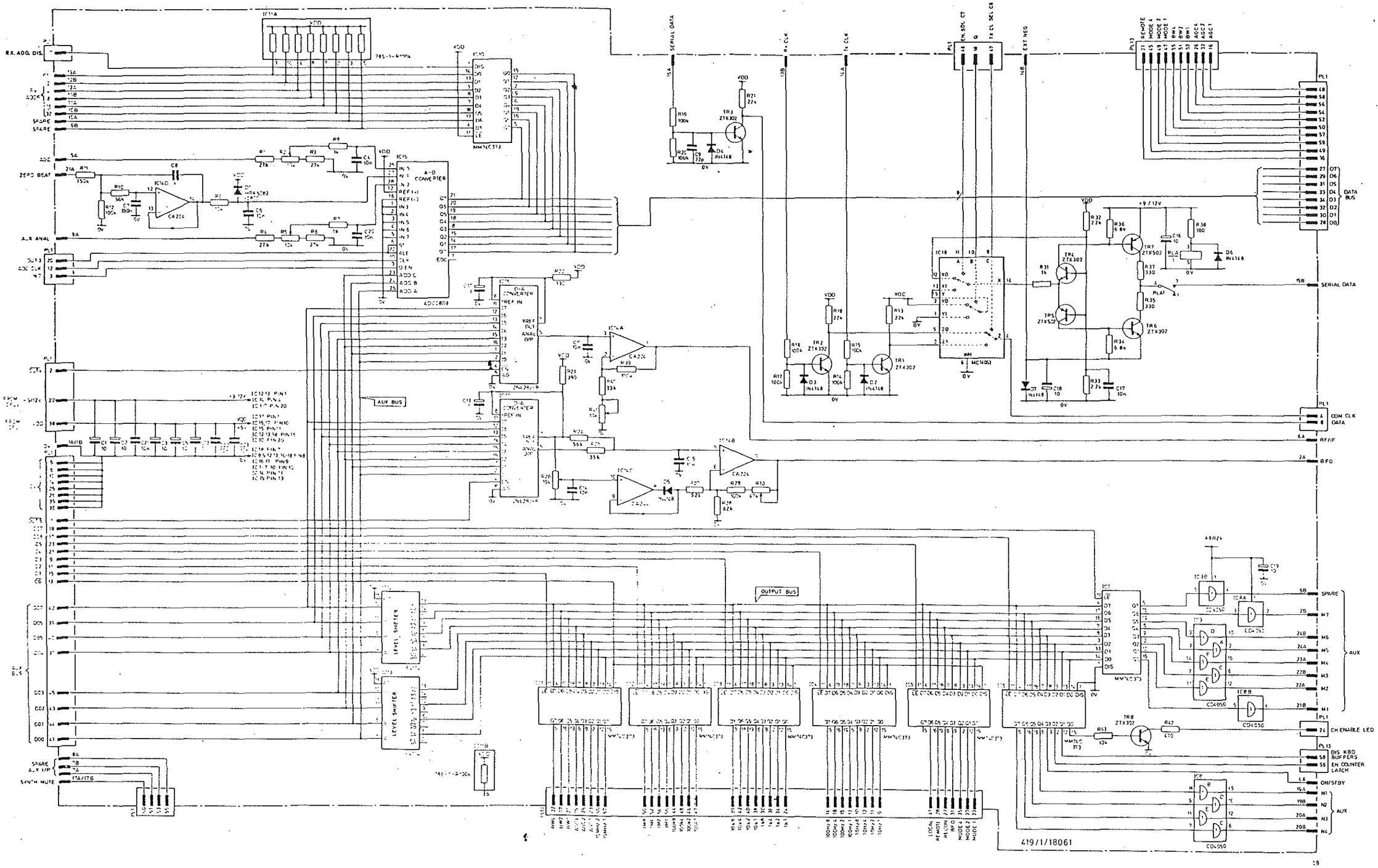


FIG 1

MODULE 12 : ANALOGUE PANEL – CIRCUIT DIAGRAM

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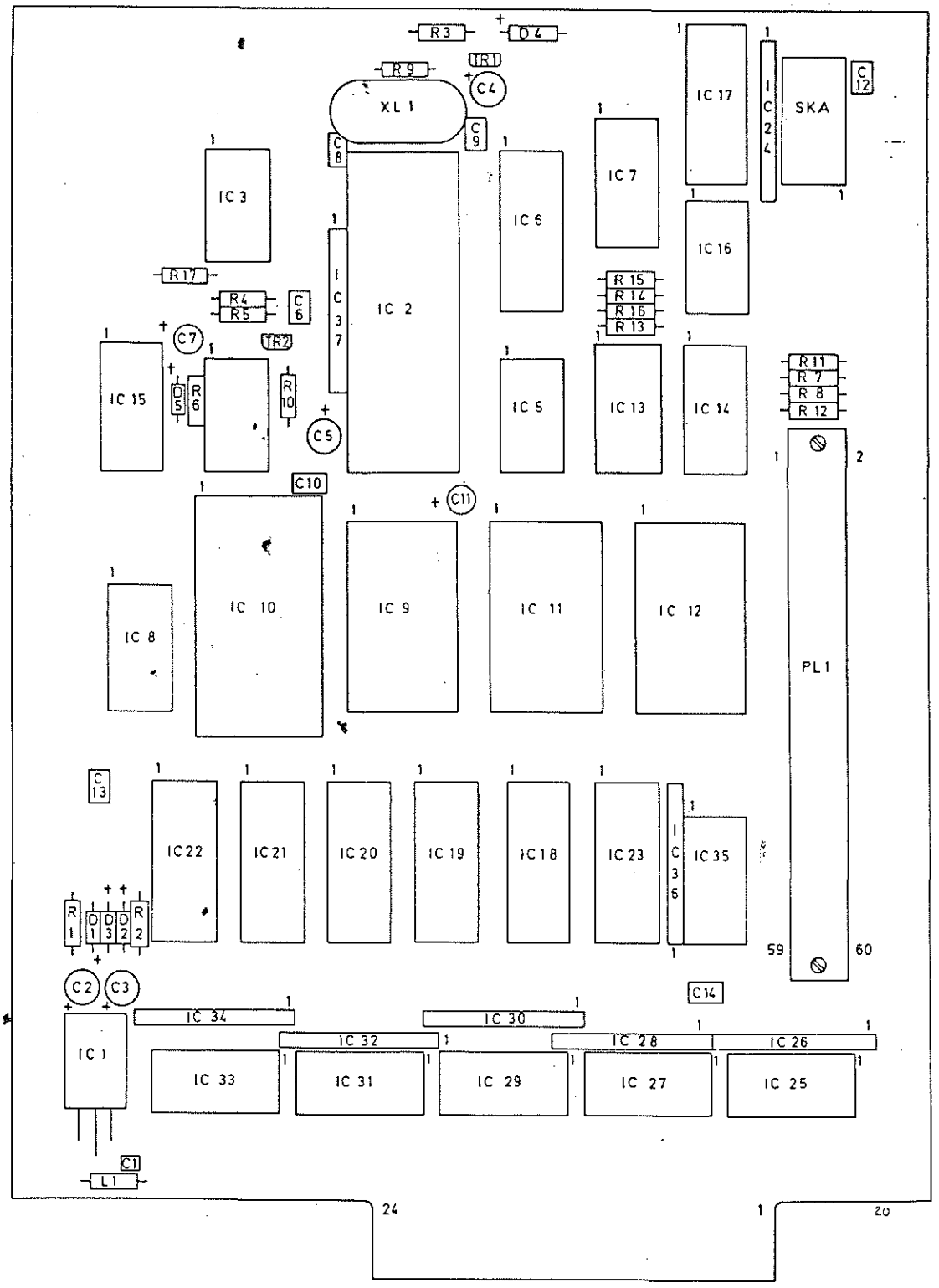

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CPU PANEL - COMPONENT LAYOUT

FIG 3

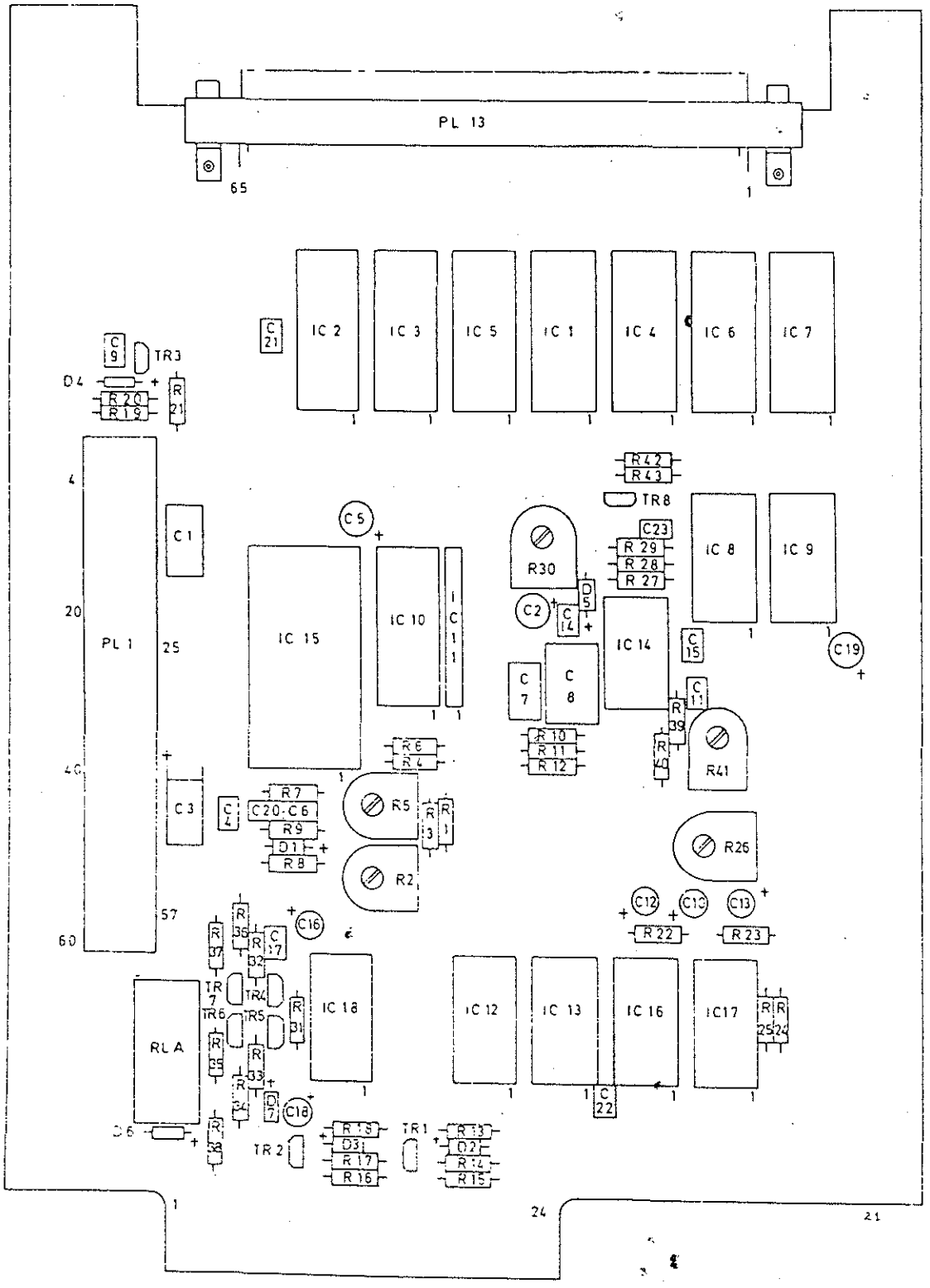


FIG 4 ANALOGUE PANEL - COMPONENT LAYOUT

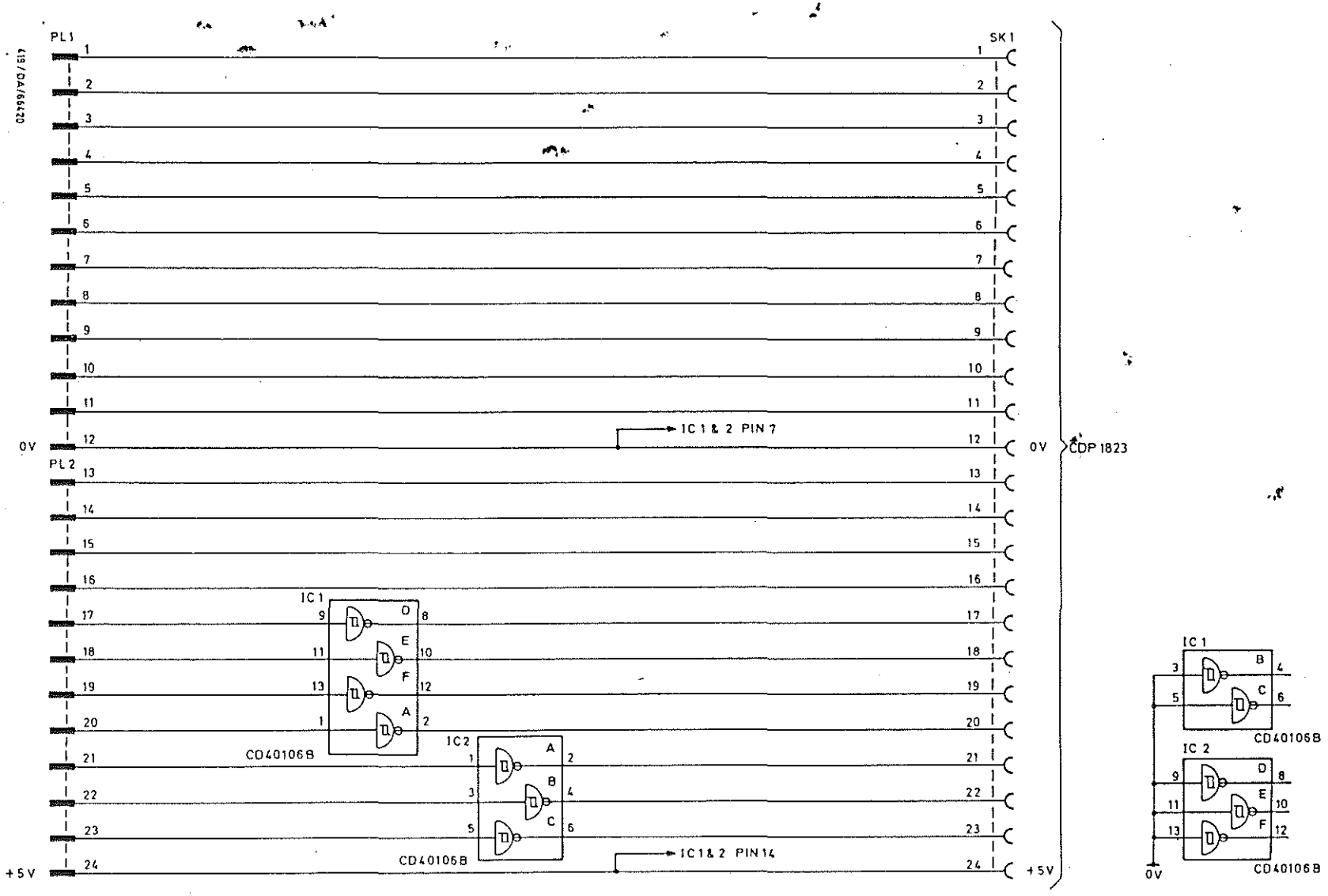


Fig 5 Composite Version of IC9

INTEGRATED CIRCUIT DEFINITIONS

This information forms a supplement to the circuit diagrams in respect of complex integrated circuits which are shown diagrammatically by a retangular outline only.

CDP1802 Microprocessor

Fully described in text. Part of the RCA COSMAC 1800 series.

CDP1852

A parallel 8-bit mode-programmable input-output port. Mode control at '0' programs the device as an input port: mode control at '1' programs the device as an output port. As an input port, data is strobed into the internal 8-bit register by a '1' level clock. The '1-0' clock transition sets the Service Request flip-flop ($\overline{SR}$ = 0) and latches the data in the register. The $\overline{SR}$ output can be used to signal the associated microprocessor. When CS2 and CS1 (CS = 'chip select') both equal '1' the 3-state output drivers are enabled. The '1-0' transition of CS1 and CS2 resets the SR flip-flop (SR = 1).

As an output port, data is strobed into the register when $\overline{CS1}$ and CS2 and CLOCK equal '1'.

The 3-state output drivers are enabled at all times when the device is operating as an output port. The Service Request signal is generated at the termination of '$\overline{CS1}$ and CS2 equal '1'' and remain at '1' until the following '1-0' clock transition.

$\overline{CLEAR}$ resets the register and the SR flip-flop.

CDP1853

A 'one of eight' decoder designed to interface directly with a CDP 1800 series microprocessor.

N2	N1	N0	EN	1	2	3	4	5	6	7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	1	1	0	0	0	0	0	0
0	1	0	1	0	1	0	0	0	0	0
0	1	1	1	0	0	1	0	0	0	0
1	0	0	1	0	0	0	1	0	0	0
1	0	1	1	0	0	0	0	1	0	0
1	1	0	1	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	1
X	X	X	0	0	0	0	0	0	0	0

CE	CL.A	CL.B	EN
1	0	0	*
1	0	1	1
1	1	0	0
1	1	1	1
0	X	X	0

* = ENABLE remains in previous state.

HEF4104

A quad low voltage/high voltage level shifter producing both true and complementary outputs via tri-state logic. Logic Level inputs to I0, I1, I2, and I3 are level shifted and appear on Z0, $\overline{Z0}$, Z1, $\overline{Z1}$, Z2, $\overline{Z2}$ and Z3, $\overline{Z3}$. The device is active with the E0 input held at '1'; with E0 = '0', all outputs are high impedance.

MM74C42

A 4-bit parallel input BCD/decimal decoder. For any binary input value between 0 and 9, the appropriate one of the ten outputs falls to logic '0'. For input values between 10 and 15, all output levels remain at logic '1'.

I2716

A 2K x 8 UV-erasable and electrically-programmable PROM. Not that the IC has, on its upper surface, an opaque label; this label masks a transparent 'window' over the active portion of the device. Do not remove this label as, with the label removed, erasure can occur if the device is exposed to sunlight or fluroescent tube light for a period of several days.

$\overline{CE}$ is the power control, used for device selection. $\overline{OE}$ is the output control, used to gate data to the output pins. Data is available at the output pins 120 nS after the '1-0' edge of $\overline{OE}$. To place the device in the standby mode, reducing active power dissipation by 75%, a '1' level is applied to $\overline{CE}$: in this mode, all outputs are high impedance irrespective of $\overline{OE}$ level.

ZN428J-8

An 8-bit latched input digital/analogue converter. It contains a D-A converter using a switched resistive network supplied by an externally applied reference source. Input latches are transparent to data when $\overline{ENABLE}$ = '0': data is held when $\overline{ENABLE}$ = '1'. A data input of 'all 1' produces an output level within one LSB of VREF. A data input of 'all 0' produces an output level of 0V. Response is linear.

ADC0809

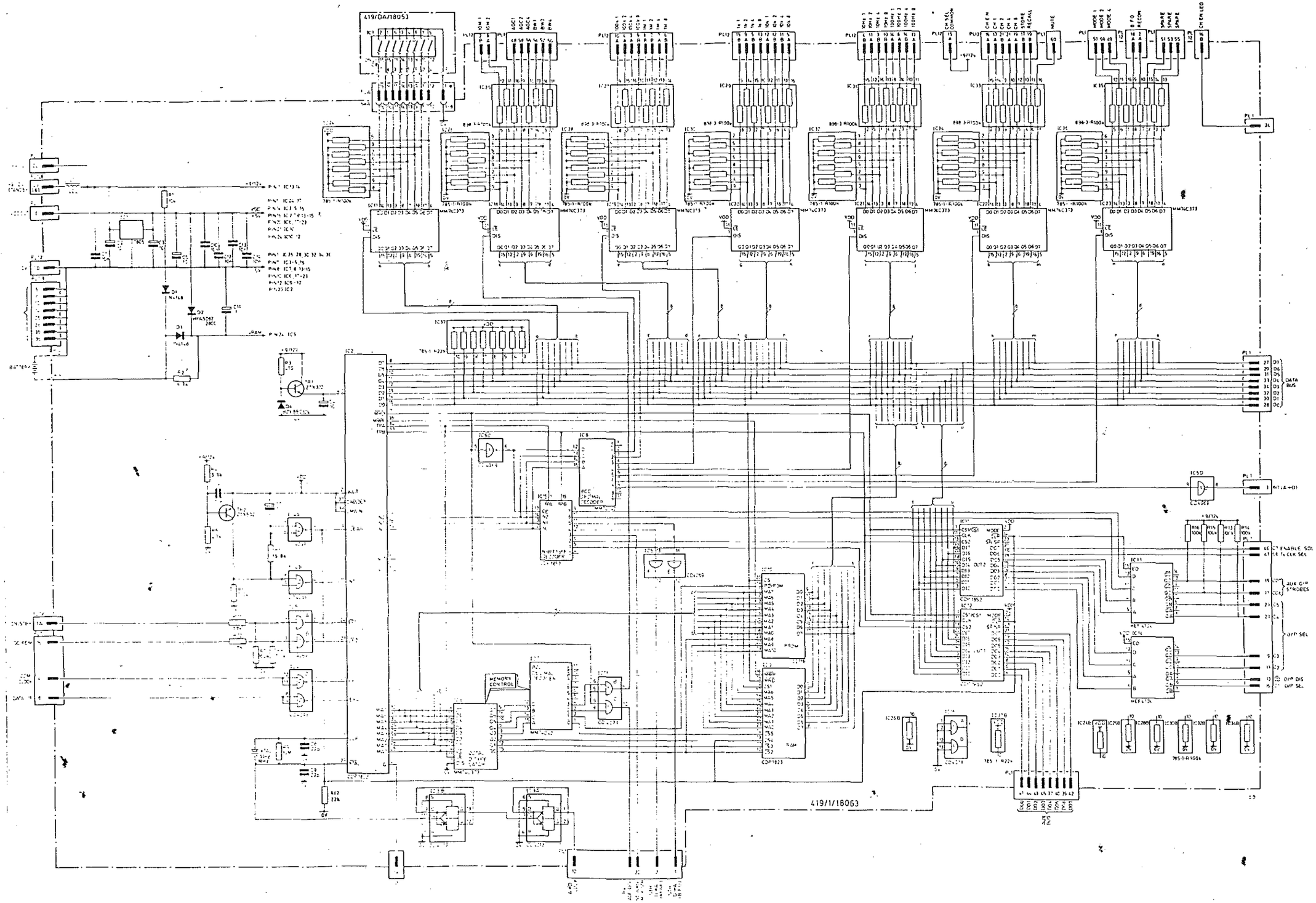
An 8-bit analogue/digital converter incorporating input switching to select any one of eight applied inputs by means of a 3-bit address. Address input is activated by setting ADDRESS LATCH ENABLE input to '1'. The A/D converter uses a switched resistive network supplied by an externally applied reference source. The applied input and the resistive network feed a comparator input to a successive-approximation register, producing a high degree of conversion accuracy. The digital output is produced as an 8-bit parallel number.

MM73C373

An 8-bit D type latch. When $\overline{\text{LATCH ENABLE}}$ = '1', the Q outputs follow the D inputs. When $\overline{\text{LATCH ENABLE}}$ = '0', data at the D inputs is retained at the outputs until $\overline{\text{LATCH ENABLE}}$ level returns to '1'. Outputs are taken via tri-state buffers. When OUTPUT DISABLE = '0', outputs are available; when OUTPUT DISABLE = '1', all outputs are high impedance.

CDP1823

A 128-word, 8-bit, static random-access memory (RAM). The device has 8 common data input-output terminals (BUS 0 to BUS 7) for direct connection to a bi-directional data bus. Five CS (chip select) inputs are provided for memory expansion. To enable the device, $\overline{\text{CS2}}$, $\overline{\text{CS3}}$ and $\overline{\text{CS4}}$ must be at '0', and CS1 and CS5 must be at '1'. The $\overline{\text{MRD}}$ (memory read) input enables all 8 output drivers when set to '0', and should be at '1' during a 'write' cycle. Output data is valid until either $\overline{\text{MRD}}$ is set to '1', the device is de-selected, or after the access time (typically 200nS) of an address change has elapsed. MA0 to MA6 are address inputs. $\overline{\text{MWR}}$ is 'memory write'.



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MODULE 12 : CPU PANEL - CIRCUIT DIAGRAM

FIG 2

CHAPTER 13

INTERFACE MODULE

CONTENTS

ILLUSTRATIONS

INTERFACE MODULE

1. FUNCTIONAL DESCRIPTION

1.1 The interface module is fitted in the PR2251 model. It consists of 8 quad bi-lateral switch integrated circuits and a power control circuit. Each switch acts as a buffer stage, and is enabled by a '1' level control input. All 32 circuits are identical, therefore only one will be described.

2. CIRCUIT DESCRIPTION

2.1 The circuits will be described in terms of that between pin 1 of PL1 and pin 1 of PL2. The input from the master receiver is fed onto pin 10 of IC1, which is returned to 0V via 100k ohm. The output, also returned to 0V via 100k ohm, is taken from pin 11 and is fed to the slave receivers via pin 1 of PL2. The control input is applied to pin 12.

2.1.1 A power control circuit consisting of D1-4, C1 and R1 is provided. +15V is fed into this circuit from both the master receiver and the slave receiver. When both +15V inputs are presemt, D1 and D2 conduct. This produces logic '1' at D3-D4 junction, causing the switches to close and completing the paths between master receiver and slave receiver.

2.1.2 If either +15V were low, D3 or D4 would conduct, producing logic '0' at D3-D4 junction, causing the switches to open and breaking the circuits between master and slave receivers.

3. TEST DATA

3.1 General

The procedure outlined in the following paragraphs forms a complete test procedure and need not be used to locate individual faults.

3.2 Test Equipment

The following items of test equipment are required:

1000 ohm resistor.

Oscilloscope (general purpose).

Signal Generator capable of producing 1MHz at 2.5V peak-to-peak.

3.3 Functional Tests

3.3.1 Apply a sine wave signal input of 2.5V peak-to-peak between all the inputs strapped together and 0V.

3.3.2 Connect +15V to pins 50 of PL1 and PL2; 0V to pin 17.

3.3.3 Check for an undistorted 2V peak-to-peak minimum on each of the outputs, using an oscilloscope across a load of 1000 ohms.

3.3.4 Remove one 15V supply and check that all outputs stop.

3.3.5 Replace the first 15V supply and remove the other. Check that again all the outputs stop.

4. COMPONENT LISTS

Main Assembly (630/1/35330)
Panel Electronic Circuit (419/1/18065)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
-	Panel Printed Circuit	Plessey	419/2/18066
-	Socket, Semi-Conductor	Texas 14L DIL C831402	508/4/22194/002
C1	Capacitor 0.01uF ± 5% 400V	Siemens V32560	435/4/90317/029
IC1-8	Integrated Circuit	Motorola MC14066BCL	445/4/10796
IC9-15	Resistor Package, 10 lead	Beckman 785-1-R100K	403/4/07080/008
R1,2	Resistor 100k ± 2%	Electrosil TR4	403/4/05525/100
D1-4	Diode	Texas 1N4148	415/4/05720
PL1	Plug, Electrical	Cannon DD51223-1	508/4/28805/005

Connector Assembly (705/1/12560)

Circuit Ref.	Description and Tolerance	Manufacturer and Ref.	Part No.
PL2	Plug, Electrical	Cannon DD-50P	508/4/28010/007
-	Adaptor Cable to Elec Plug-Socket	Cannon DD51216-1	508/4/22125/005

TABLE 1 : KEY ANALOGUE LEVELS

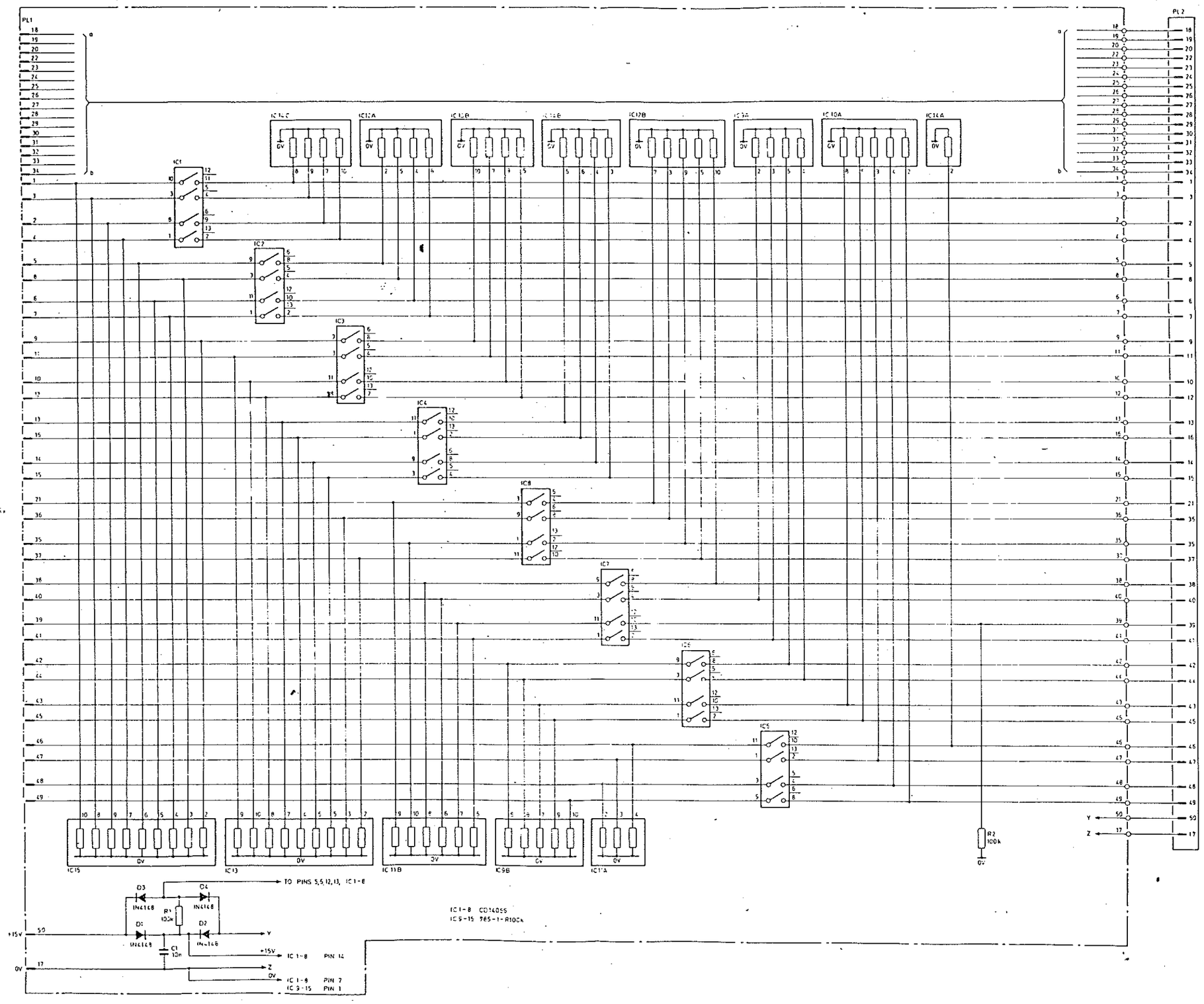
MODULE	MODE	INPUT(S) SIGNAL	INPUT(S) SOCKET	OUTPUT(S) SIGNAL	OUTPUT(S) SOCKET
1	ALL	15500kHz AM, 30% mod, 1mV rms, 50 ohm from Sig. Gen.	AERIAL	1500kHz, -3dB w.r.t. input sig., 50 ohm	SKH
2	ALL	LO(1); from Module 9 SKA, 65000kHz to 94999.99kHz, 8dBm ±3, 50 ohm. Signal; from Module 1 SKH (unchanged).	SKG SKA	65000kHz, +4dB +0 -2 w.r.t. Module 1 output, 50 ohm	SKC
3	ALL	LO(2); from Module 9 SKB 63600kHz, 8dBm ±3, 50 ohm. Signal; from Module 2 SKC (unchanged).	SKH	1400kHz, +10dB ±2 w.r.t.Module 2 output 1000 ohm (Measured with 50 ohm meter)	SKB
4	USB, F, ISB, CW & 0.1 B/W AM, ISB LSB, ISB CW not 0.1 B/W	) Signal; from) Module 3 SKB) (unchanged:) measured with) a 50 ohm meter)	SKA	1400kHz, 15mV r.m.s. ±2dB, 50 ohm. 1400kHz, 10mV r.m.s. ±2dB, 50 ohm. 1400kHz, 10mV r.m.s. ±2dB, 50 ohm. 1400kHz, 20mV r.m.s. ±2dB, 50 ohm.	SKF SKC SKE SKF
5	AM, ISB USB, ISB (U), CW, F not 0.1 LSB, ISB (L) ALL ALL ALL ALL	Signal; from Module 4 SKC (unchanged). Signal; from Module 4 (unchanged). Signal; from Module 4 SKE (unchanged). 1.4MHz LO; from Module 6 SKA (unchanged). (50 ohm meter). 1.5MHz LO; from Module 6 SKC (unchanged). (50 ohm meter).	SKA SKB SKD SKC SKE	'100kHz IF' outputs. 100mV r.m.s. ±20mV, 50 ohm, or as set up. Variable level audio to speaker and phones.	SKF

TABLE 1 continued ...

MODULE	MODE	INPUT(S)		OUTPUT(S)	
		SIGNAL	SOCKET	SIGNAL	SOCKET
6	LSB	Signal; from Module 4 SKF (unchanged). Ref; from Module 7 SKA (unchanged).	SKE SKG	1400kHz (nominal) 10mV r.m.s, 1000 ohm (measured with 50 ohm meter).	SKA & SKC
7	ALL	-	-	1000kHz, 290mV, r.m.s. 50 ohm.	SKA
9	ALL	-	-	65000kHz to 94999.99kHz, 8dBm ±3, 50 ohm (LO1). 63600kHz, 8dBm ±3, 50 ohm (LO2).	SKA SKB

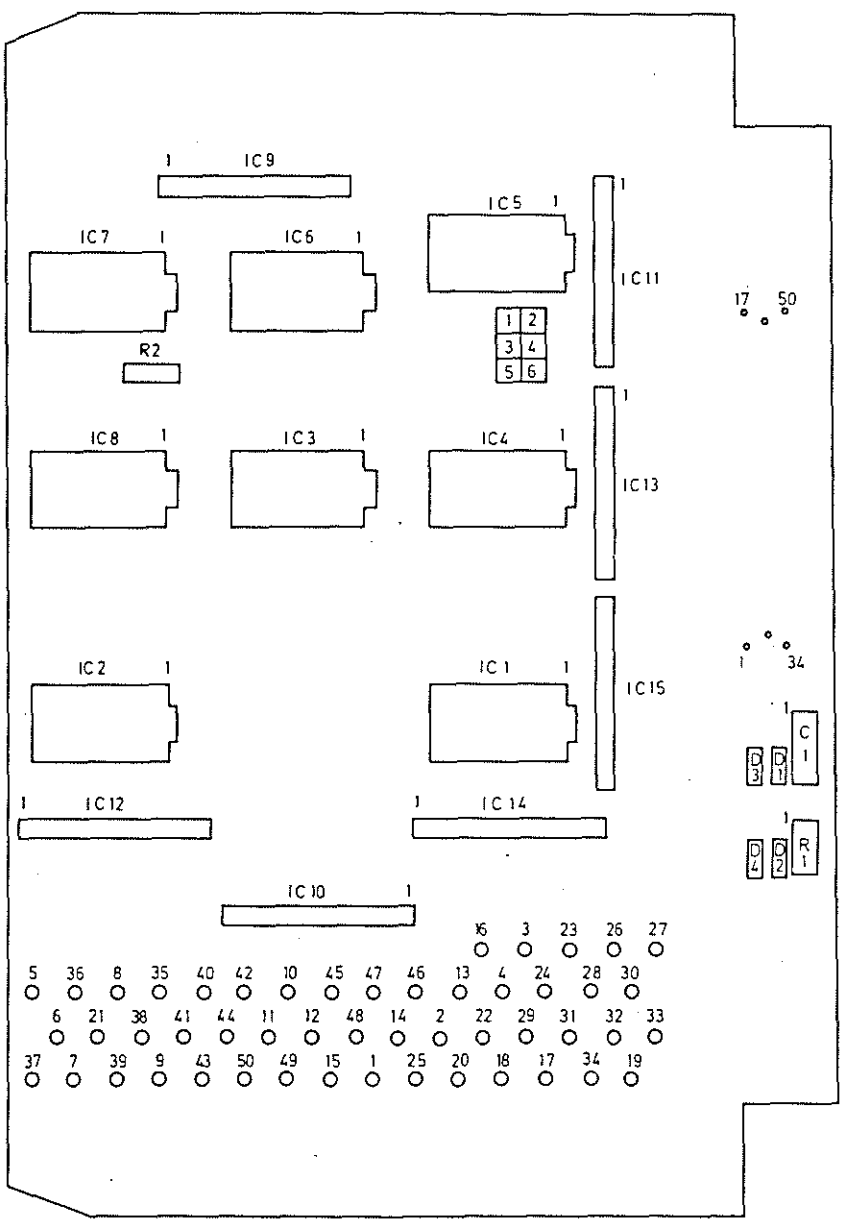
FROM MASTER Rx

TO SLAVE Rx



INTERFACE MODULE : CIRCUIT DIAGRAM

FIG I



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INTERFACE MODULE - COMPONENT LAYOUT

FIG 2

CHAPTER 14

INTERCONNECTIONS

CONTENTS

ILLUSTRATIONS

INTERCONNECTIONS

1. INTRODUCTION

All the electronics of the PR2250 Series receivers are situated in the various modules, and are interconnected in the receiver frame by either flat flexible multi-way plastic strips or by co-axial cable links. As the front panel also forms a module, the large amount of fixed wiring associated with a conventional non-removeable front-panel is eliminated; instead a maximum (according to the model of receiver) of three flat flexible multi-way connectors carry all lines to the front-panel. The physical layout is described in Section 3, Chapter 1.

2. DESCRIPTION

2.1 RF Interconnections

All r.f. interconnections are made by lengths of RG174/U 50 ohm co-axial cable, except for the line from the rear panel AERIAL socket; this uses RD316 50 ohm co-axial cable. All connections to modules are made by Belling-Lee miniature co-axial plugs and sockets.

2.2 Non-RF Interconnections

All interconnections which do not carry r.f. signals are made via multi-pin connectors on the various modules. These plug into mating connectors on multi-way strip connectors which run through the centre of the receiver and out at the front to the point where flexible multi-way strips plug in from the front-panel.

3. VARIATIONS

3.1 The interconnection harness is standard on all PR2250 Series receivers. PR2251 receivers do not employ all the lines to the front-panel and do not contain Modules 7 and 9; therefore the lines to these module positions are not used.

3.2 Figures 1 to 5 form a full statement of the interconnection harness. Unused lines to the front-panel in PR2251 receivers can be seen from the diagrams in Chapter 10 of this section of the manual, 'Modules 10, 10A and 10B'.

3.3 PR2251 Receivers employ an Interface Module as an input buffer on incoming control lines. This module is defined in terms of interconnections in Fig.3. As can be seen, this module connects to the receiver solely via the rear panel CONTROL socket, through which it also receivers power supplies.

MODULE 11/12

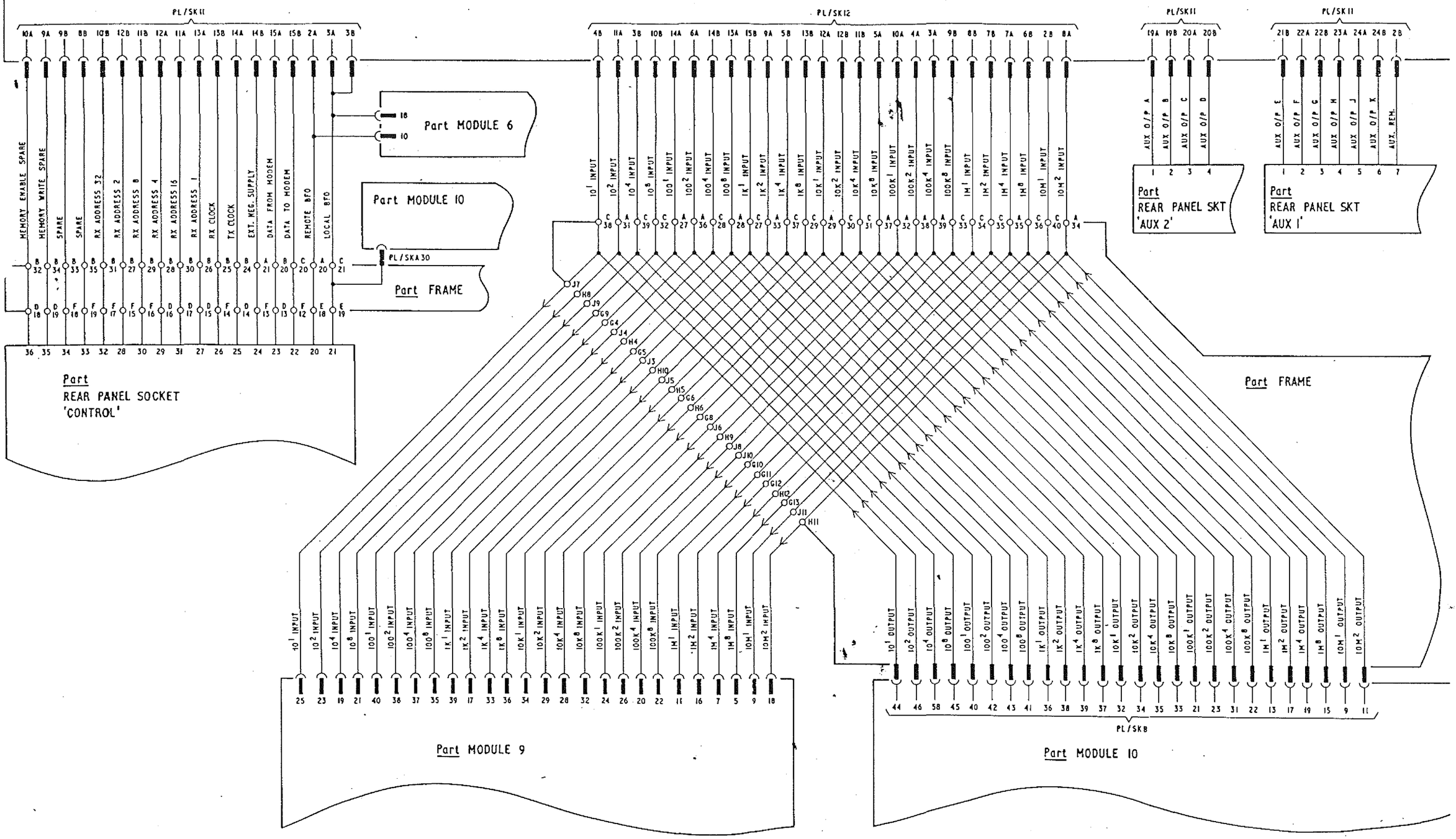
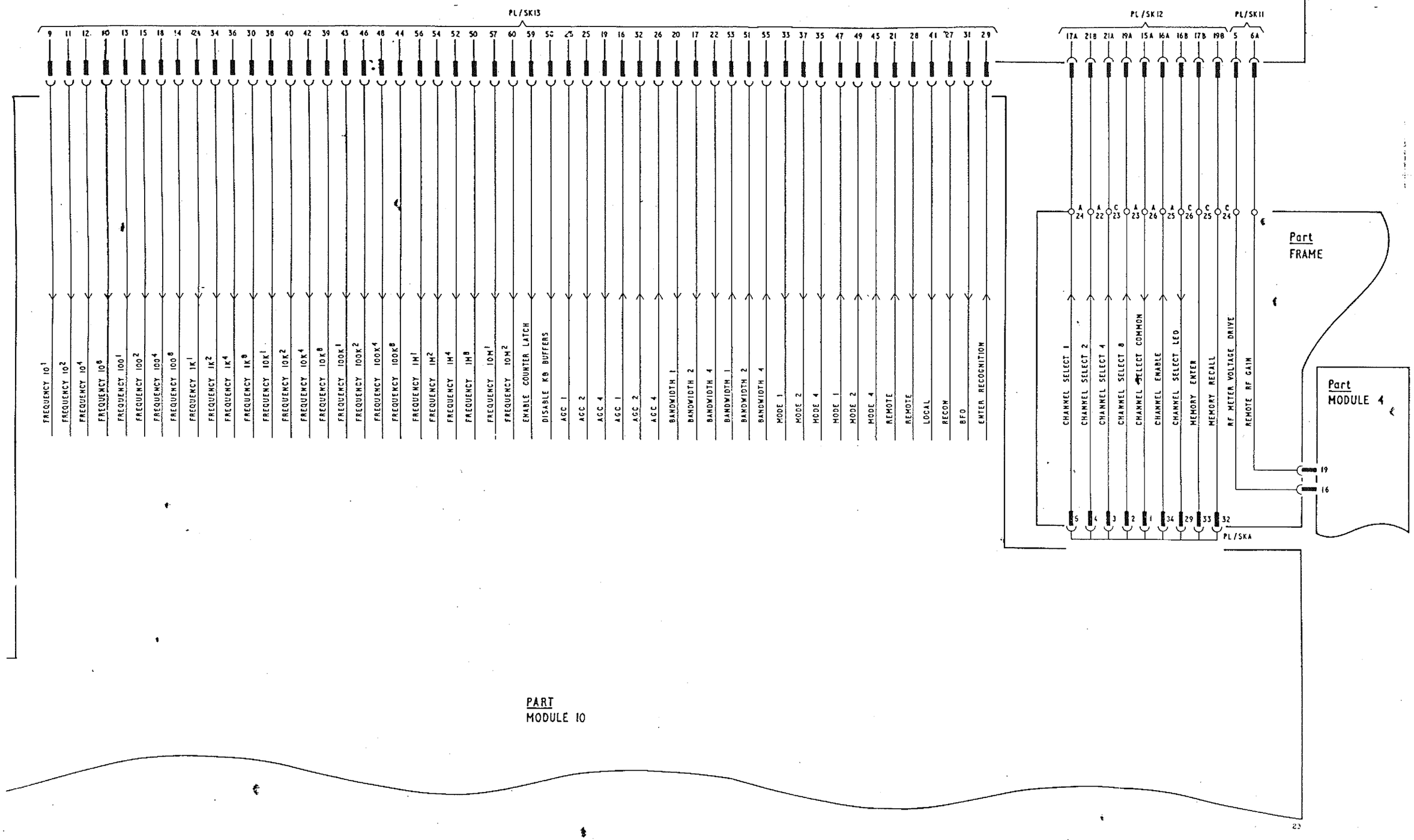


FIG 1

PR2250 INTERCONNECTION DIAGRAM(a)

MODULE 11 / 12



PART
MODULE 10

PR2250 INTERCONNECTION DIAGRAM(b)

FIG 1

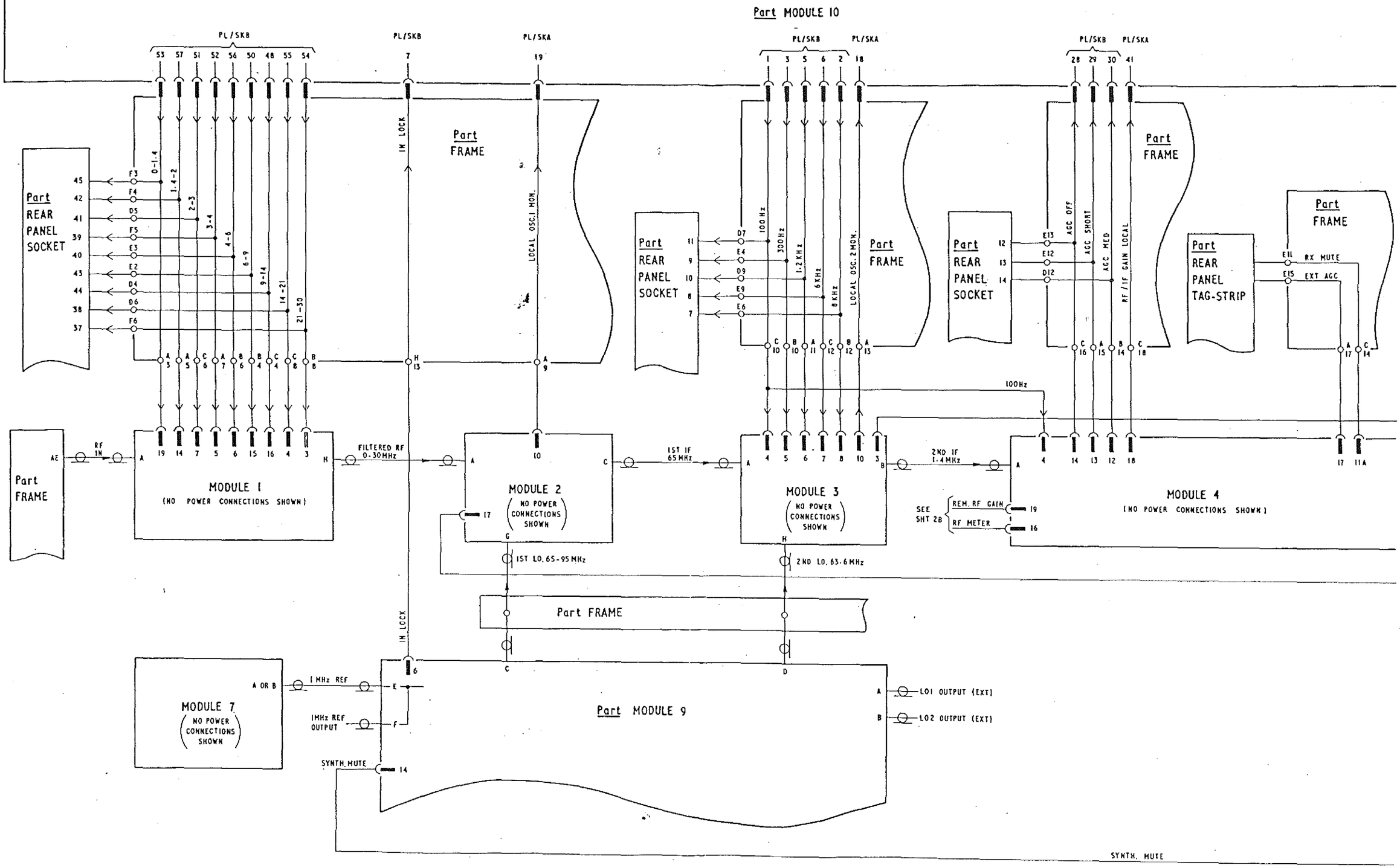


FIG 2

PR2250 INTERCONNECTION DIAGRAM (c)

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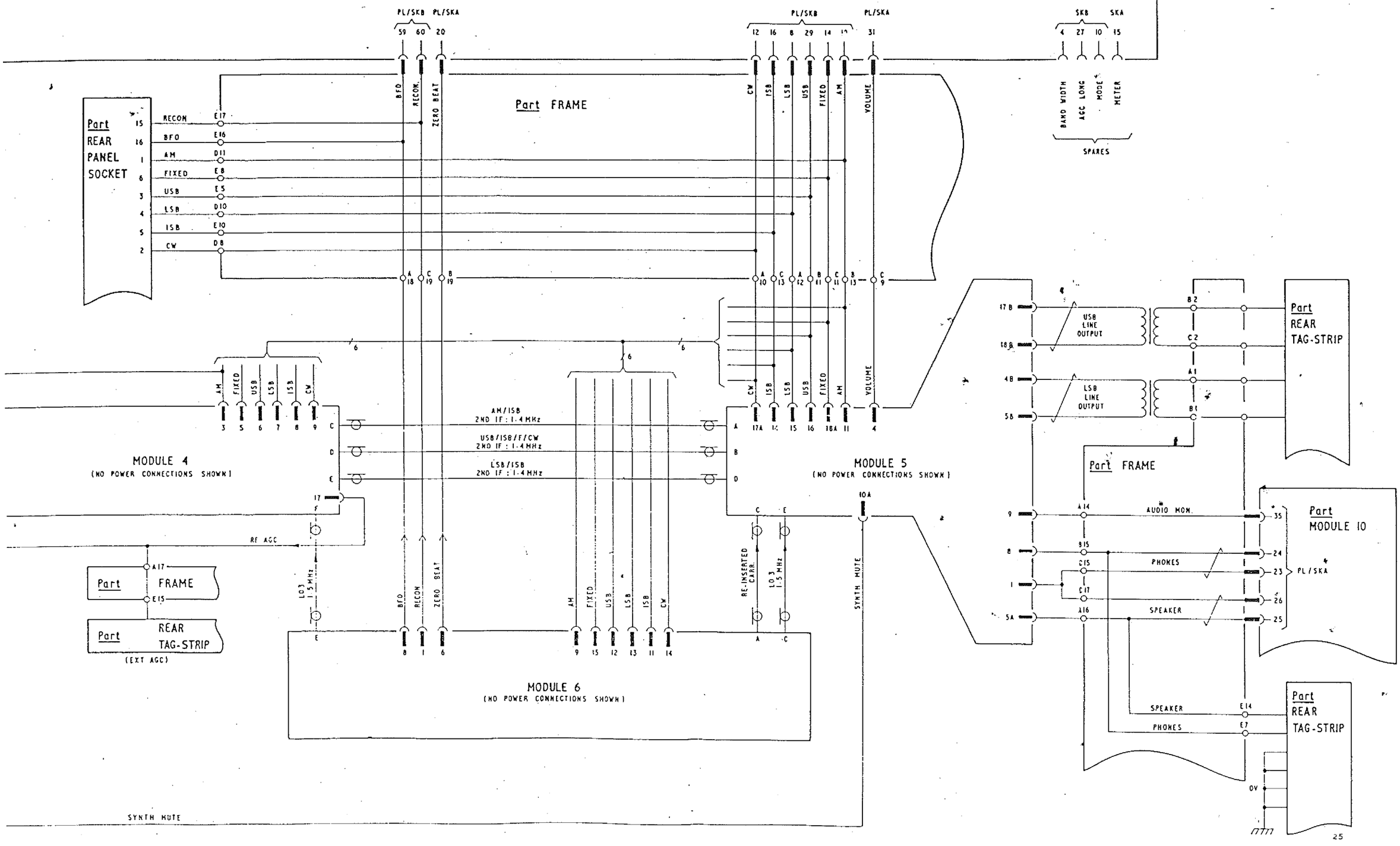


PR2250 INTERCONNECTION DIAGRAM (d)

FIG 2

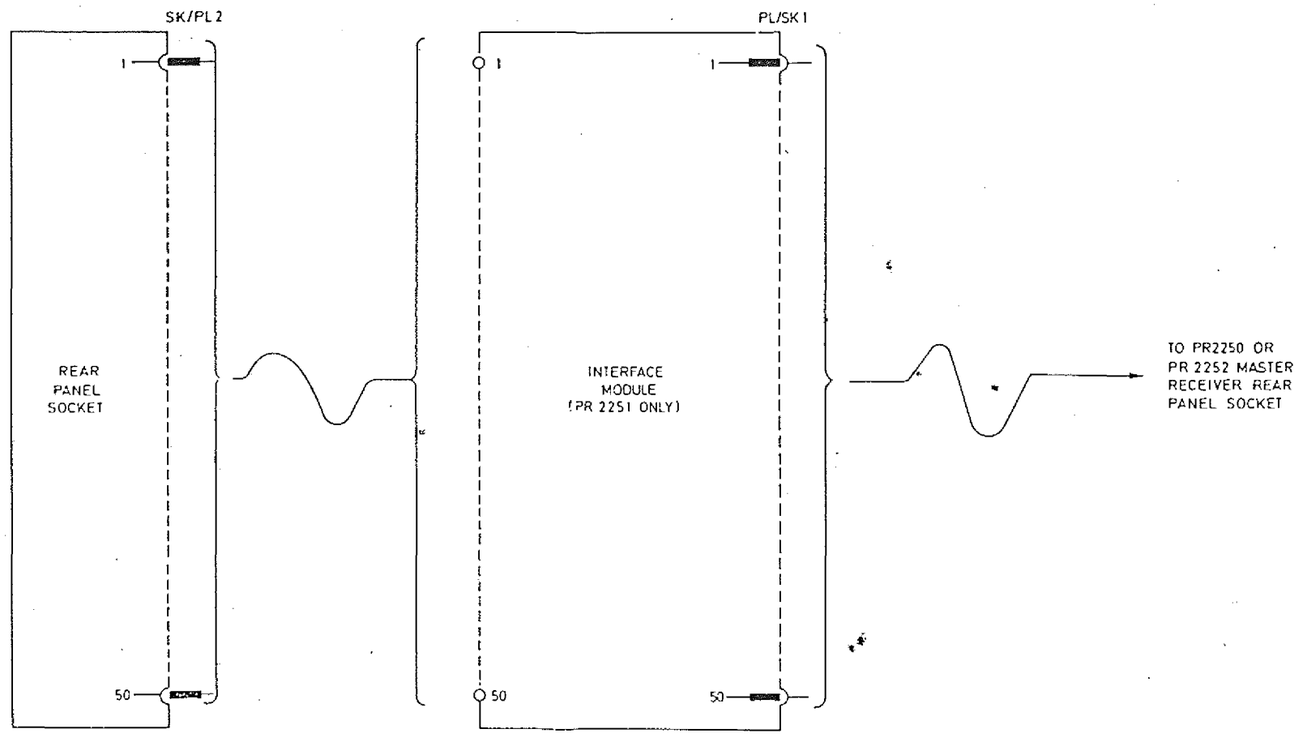
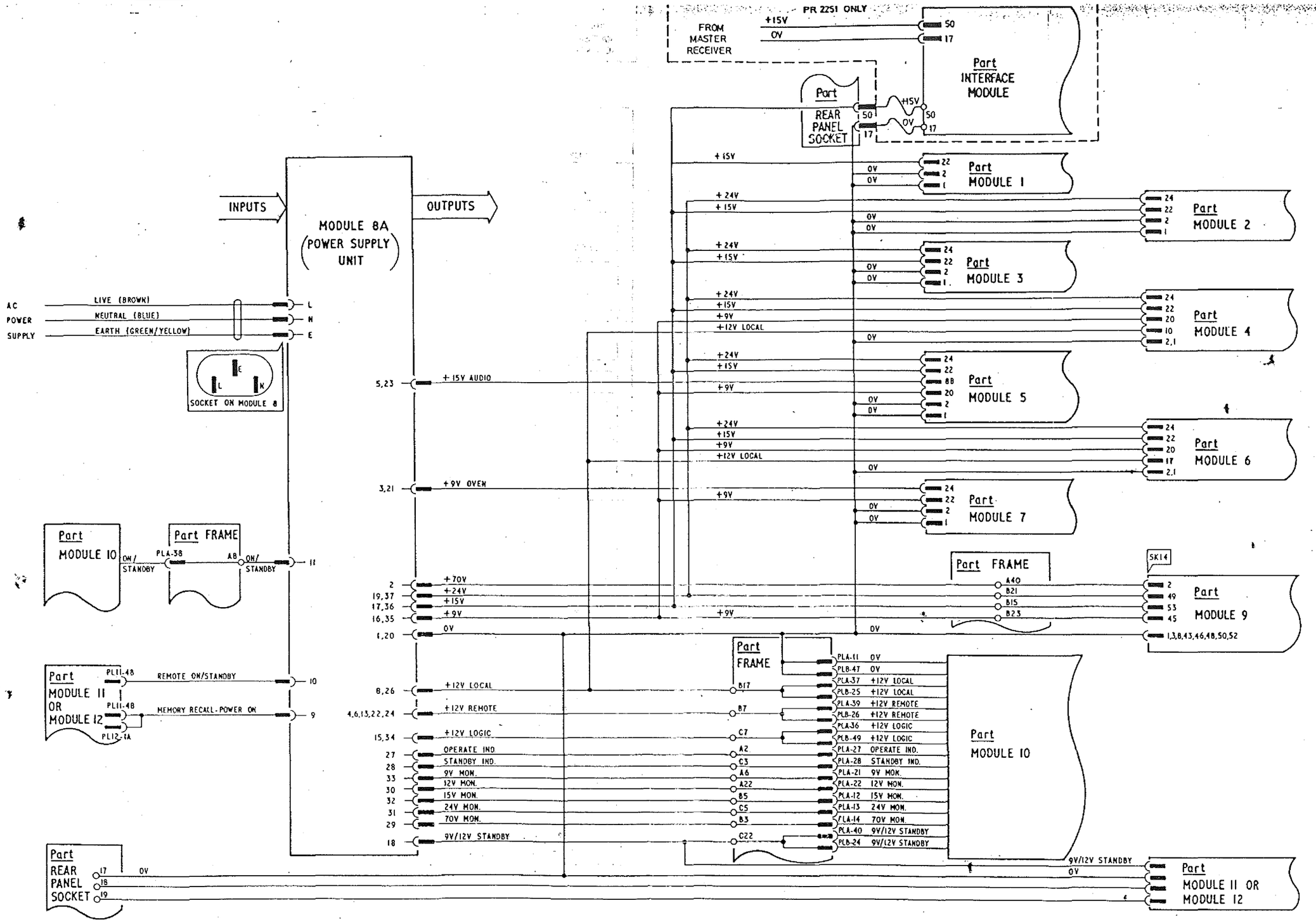


FIG. 3 PR2251 INTERCONNECTION DIAGRAM - INTERFACE MODULE



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PR2250 INTERCONNECTION DIAGRAM-POWER SUPPLIES

FIG 4