memoryscan™

ms — 1
ms — 2

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SERVICE MANUAL

TENNELEC

customer service
orangeburg, s.c.

Bill Hall

INCL. 7 SCHEMATICS

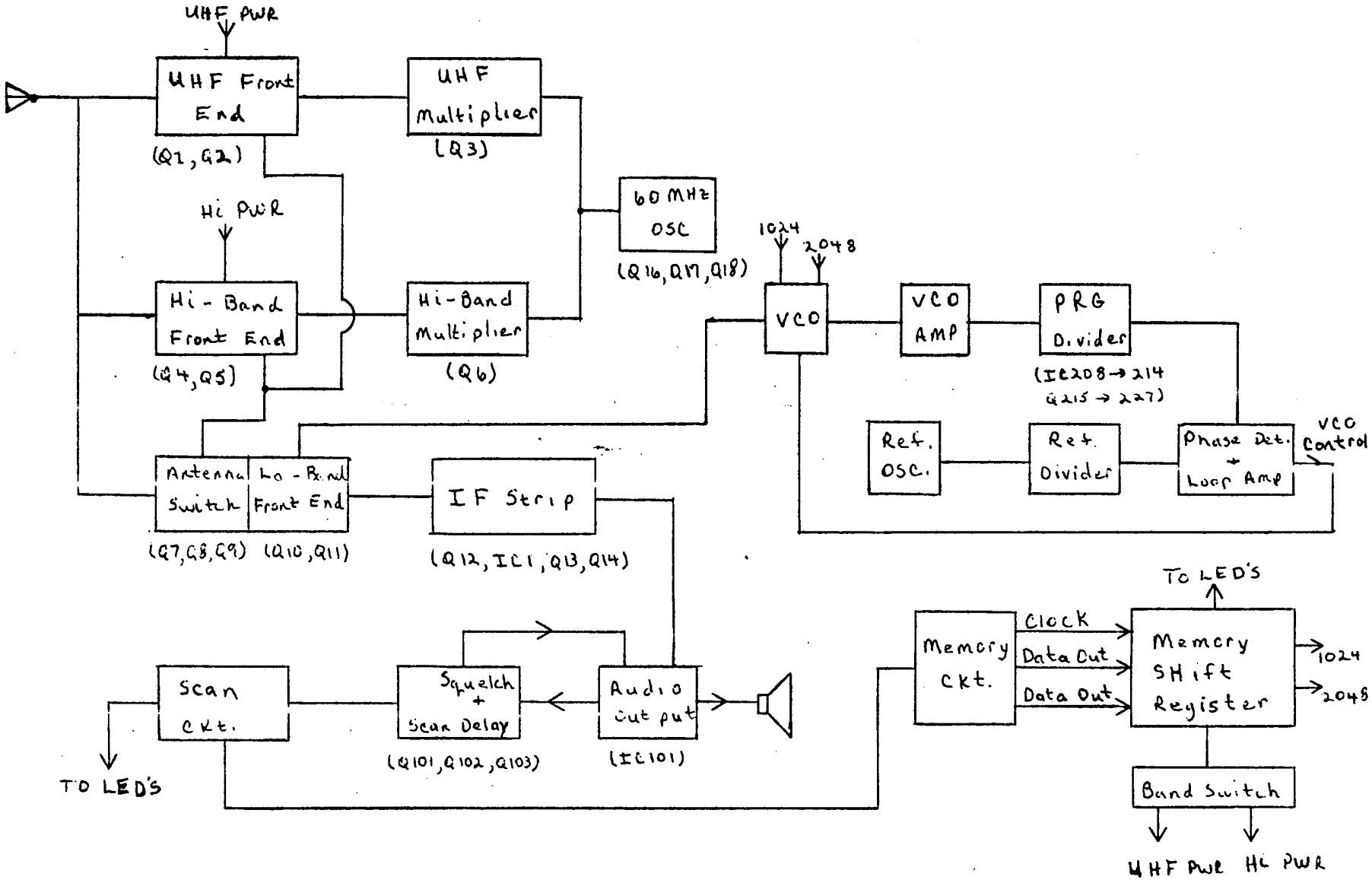

Figure 1: Block Diagram

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TENNELEC MEMORYSCAN

CIRCUIT DESCRIPTION

I. IF/RF Board MS-2

A. Power Supply

The power supply generates six separate voltages for the circuits in the scanner. These voltages are: +13V, +9V, +5V to Pin 5 of IC106, -6V to Pin 8 of IC106, -6V to Pin 4 of IC106. The +13V is used to produce all the other voltages and to power the audio amplifier. The +9V powers all RF circuits, the 10.245 MHz oscillator, and the squelch circuit. The +5V powers all logic circuits except for the memory. The +5V to Pin 5, -6V to Pin 8, and -6V to Pin 4 of IC106 all power the memory. These three voltages keep the memory activated even with the power switch off.

The +13 is generated by the center-tapped secondary of T1 and rectifier diodes CR15 and CR16. C89 and C90 are the +13V filters. Nominal ripple is 2V p-p at 120 Hz. When the power switch is on the +9V and +5V are generated. The Q25 circuit is a +9V regulator with 9V zener diode VR3 setting the reference for the +9V. Nominal ripple is 10mV p-p at 120 Hz. The Q24 circuit is a +5V series voltage regulator, where 5V zener diode VR1 sets the reference for the +5 supply. C91 prevents degenerative feedback. R72, CR18, and CR19 provide the correct bias for Q24. Nominal ripple is 50mV p-p at 120 Hz.

The +5V to Pin 5 of IC106 is produced by the 5V zener diode VR1. The zener is fed by the +13V before the power switch thru a 470-ohm R70. Diode CR21 isolates the battery from VR1 when the unit is not connected to the AC line. The -6V to Pin 4 of IC106 is generated by a half-wave rectifier CR17 fed from one side of the secondary of T1. The voltage is filtered by C92 and fed thru a 470-ohm R71 to 6.8V zener diode VR2. The -6V to Pin 8 of IC106 is derived from this voltage by CR23. Nominal ripple is 15mV at 120 Hz for the -6V to Pin 4 and 10mV at 120 Hz for the -6V to Pin 8 of IC106.

The nine-volt battery is present to furnish keep-alive power to the memory when the unit is not connected to the AC line. When the unit is connected to the AC line, the voltage between the anode of CR22 and the anode of CR23 is greater than nine-volts and thus keeps CR22 reverse biased. When the unit is not connected to the AC line, the battery takes over the supplies a voltage across these two points to keep the memory activated. C97 and C98 ensure a smooth voltage transition. The +5 to Pin 5 of IC106 is not necessary to keep the memory alive. In keep

A. Power Supply (continued)

alive condition, the battery has to supply approximately 3-4mA.

For mobile operation, a separate mobile power convertor supplies the +13V, and a negative voltage to power zener VR2.

B. Antenna Switching Circuit

Q7, Q8, and Q9 form the antenna switching circuit. The purpose of this circuit is to connect the low band front end either to the outside antenna or to the High or UHF band convertors. When the low band is connected to the convertors, good isolation is required between it and the outside antenna.

The operation of this circuit is as follows: When the unit is programmed for a low band frequency, the voltage on the base of Q7 is near zero and Q7 is therefore off. The voltage on the base Q8 is set at approximately 2.6V. This puts the emitter at about 2V. The voltage on its collector will also be about 2V, so the transistor is allowed to saturate. With the base-emitter junction acting as a diode junction, the signal will appear on Q8's emitter and therefore on the input of the low band front end. Also, Q9 is saturated and therefore CR1 and CR3 are reverse biased to keep any signals from being impressed on the low band from the High or UHF band front ends.

If the unit is programmed for the High or UHF band, about o.6V will appear on the base of Q7. With 0 volts on the emitter and collector, Q7 is allowed to saturate. This action will reverse bias the base-emitter junction of Q8, cutting it off, and at the same time cutting Q9 off. Therefore, resulting in good isolation between the low band front end and the antenna terminal when the unit is not programmed for low band. At the same time Q7 acts as an emitter follower to transfer the convertor outputs to the low band front end input.

C. Low Band Front End

The low band front end amplifies signals in the 30 to 50 MHz range and converts them down to the 10.7 MHz IF. Q10 is an RF amplifier which, in conjunction with L14, L15, L16 and their associated capacitors, amplifies the signal and determines the range of signals to be amplified. L14, L15, and their associated capacitors form a preset bandpass filter. L16 is adjusted using a sweep generator to give an accurate picture of the response curve of the front end. After the signal is amplified by Q10, it is applied to gate 1 of Q11 and mixed with the signal from the Voltage Controlled Oscillator, which is applied to gate 2 of Q11, to produce the 10.7 MHz IF at Q11's drain. The VCO is the first local oscillator and its frequency is on the low side (10.7 MHz below) the desired signal frequency. The low band front end uses single conversion

C. Low Band Front End (continued)

while the high band and UHF front ends use dual conversion with the low band section acting as an IF section along with the 10.7 MHz IF.

D. Voltage Controlled Oscillator (VCO)

The purpose of the VCO is to determine the frequency that the scanner will receive. The VCO is set up for low side injection, that is the VCO runs 10.7 MHz below the desired signal frequency. The specified range covered by the VCO is 20.48 MHz to 39.3 MHz corresponding to signal frequencies of 31.18 MHz to 50.0 MHz. The VCO frequency is controlled by the parameters of the Phase-Locked Loop in which it operates and the VCO frequency is phase-locked to a reference oscillator. For purposes of this explanation, the VCO frequency is controlled by a DC voltage applied to CR10 (Varicap Diode) thru R62.

The oscillator itself is Q20 operating in a standard Colpitts configuration. The components which determine its frequency are C81, CR10, and inductors L23, L24, and L25. CR10 is a special diode called a varicap or varactor. It has the property that when reverse biased, its capacitance varies with applied voltage. By varying the varactor voltage, then, the frequency of the oscillator can be varied. Since the capacitance will vary over a limited range, switchable inductors are used to cover the 20 MHz range that the oscillator must swing. For the 20 to 26 MHz range, L23, L24, and L25 are in series, and Q22 and Q23 are off. When a frequency in the 26 to 30 MHz range is to be generated, the 1024th bit of the program will be true. This turns on Q22, which shorts the junction of L24 and L25 to ground. This action removes L25 from the total inductance, thus lowering the total inductance and causing the generated frequency to be higher for a given value of capacitance of CR10. For a frequency value between 30 and 40 MHz, the 2048th bit will be true, turning on Q23 and removing all inductors except L23 from the circuit.

To keep the oscillator output constant over the frequency range, an Automatic Gain Control (AGC) circuit is used. Q19 is an emitter follower used to isolate the oscillator from all loads. The emitter follower drives rectifiers CR8 and CR9 thru C79. These rectify the negative lobes of the oscillator output and apply this voltage to the base of Q21, which is normally biased on by R59. Any increase in output amplitude tends to cut off Q21, thus decreasing the current thru Q20. As the current thru Q20 is reduced, the amplitude of oscillation drops.

Emitter follower Q19 also drives the programmable counter and Q15, which also acts as a buffer amp. Q15 furnishes local oscillator injection to the low band mixer.

E. IF Strip

The MS-2 has a common IF strip and detector for all bands. The IF strip consists of the following active devices: Q12, IF amp, IC1, IF amp and detector, Q13 and Q14, audio preamp.

The signal at the first IF of 10.7 MHz is derived from the drain of Q11 (low band mixer) and is applied to base of Q12 thru an IF transformer L18 and a 10.7 MHz crystal filter FL1. L18 is adjusted for maximum output. Q12 is the first IF amplifier. The output of the amplifier is fed thru a 10.7 MHz crystal filter FL2 to the input of IC1 where it is additionally amplified and fed to a quadrature detector internal to IC1. L26 is the tuned circuit of the detector.

The audio output appears on Pin 1 of IC1 and is fed to the base of Q13 thru R81 and C64. Q13 and Q14 form an audio preamp circuit. The audio is then applied to the squelch and audio power amp circuits.

F. 60 MHz Oscillator

Q17 is a crystal controlled oscillator at 60 MHz. The major frequency determining components of the oscillator are C68, L22, C71, and Y1. To keep the oscillator output constant an AGC circuit is used and operates on the same principles as the AGC circuit for the VCO. Q16 is the buffer amp and Q18 is the AGC transistor. The emitter of Q16 feeds either Q6 (High Band Multiplier), a doubler which amplifies the 120 MHz harmonic to mix with the VHF high band signals or Q3 (UHF multiplier) which amplifies the 420 MHz harmonic to mix with the UHF signals. The oscillator Q17 is powered only when either high or UHF bands are programmed. The multipliers, Q3 and Q6 are powered only when their respective bands are programmed.

G. UHF Front End

The UHF front end consists of RF amplifier Q1 and Mixer Q2. The mixer mixes the 420 MHz convertor oscillator signal with UHF signals in the range of 450 to 470 MHz to obtain a 30 to 50 MHz low band signal. To receive signals in the 490 to 510 MHz range, Q3's tank circuit is retuned to amplify the 540 MHz harmonic of the convertor oscillator.

H. High Band Front End

The high band front end consists of RF amplifier Q4 and Mixer Q5. The mixer mixes the 120 MHz signal from the convertor oscillator with high band signals in the range of 150 to 170 MHz to obtain a 30 to 50 MHz low band signal. To receive signals in the 146 to 148 MHz range, these signals are mixed with the 120 MHz

H. High Band Front End (continued)

to obtain 26 to 28 MHz. High side injection of the VCO is then used in the low band front end to receive these signals.

II. IF/RF Board MS-1

/. Power Supply

The Power Supply generates six separate voltages for the circuits in the scanner. These voltage points are marked A thru F on the schematic. The nominal voltages for these points are as follows: A=13.5, B=9, C=5, D=5, E=-6.* The circuit uses for these voltages follows: A is used to generate most of the other voltages and to power the audio amplifier. B powers all RF circuits. C powers all logic circuits except for the memory. D is the positive voltage for the memory and stays on even when the power switch is off. E and F are the negative voltages for the memory. These also stay on when the power switch is off.

Voltage A is generated by the center-tapped secondary of T1 and D313 and D314. C383 and C384 are the filters for A. The nominal ripple is 2V p-p @ 120Hz. When the power switch is on, B and C are generated. B is generated by D320, a nine-volt zener which is fed by two 33-ohm resistors R372 A&B from voltage A. Ripple on B is 50mV p-p nom. @ 120Hz. Voltage C is simply dropped from A by series resistor R371. No zener regulation is used. Nominal ripple is 50mV p-p @ 120Hz.

Voltage D is produced by the five-volt zener D319. The zener is fed by A before the power switch thru a 470-ohm R370. Diode D318 isolates the battery from D319 when the unit is unplugged from the wall. Voltage E is generated by a half-wave rectifier D312 fed from one side of the secondary of T1. The voltag is filtered by C380 and fed thru a 470-ohm R369 to 6.8-vol zener D315. The voltage at F is derived from E by diode D316.

The nine-volt battery is present to furnish keep-alive power to the memory when the unit is not plugged into the wall. When the unit is plugged in, the voltage between D and F is greater than nine-volts and thus keeps D317 reverse biased. When the unit is unplugged from the wall, the battery takes over and supplies a voltage across D and F to keep the memory alive. Caps C381 and C382 ensure a smooth voltage transition. Voltage E is not necessary to keep the memory alive. In keep-alive condition, the battery has to supply approximately 3 to 4m .

For mobile operation, a separate mobile power convertor supplies +13V to A, and negative voltage to power zener D3 5.

* F=-6

B. Antenna Switching Circuit

Q308, Q309, and Q310 form the antenna switching circuit. The purpose of this circuit is to connect the low band front end either to the outside antenna or to the High or UHF band convertors. When the low band is connected to the convertors, good isolation is required between it and the outside antenna.

The operation of this circuit is as follows: when the unit is programmed for a low band frequency, the voltage on the base of Q308 is near zero and Q308 is therefore off. The voltage on the base of Q309 is set at approximately 2.6V by the voltage divider R331 and R332. This puts the emitter at about 2.0V. The transistor is allowed to saturate, so the voltage on its collector will be about 2V also. Since the transistor is saturated and its base is free to move, a signal impressed on its collector will appear at its emitter also. The antenna is connected to the collector of Q309 so that any signals appearing at the antenna terminal will appear on Q309's emitter and therefore on the input of the low band front end.

If the unit is programmed for High or UHF band, however, a large voltage will appear on the base of Q308. This action will reverse bias the emitter-base junction of Q309, cutting it off, and at the same time turn on Q310 thru the voltage divider R328 and R329. When Q310 turns on, it clamps the base of Q309 to ground. The base of Q309 then acts as a shield between collector and emitter, reducing the stray capacitance between those two points. This circuit results in about 60db of isolation between the low band front end and the antenna terminal when the unit is not programmed for low band. At the same time, Q308 acts as an emitter follower to transfer the convertor outputs to the low band front end input.

C. Low Band Front End

The Low Band Front End amplifies signals in the 30 to 50 MHz range and converts them down to the 10.7 MHz IF. Q311 is an RF amplifier which, in conjunction with L315, L316, L317 and their associated capacitors, amplifies the signal and determines the range of signals to be amplified. L315, L316, and L317 are adjusted using a sweep generator to give an accurate picture of the response curve of the front end. After the signal is amplified by Q311, it is mixed in Q312 with the signal from the Voltage Controlled Oscillator (VCO) to produce the IF of 10.7 MHz at Q312's collector. The VCO is the first local oscillator and its frequency is on the low side (10.7 MHz below) the desired signal frequency.

D. IF Strip

The MS-1 has a common IF strip and detector for all bands. The IF strip consists of the following active devices: IC301, IF amp and Detector; Q315, IF amp and mixer; Q313, IF amp; and Q314, IF amp.

The signal at the first IF of 10.7 MHz is derived from the collector of Q312 (LO band mixer) and is applied to the base of Q314 thru an IF transformer L318. L318 is adjusted for maximum output. Q314 is in a dc feedback configuration and obtains its bias from the cold side of L318 secondary. This point is bypassed by C351. Q313 is an emitter follower dc coupled to the collector of Q314. Its purpose is to drive the 10.7 MHz ceramic filter without loading the collector of Q314. Q315 is also in a dc feedback configuration with the feedback resistor (R349 and R350) split and bypassed by C356 to increase the gain. The second local oscillator frequency of either 10.245 MHz or 11.155 MHz is applied to the base of Q315 thru R348. R348 in conjunction with C355 forms a low-pass filter to supress harmonics of the second local oscillator. Q315 mixes the 10.7 signal and the second local oscillator signal to produce a 455kHz signal at its collector. C358 removes most of the residual 10 MHz signal from Q315's collector, leaving the 455kHz to be applied to the 455kHz ceramic filter. The function of this filter is to establish the overall receiver bandwidth for good adjacent channel rejection. The purpose of the 10.7 MHz ceramic filter is to suppress the image that results when 10.7 MHz and the local oscillator are mixed. (If the second oscillator is 10.245 MHz, then both 10.7 MHz and 9.79 MHz at the input to the IF strip will produce a 455kHz output. The 9.79 MHz response is an undesired image, and is suppressed by the 10.7 MHz ceramic filter.)

The output of the 455 ceramic filter is fed to the input of IC301 where it is additionally amplified and fed to the quadrature detector internal to IC301. L319 is the tuned circuit of the detector, and is adjusted by applying a 10.7 MHz signal to the input of the IF strip, and adjusting (L319) for maximum 455kHz output as seen with a scope at Pin 11 of IC301.

The audio output appears on Pin 1 of IC301. R355 isolates the output of IC301 from the long wire run to the audio and squelch circuits to suppress oscillation.

E. 60 MHz Oscillator

Q305 is a crystal controlled oscillator at 60 MHz. Its emitter feeds Q304, a doubler which amplified the 120 MHz harmonic to mix with the High Band signal. The oscillator also drives Q303, a multiplier which amplifies the 420 MHz harmonic to mix with the UHF band. The oscillator Q305 is powered only when either High or UHF bands are programmed. The multipliers, Q303 and

E. 60 MHz Oscillator (continued)

Q304 are powered only when their respective bands are programmed.

F. Voltage Controlled Oscillator (VCO)

The purpose of the VCO is to determine the frequency that the scanner will receive. The VCO is set up for low side injection, that is the VCO runs 10.7 MHz below the expected signal frequency. The exact range covered by the VCO is 20.48 MHz to 39.3 MHz-corresponding to signal frequencies of 31.18 MHz to 50.0 MHz. The VCO frequency is controlled by the parameters of the Phase-Locked Loop in which it operates, and the VCO frequency is phase-locked to a reference oscillator. For purposes of this explanation, the VCO frequency is controlled by a dc voltage applied to D307 (varicap diode) thru R361.

The oscillator itself is Q317 operating in a standard Colpitts configuration. The components which determine its frequency are C372, D307 and inductors L321, L322, and L323. D307 is a special diode called a varicap. It has the property that when reverse biased, its capacitance varies with applied voltage. By varying the varicap voltage, then, the frequency of the oscillator can be varied. Since the capacitance will vary over a limited range, switchable inductors are used to cover the 20 MHz range that the oscillator must swing. For the 20 to 26 MHz range, L321, L322, and L323 are in series, and Q319 and Q320 are off. When a frequency in the 26 to 30 MHz range is to be generated, the 1024th bit of the program will be true (3.6V) This turns on Q319, which shorts the junction of L322 and L323 to ground. This action removes L323 from the total inductance, thus lowering the total inductance and causing the generated frequency to be higher for a given value of capacitance of D307. For a frequency value between 30 and 40 MHz, the 2048th bit will be true, turning on Q320 and removing all inductors except L321 from the circuit.

To keep the oscillator output constant over the whole frequency range, an Automatic Gain Control (AGC) circuit is used. Q316 is an emitter follower used to isolate the oscillator from all loads. The emitter follower drives rectifiers D305 and D306 thru C367. These rectify the negative lobes of the oscillator output and apply this voltage to the base of Q318, which is normally biased on by R358. Any increase in output amplitude tends to cut off Q318, thus decreasing the current thru Q317. As the current thru Q317 is reduced, the amplitude of oscillation drops.

Emitter follower Q316 also drives the programmable counter and furnishes local oscillator injection to the low band mixer.

G. UHF Front End

The UHF front end consists of RF amplifier Q301 and Mixer Q302. The mixer mixes the 420 MHz convertor oscillator signal with UHF signals in the range of 450 to 470 MHz to obtain a 30 to 50 MHz Lo band signal. To receive signals in the 490 to 510 MHz range, Q303's tank circuits are returned to amplify the 540 MHz harmonic of the convertor oscillator.

H. Hi Band Front End

The Hi band front end consists of an RF amplifier, Q306, and a mixer, Q307. The mixer mixes the 120 MHz signal from the convertor oscillator with Hi band signals in the range of 150 to 170 MHz to obtain a 30 to 50 MHz Lo band signal. To receive signals in the 146 to 148 MHz range, these signals are mixed with the 120 MHz to obtain 26 to 28 MHz. Hi side injection of the VCO is then used in the Lo band front end to receive these signals.

III. Logic Board

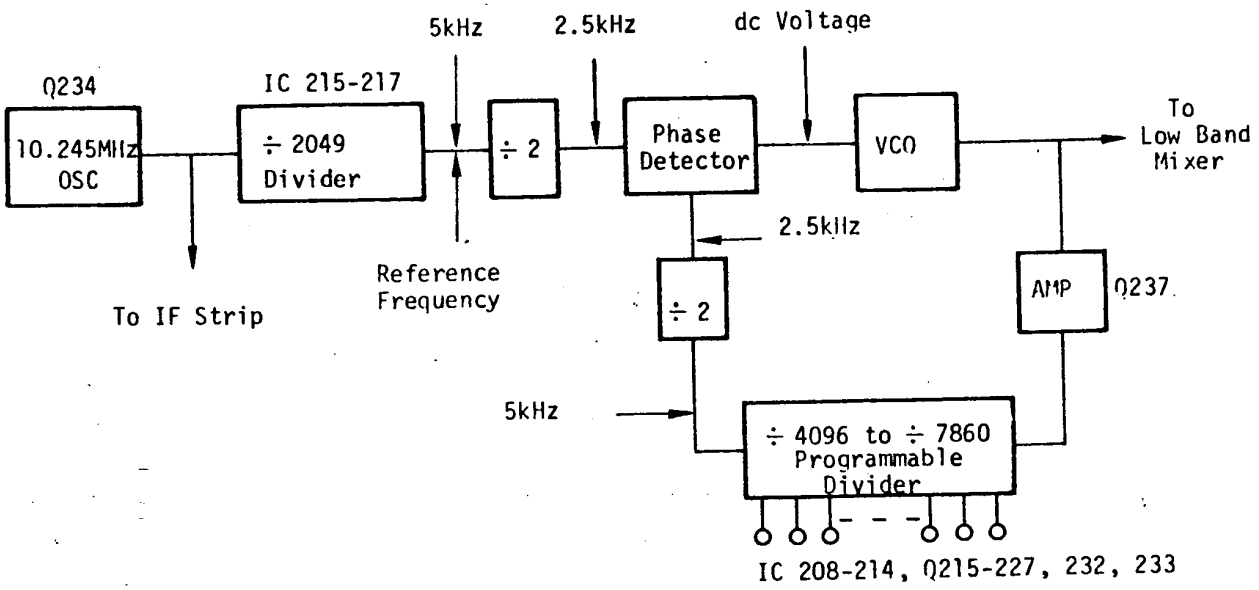


Figure 2: Phase Locked Loop Block Diagram

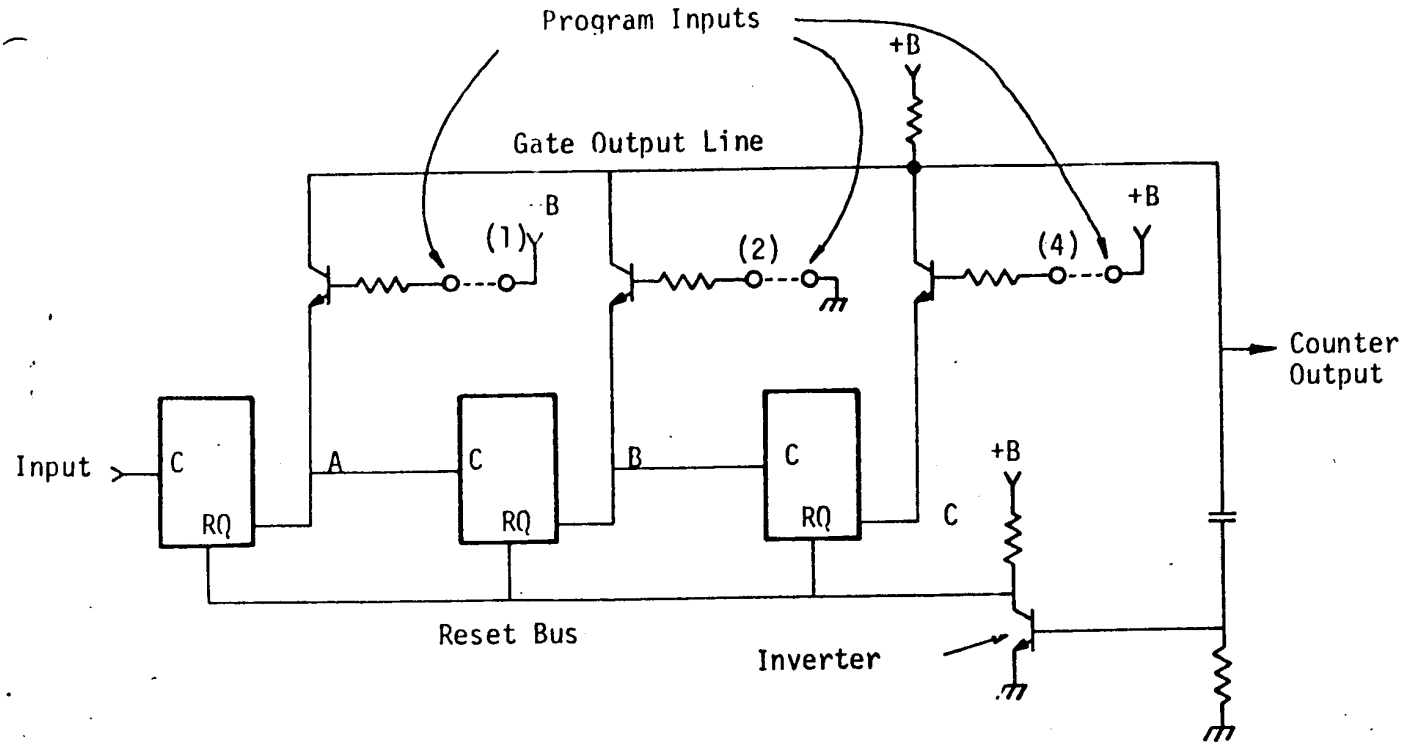
A. Phased-Locked Loop

Before describing in detail the various circuits on the logic board, it is best to understand the operation of the phase-locked loop from a block diagram standpoint. Figure 2 is

a block diagram of the phase-locked loop as used in the MS-1 & 2. The basic principle of the phase-locked loop (PLL) is that a free running oscillator is phase locked to a standard or reference frequency, and thereby acquires the stability and accuracy of the reference frequency. The phase locking is done with a phase detector which compares the phase of the reference frequency and the VCO frequency and develops a dc output voltage to make them equal in phase. Referring to Fig. 2, the reference oscillator operates at 10.245 MHz, and is the same oscillator used to mix the 10.7 MHz IF down to 455kHz. To develop the 2.5kHz reference frequency required by this application, the 10.245 MHz signal is divided by a factor of 4058. This division is accomplished by IC's 215, 216, 217, and 219. This 2.5kHz is supplied to one input of the phase detector, IC 218. The VCO on the RF Board is amplified by Q237 and fed to the programmable divider IC 208-214. The divider has its division factor controlled by the binary code on its programming lines. Thus, its division factor can be 8192 to 15720, depending on the binary input. The output of the divider is fed to the other input of the phase detector to be compared with the reference frequency. The output of the phase detector is a dc voltage which is fed to the VCO. This dc voltage controls the frequency of the VCO in response to the phase difference between the 2.5kHz reference and the divider output. For instance, if the VCO output frequency is too low so that the signal out of the divider lags the reference signal in phase, a high voltage will appear at the output of the phase detector which will cause the VCO frequency to increase, thus removing the phase error. The opposite will happen if the VCO frequency is too high. Since the frequency out of the programmable divider must always be 2.5kHz in phase and therefore equal in frequency to the 2.5kHz reference signal, it must always be 2.5kHz also. Now, since the output frequency is fixed, it is the input frequency to the divider or the VCO frequency that will change as the division factor is changed. Thus, the VCO frequency can be changed from 20.48 MHz (2.5kHz x 8192) to 39.3 MHz (2.5kHz x 15720). This change in frequency in 5kHz steps is what enables the MS-1 & 2 to tune 3764 frequencies in three bands for a total of 11,280 frequencies. The divider gets its binary code input from the memory, which delivers a new code to the divider each time that a channel is scanned.

B. Reference Frequency Oscillator

his oscillator Q234 operating at 10.245 MHz furnishes the reference frequency o the PLL and in the MS-1 only provides a signal to the IF for mix-down from 0.7 MHz to 455 KHz. It is a conventional Colpitts circuit with a frequency djustment, CV 201. This frequency adjustment determines the absolute a curacy of all channel frequencies fo the MS-1 & 2. An emitter-



Note: +B on program inputs (1) and (4) causes this counter to divide by 5.

Figure 3A: Simple programmable counter

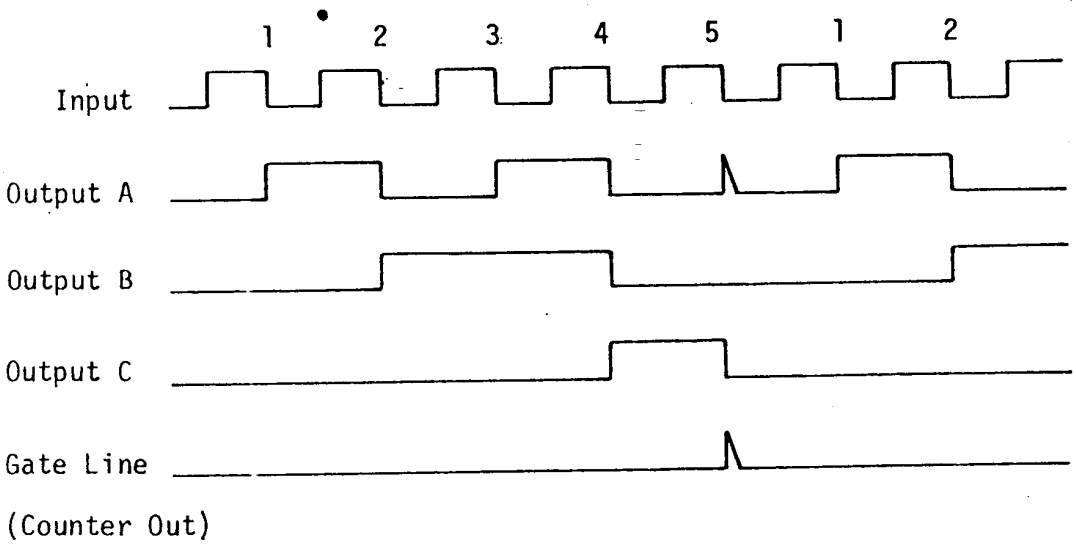


Figure 3B: Timing diagram

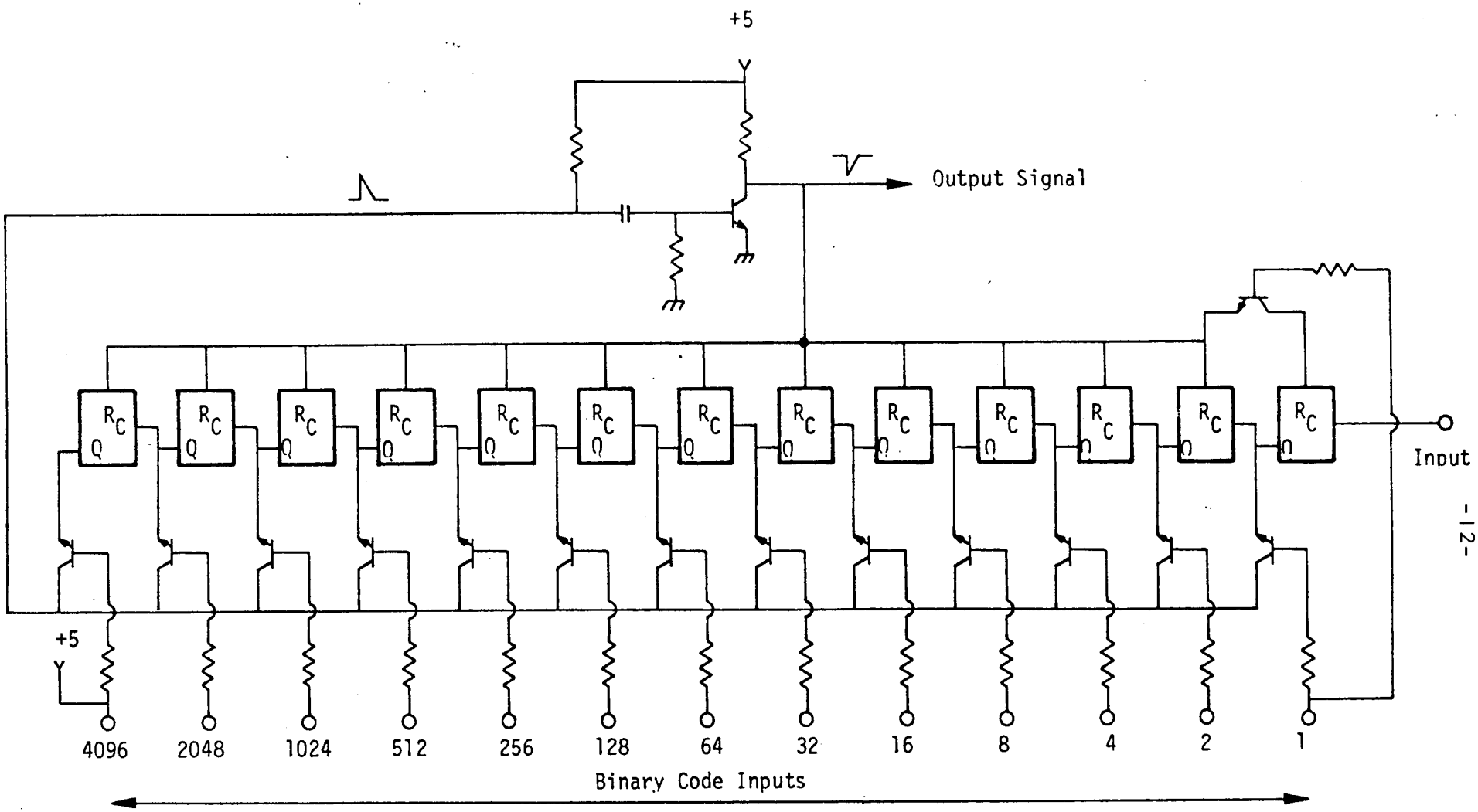


Figure 4: Programmable divider simplified circuit diagram

follower, Q235, drives the reference frequency divider circuit.

C. Reference Frequency Divider

This divider circuit consists of IC's 215, 216, 217, and 219, and is a fixed division factor of 4098 to produce the 2.5kHz reference frequency from 10.245 MHz, which is then applied to IC218. Its operation is similar to that of the programmable divider; see that section for the description.

D. Phase Detector

The Phase Detector consists of a single IC218. This is a commercially available IC having a phase detector and amplifier in the same package. The unit's operation as it is wired in our application is the following: the reference frequency is applied to Pin 1, and the variabel (VCO) frequency to Pin 8 and is routed to the VCO thru an emitter follower, Q236. If the phase of the signal at Pin 3 (frequency high is leading) that at Pin 1, the voltage at Pin 8 goes lower. If the phase at Pin 3 is lagging (frequency lower) that at Pin 1, the voltage at Pin 8 goes higher. Components C222, R248, R257, C221, R250, C225, R256, and C374 on board 3 determine the loops bancwidth and therefore the loop settling time.

E Programmable Divider

For operation of the programmable divider refer to the simplified diagram in Fig. 3. The principle is this: the counter operates until it counts to a number that equals the desired division factor, then it resets to zero and starts over again. In the example in Fig. 3 the transistors connected to the flip-flop outputs form an AND gate to sense the number five (4+1). When the count of five is reached, the gate output line goes positive and the reset bus goes to zero, resetting the counter. When the counter resets, the gate output line goes down immediately, resulting in a short spike on the gate output line and reset bus that serves as the output signal from the counter. This spike will occur at every fifth input pulse. Th change the division factor, we simply change the program inputs on the bases of the transistors. For example, if we want the counter to divide by three, we apply b+ voltage to inputs (1) and (2) and not (4).

The reference frequency divider described in paragraph B works exactly like this except that it is not programmable and, therefore, uses diodes in place of transistors.

The programmable counter as used in the MS-1 & 2 is shown in Fig.4. Its operation is identical to that of the simple counter shown in Fig. 3 except on a larger scale. The counter's programming inputs come from a shift register which is loaded by the memory

with a binary code each time a channel is scanned. The operation of this shift register will be described in detail in the memory description section.

IV. Front Panel Board

A. Audio Output Circuit

The audio is taken off the emitter of Q14 in the IF strip and applied to Volume Control RP1. From RP1, the audio is fed thru C107, R104, and R103 to Pin 6 of Audio Power Amplifier IC101. IC101 is an Operational Amplifier, where the associated resistors and capacitors are used to properly bias the chip and filter the audio. The audio output appears on Pin 8 and is fed thru C101 to the speaker. The speaker is an 8 ohm and is disabled when the external speaker jack is in use.

B. Squelch Circuit and Scan Delay

The Squelch and Scan Delay Circuits consist of Q101, Q102, and Q103. The noise is taken from one side of volume control RP1 and applied thru C108 and C109 (Hi-pass Filter) to the Squelch Control RP2. When RP2 is in the unsquelched position, the noise is allowed to pass thru to ground. With no noise at the base of Q101, the transistor does not amplify and thus Q102 is allowed to turn on. Therefore its collector is at ground potential. Its output is used to turn off the scan circuit. With Q102 turned on, Q103 is also turned on, which biases Pin 1 of IC101 and turns on the audio power amp. With Q103 turned on, C113 is charged.

When RP2 is in the squelched position, the noise is allowed to pass thru C110 to the base of Q101. Q101 is a noise amplifier; it amplifies only the high frequency noise. The noise is then negative rectified by D101 and D102. With a negative voltage on the base of Q102, it is allowed to turn off. Therefore, turning Q103 and IC101 off. With Q103 off C113 is allowed to slowly discharge causing a 2 second scan delay.

C. Scanning Circuit

With the unit in the squelched position and in the scan mode C115 is allowed to charge and discharge with respect to Q105 (after C113 has discharged to cretain level) causing a clocking action. The positive pulses at the output of the clock Q105 are applied to the base of Q104. Negative pulses appear on the collector of Q104. Negative pulses appear on the collector of Q104 which drives the Binary Counter IC102. The binary outputs of IC102 are applied to IC103 and IC104.

This logic sequentially places a ground potential on LED's I1 thru I16 sequentially turning them on causing a scanning action. The scan rate is 80 to 120 milli-seconds (or 8 to 12 channels per second). The scan rate cannot exceed 120 milli-seconds due to the settling time of the PLL IC218 Q107 is a switching transistor which allows IC103 and IC104 from being turned on at the same time. When a channel is locked-out, the biasing action on Q106 causes the clock to temporarily speed up making it appear to skip the channel completely.

D. Memory

The function of the memory is to store the codes that tell the PLL what frequency to produce. The memory has to store 16 different codes (one for each channel to be scanned). Each code contains 14 bits. The memory IC itself has 256 (16 x 16) memory locations (addresses) in which a 1 or 0 can be stored. Any storage location can be accessed by giving the memory a row address and a column address. The intersection point of those two addresses is the desired memory location. To save connections to the memory, the address inputs are 4-line binary which are decoded to 16-line inside the package. So to address any memory location, we must give the memory a row and a column address in binary form. The complete memory also contains a read/write control line and data input and output lines. Once a location has been addressed, the read/write line determines whether data will be written in or read out of that location.

With the unit in the Program Mode, +5V is applied to the "0" and "1" switches and therefore sets up the R/W line and data in line to the memory chip IC106. The output of Binary Counter IC102, which determines the channel location, is also applied to the Y-address determining the memory storage location of IC106. As the code is entered, clock pulses are applied to Pin 14 of Binary counter IC105 from clock Q109 thru inverter Q110 (one clock pulse per bit). The binary outputs of IC105 are applied to the X-address of IC106 which determines each bit of the location. The outputs of IC106 are applied to the Memory Shift Register (IC201 thru IC207), which in turn drives the respective LED's, distinguishing the proper code. Also, the output of Q110 is applied to wave shaping network Q111, Q112, and Q114 which is fed to the clock inputs of the Memory Shift Register.

V. Servicing

A. MS-1 and MS-2

1. Necessary Test Equipment

a.	OSCILLOSCOPE	50 MHz Tektronix 544 or equivalent
b.	SIGNAL GENERATOR	Measurements 801 or equivalent

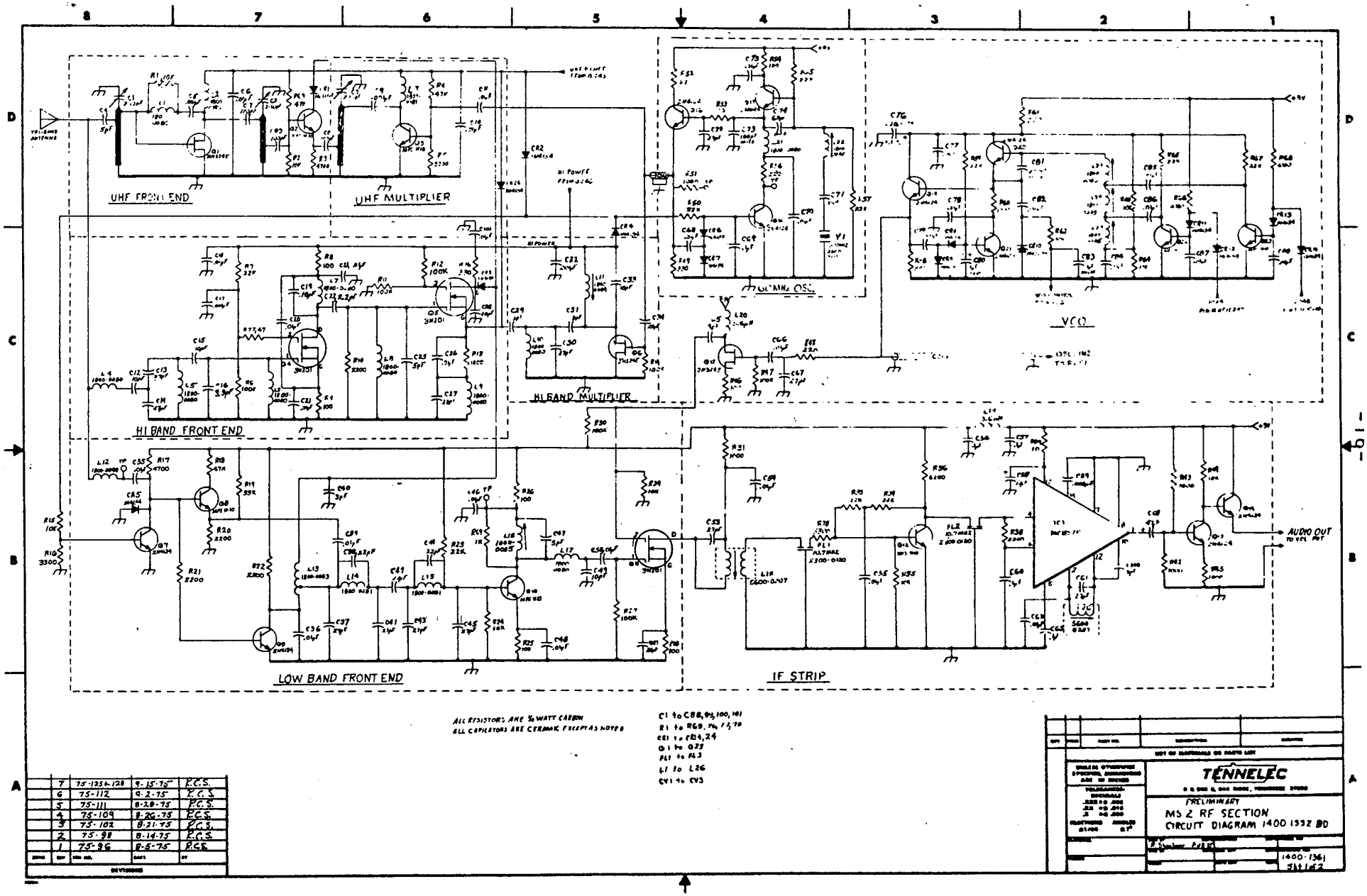
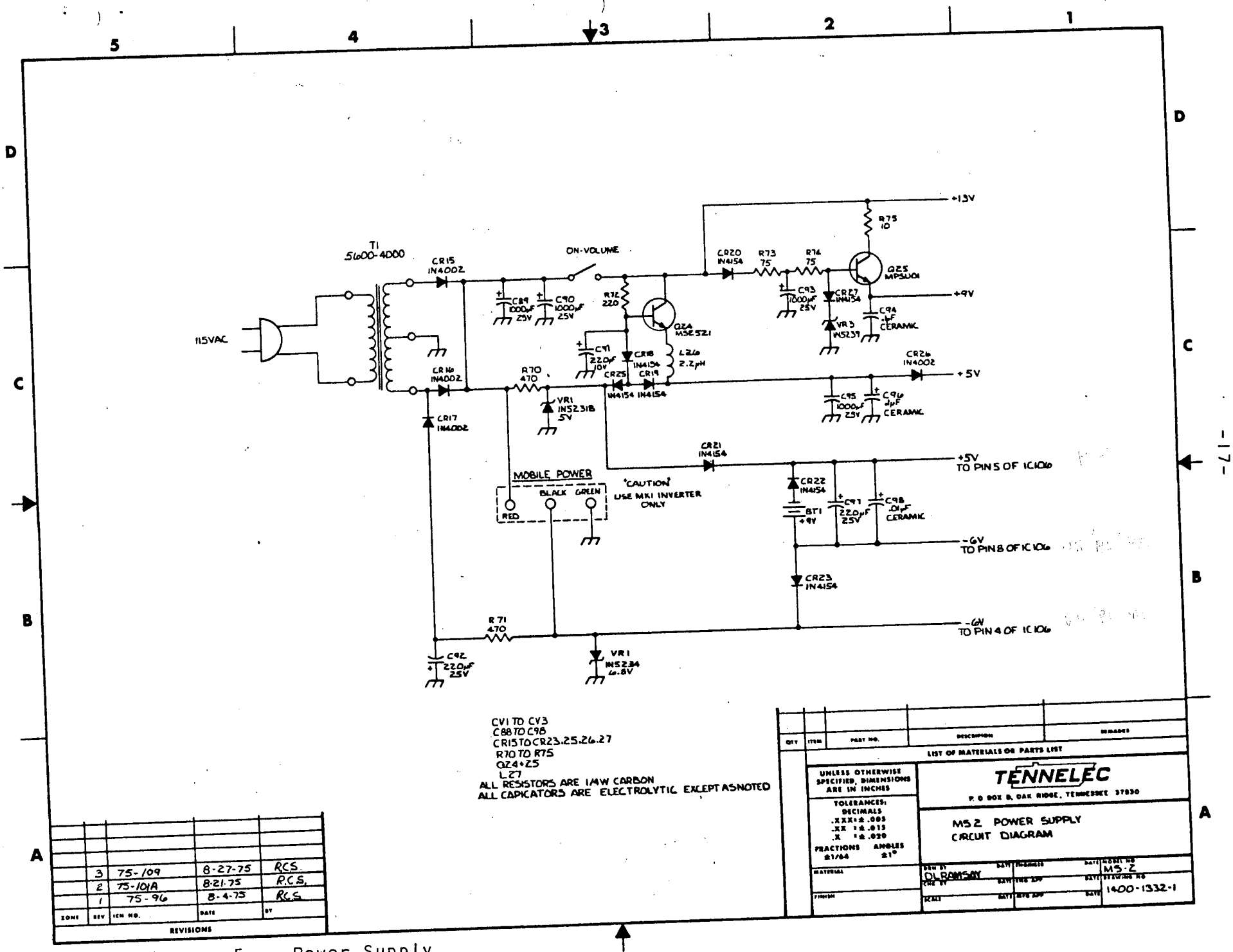


Figure 5: MS-2 IF/RF Circuit Diagram



CV1 TO CV3
C88 TO C98
CR15 TO CR23, 25, 26, 27
R70 TO R75
Q24 + Q25
L27
ALL RESISTORS ARE 1/4W CARBON
ALL CAPACITORS ARE ELECTROLYTIC EXCEPT AS NOTED

ZONE	REV	ECN NO.	DATE	BY
	3	75-109	8-27-75	RCS
	2	75-101A	8-21-75	R.C.S.
	1	75-96	8-4-75	RCS

REVISIONS

QTY	ITEM	PART NO.	DESCRIPTION	REMARKS

LIST OF MATERIALS OR PARTS LIST

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES

TOLERANCES:
DECIMALS
.XXX ± .005
.XX ± .015
.X ± .020
FRACTIONS ±1/64
ANGLES ±1°

MATERIAL

FINISH

TENNELEC
P. O. BOX 8, OAK RIDGE, TENNESSEE 37830

MS-2 POWER SUPPLY
CIRCUIT DIAGRAM

DRN BY D. L. RAMSAY DATE
CHK BY DATE
ENGR DATE
APVD DATE
SCALE DATE
MODEL NO MS-2
DRAWING NO 1400-1332-1

Figure 5a: Power Supply

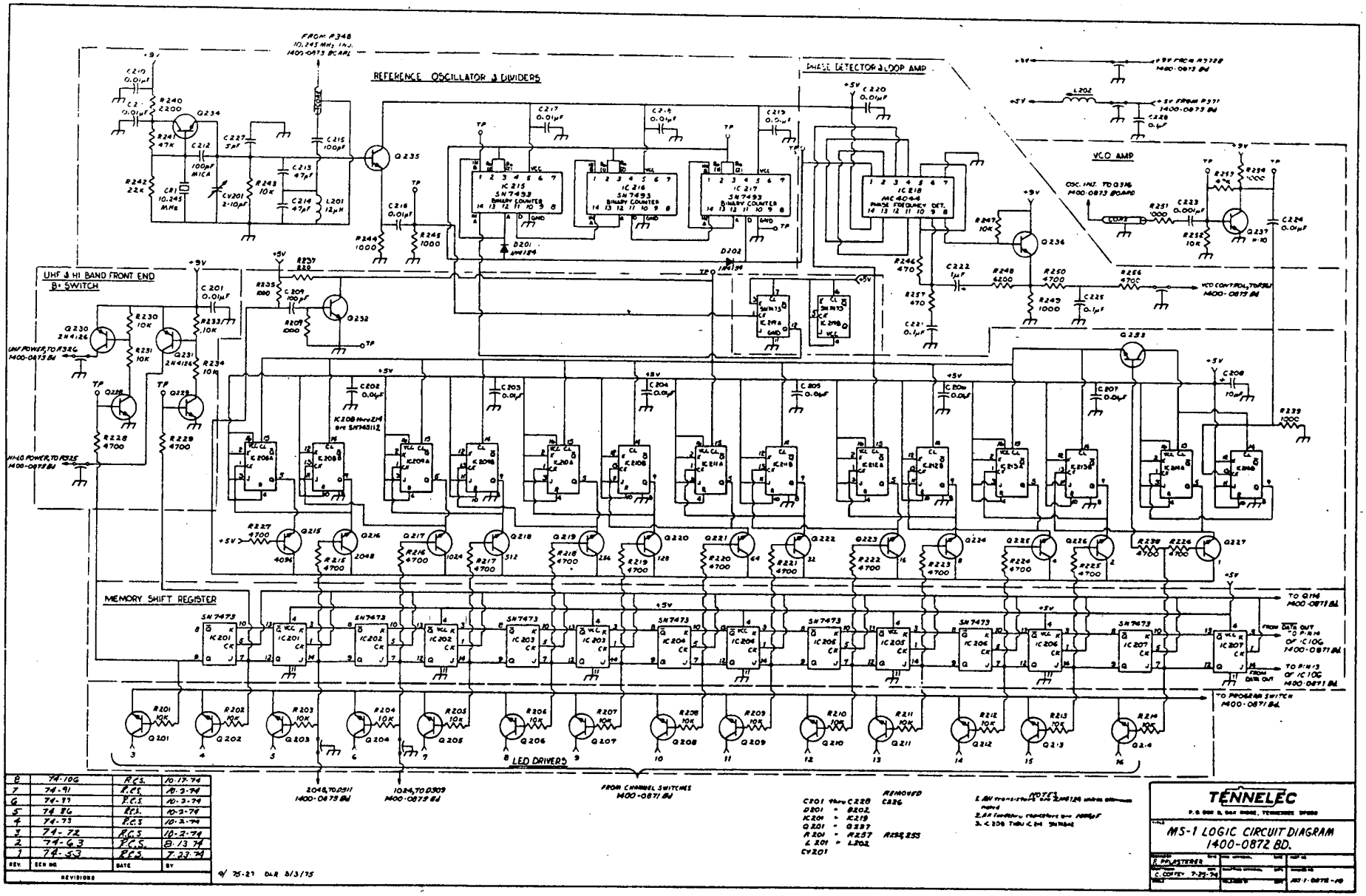


Figure 6: MS-1, MS-2 Logic Circuit Diagram

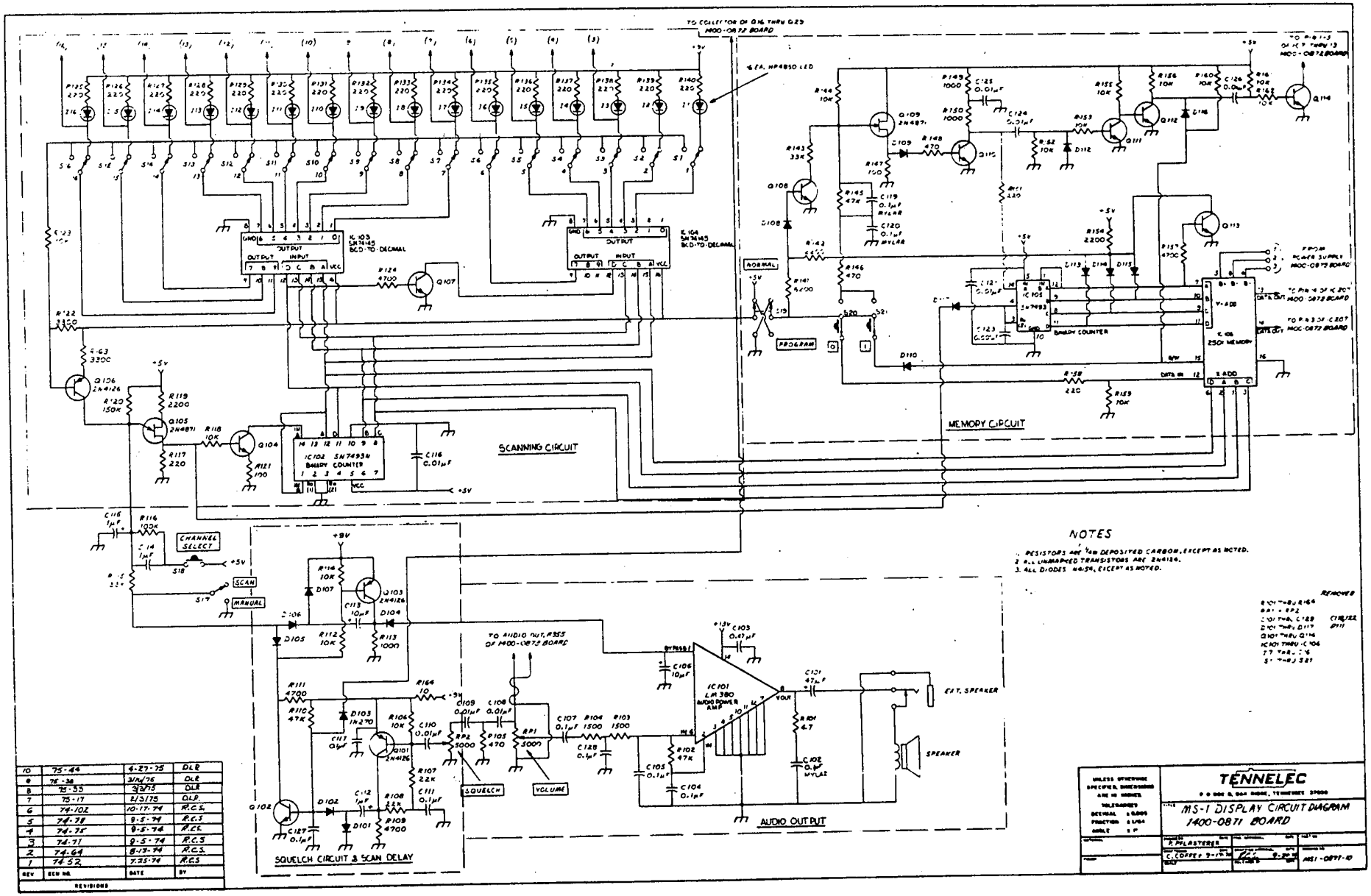


Figure 7: Front Panel Circuit Diagram

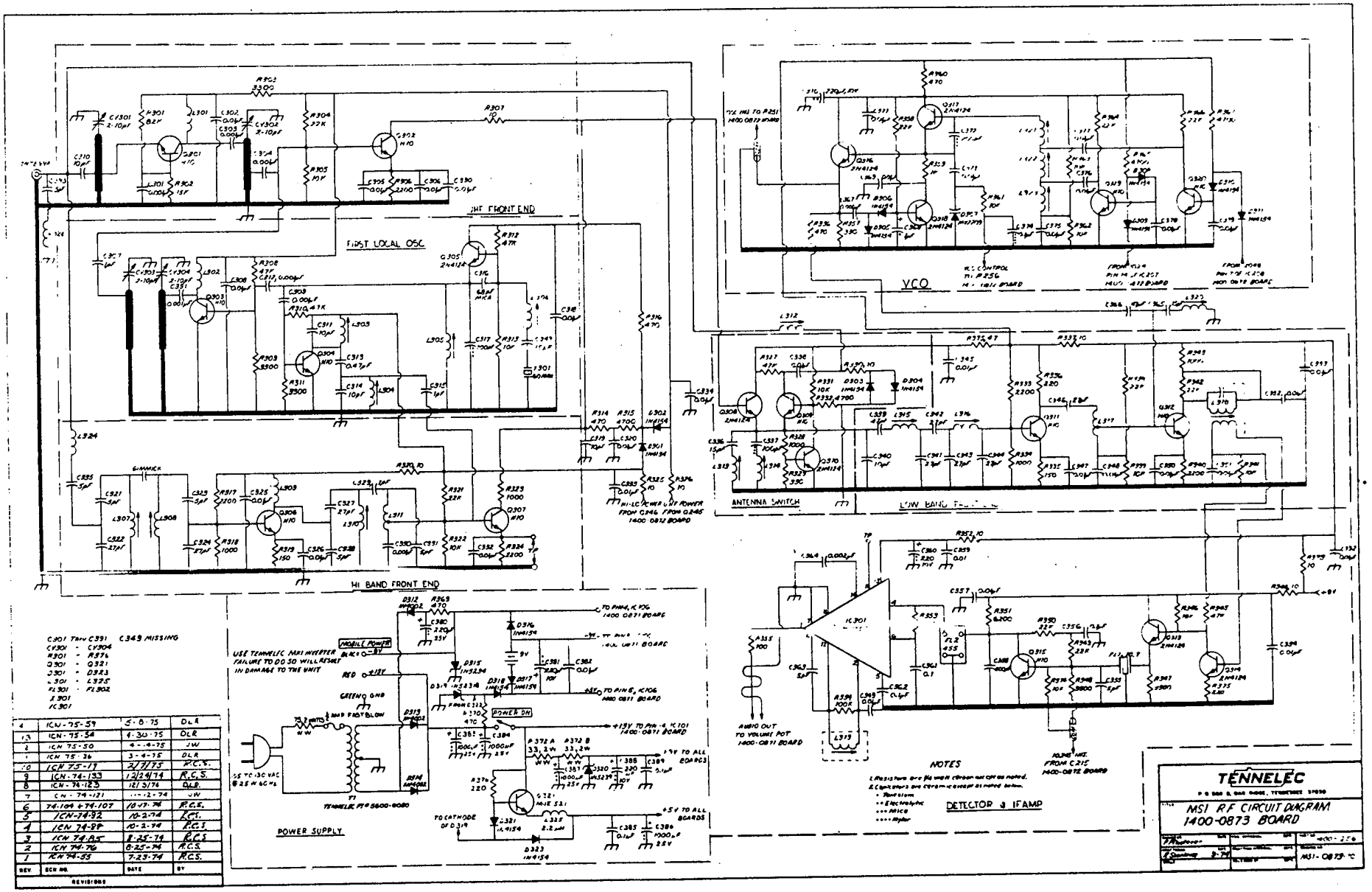
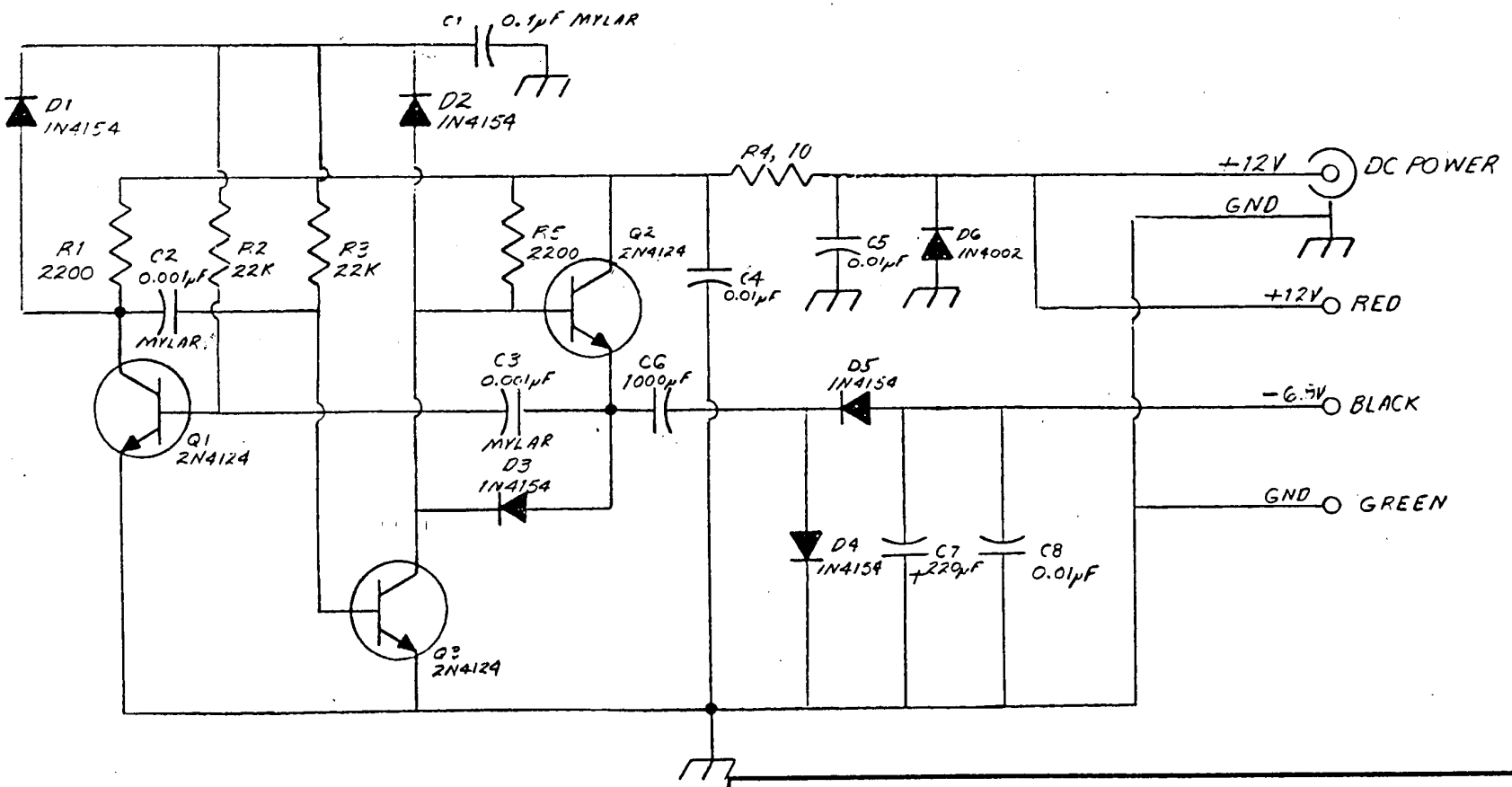


Figure 8: IF/RF Circuit Diagram (MS-1)



TENNELEC

P. O. BOX D, OAK RIDGE, TENNESSEE 37830

TITLE: MK1 MOBILE INVERTER					
ENGINEER	DATE	ENG. APPROVAL	DATE	PART NO.	
DRAFTSMAN R.C.S.	DATE 10-3-74	DRAFTING APPROVAL	DATE	DRAWING NO MK1-10	
SCALE		RELEASED BY	DATE		

Figure 9: MK-I Circuit Diagram

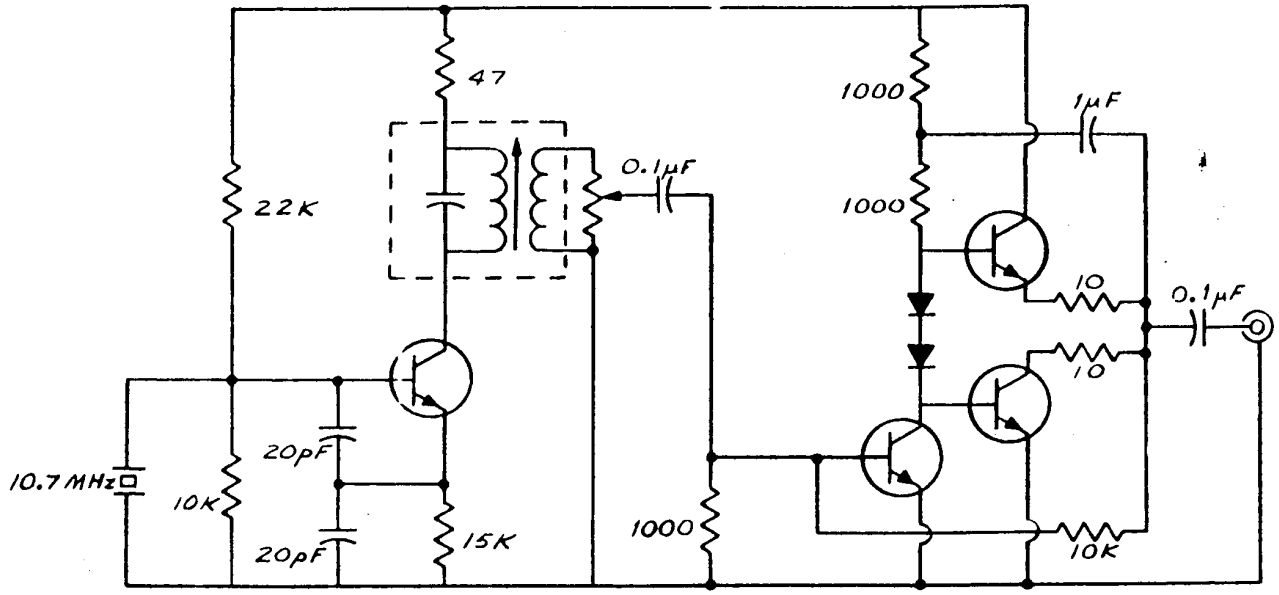


Figure 10: Suggested 10.7 MHz Generator

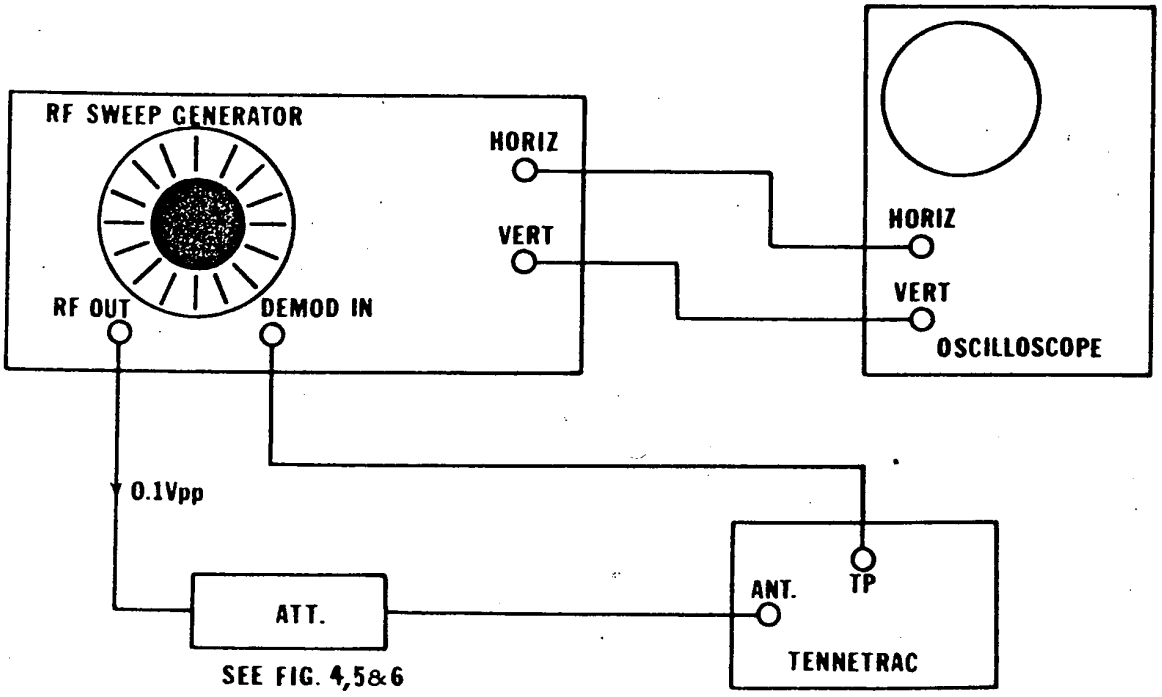


Figure 11: Test Set-Up

c.	SWEEP GENERATOR	Texscan VS-50M or equivalent
d.	AC VOLTMETER	H.P. 400D, 400E or equivalent
e.	DC VOLTMETER	20,000 ohms/V
f.	FREQUENCY COUNTER	60 MHz H.P. 5248L or equivalent
g.	DC SUPPLY	12V dc @ 1A
h.	10.7 MHz OSC.	See Fig. 10

2. Disassembly

Remove the four screws going through the woodgrained cabinet in the back, slide the cabinet off. To remove faceplate: loosen the four screws on the side of the chassis, remove the two screws extending through the control board into the faceplate and remove the faceplate. When removing the RF shields from the digital board use extreme caution to not bend or warp the shields.

3. Assembly

Care should be taken in assembling to not disturb any components. Note the four (4) 1000microF capacitors on the RF board, care should be exercised to not knock them over. Attention should be given to the battery cable during servicing - should the contacts touch any conductive portions of the unit, it will erase the memory.

4. 10.245 MHz Oscillator Alignment

Attach counter probe to Pin 1 of IC219. Adjust CV201 for 10.245 MHz ± 10 Hz. Check Pin of IC218 for 2.5 MHz.

5. VCO Alignment

Attach counter probe to emitter of Q319 (Q316 of MS-1), program a "1" in the #6 channel position, read 30.720 MHz. Ground collector Q232, adjust L23 (L321 in MS-1) for 40,000 MHz. Remove ground, ground pin 1 of IC218, counter should drop below 30 MHz, remove ground, program a "1" in channel 6. Ground collector Q232, adjust L24 (L322 in MS-1) for 31.5 MHz, remove ground, ground Pin 1 of IC218 counter should drop to 24.5 MHz or less. Remove ground, program all "0", adjust L25 (L323 in MS-1) for 26.500 MHz, remove ground. Ground Pin 1 of IC218, counter should drop to 19.8 MHz less. Replace shield.

B. MS-1 Only

1. IF Alignment

Program Channel 1 for a low band frequency: plug in AC line cord and turn on radio. Depress scan manual switch and push channel select until Channel 1 light comes on. Inject 33 mVpp of 10.7 MHz into the antenna jack. This 10.7 MHz must be ± 1 kHz. Move scope probe to Pin 11 of IC 2; you should see 455 kHz signal. Tune L319

to move blip to top of sinewave; tune L318 for maximum noise at speaker.

60 MHz Oscillator Alignment

2. RF Alignment

Connect the output of the sweep to antenna receptacle and demodulation input to the emitter of Q312. No additional detector is needed. See Fig. 11.

VHF Low

Program a low band frequency and place a small jumper across L312. Center trace at 40MHz. Tune L315, L316, and L317 to peak trace so 33 MHz and 40 MHz are approximately the same height.

3. Sensitivity

VHF Low

Program a low band frequency - Connect the output of a signal generator modulated 3 kHz with 400 Hz- to antenna receptacle. Turn output to minimum. Connect AC voltmeter between the speaker terminal and ground, connect a small jumper wire across L312. Turn squelch control fully clockwise. Turn volume control until voltmeter reads -10dBm. Set signal generator for 100 ohm V and tune until the signal is heard. Decrease signal level until voltmeter reads -20dBm. Retune signal generator for maximum reading on voltmeter. Decrease the signal level to .6 ohm V. Retune generator for maximum signal and set volume at -10dB. Turn off the modulation. The voltmeter should drop to -20dBM or below.

VHF High

Program a high band frequency - Remove the jumper wire from L312. Follow the procedure for VHF Low. When the modulation is switched off L303 and L304 may be tuned to improve sensitivity.

UHF

Program a UHF frequency - Remove the jumper wire from L312. Follow the procedure for VHF Low. When the modulation is switched off CV303 and CV304 may be tuned to improve sensitivity.

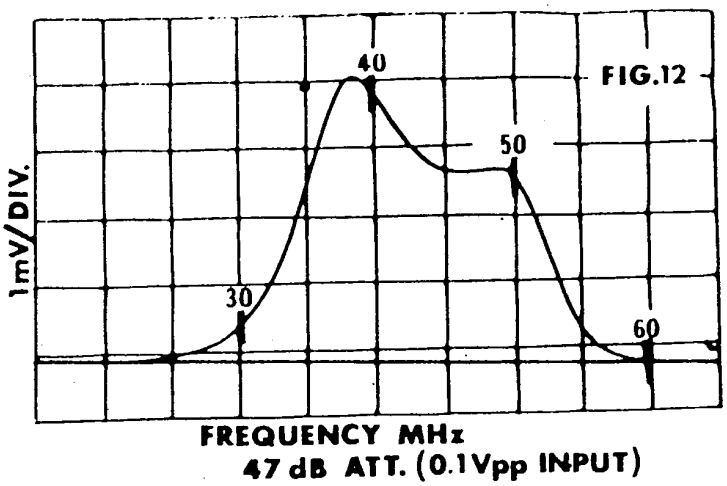


FIG.12

VHF HIGH

Program a high band frequency - Remover jumper from L312. Center trace at 160 MHz and tune L307, L308, L310, and L311 and L309 to peak trace. Two peaks should be seen in Figure 13.

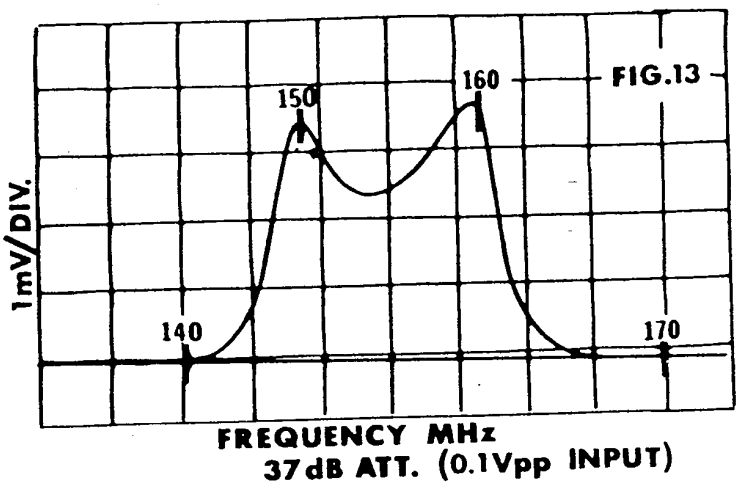


FIG.13

VHF SPECIAL ALIGNMENT 146-148 - Adjust sweep generator to cover 140 to 170 MHz. adjust L307, L308, and L314 to obtain pattern in Figure 14.

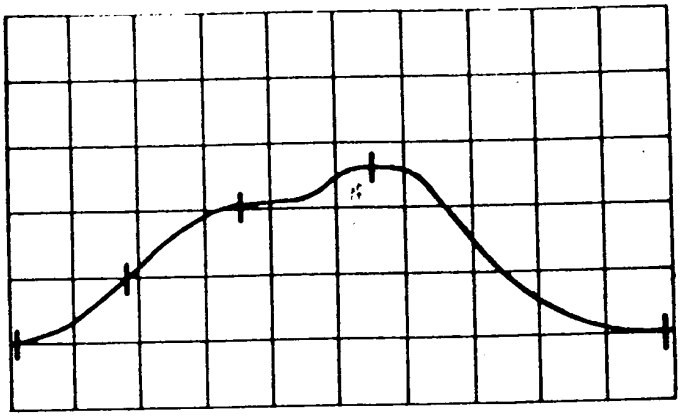
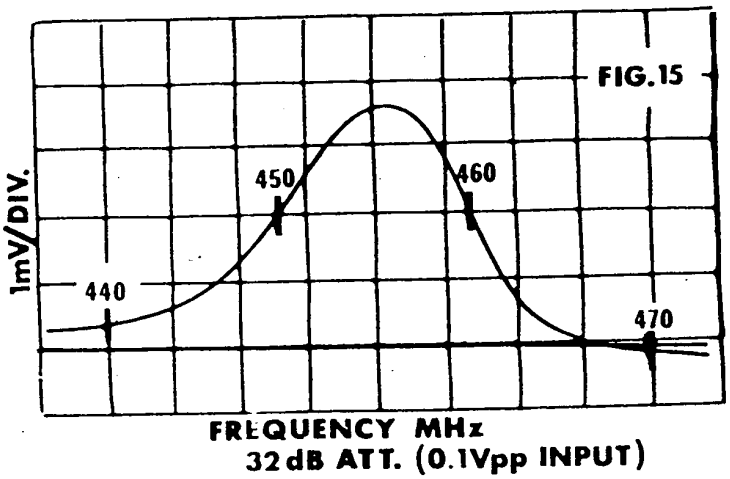


Figure 14: 2 Meter sweep

UHF

Program a UHF band frequency - Adjust sweep generator to cover 450 to 470 MHz. Tune CV301, CV302, CV303, and CV304 to peak trace at 457 MHz or 494 MHz. See Figures 15 & 16.



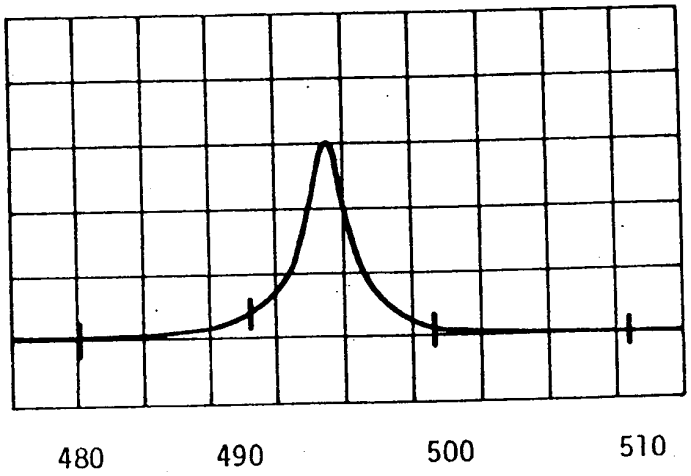


Figure 16: UHF special alignment sweep

(. MS-2 Only

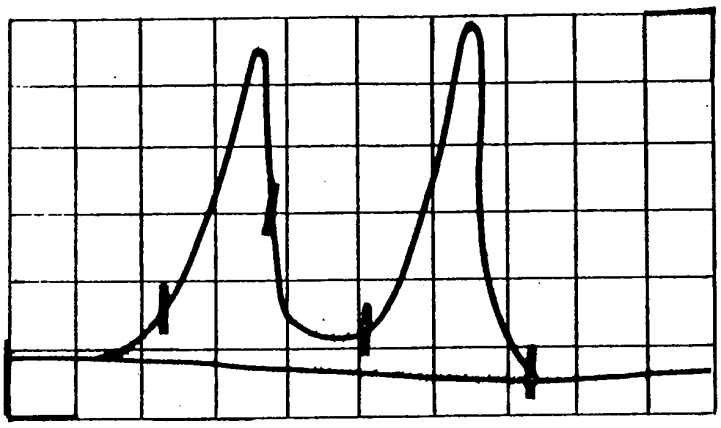


Fig. 17: MS-2 Low Band Sweep
(45 db attenuation -- (0.1 mv pp)

I. RF Alignment

Attach detector circuit to high side of L18 primary. See Fig. 23. Set sweep for 30-50 MHz display. Program low, adjust L16 for response similar to Fig. 17. Remove jumper.

Program any UH frequency. Attach counter to base of Q16, adjust L22 for 60 MHz ± 150 Hz. Then program a high band frequency and check for minimum change.

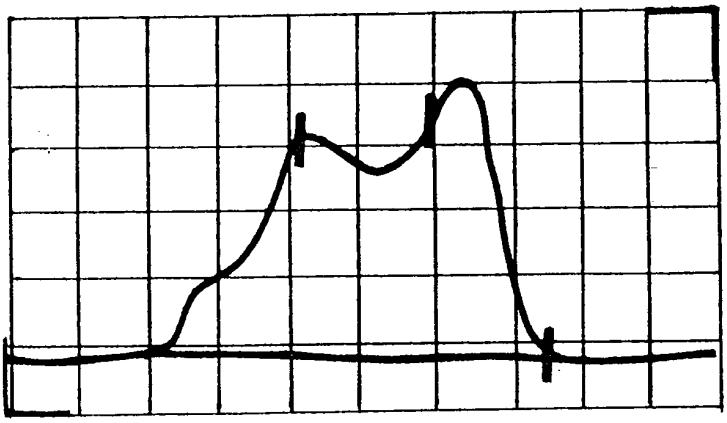


Fig. 18: MS-2 High Band Sweep
(50 db attenuation -- (0.1 mv pp)

High -- Set equipment for 150-170, adjust L11 for response, similar to Fig. 18.

C. MS-2 Only (continued)

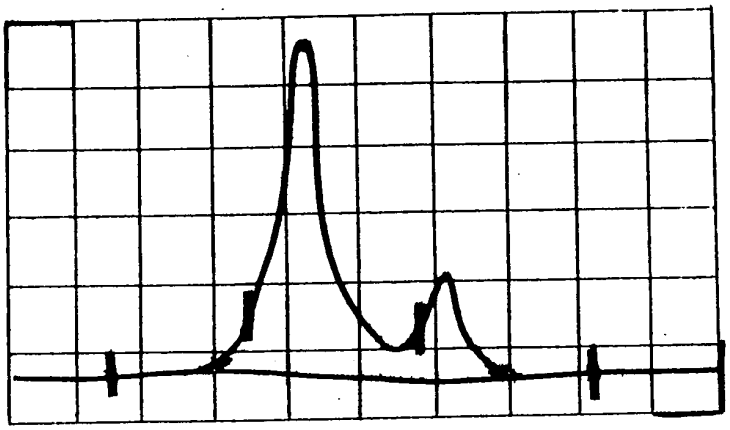


Fig. 19: MS-2 UHF Sweep
(50 db attenuation -- (0.1 mv pp)

UHF -- Set equipment for 450-470, adjust C1, C2, C3 for response similar to Fig. 19.

Special Alignments

146-148 -- Attach a 2.2pf ceramic cap from a point between C13 and C15 to ground. Attach a 2.2pf ceramic cap from gate of Q4 to ground. Attach a 5pf ceramic from gate of Q5 to ground. Attach a 39pf in parallel with C42. Adjust L11 for response as in Fig. 20.

Fig. 20: MS-2 2-Meter Sweep
(50 db attenuation -- (0.1 mv pp)

C. MS-2 Only (continued)

Fig. 21: UHF Special Alignment Sweep
(50 db attenuation -- (0.1 mv pp)

490-508 -- Adjust C1, C2, C3 for response similar to Fig. 21.

2. IF Alignment

Program unit for 45 MHz, ± 0.5 MHz. Inject 0.6 uV 400 Hz modulated signal into antenna jack with jumper installed (antenna terminal to L12 TP). Tune Quad can (L26) for best 400 Hz tone. Inject 0.6uV CW signal into antenna jack with jumper installed. Tune 10.7 can (L18) for maximum quieting.

60 MHz

D. Special Notes

Scan Delay

The scan delay of the MEMORYSCAN can be changed if so desired. To eliminate the delay, remove the +10, +25V electrolytic capacitor C113* located beside Q103. To decrease the delay, replace the capacitor with one of a lower value; to increase, replace with a capacitor of higher value. Please observe polarity.

* In MS-2 also remove R165, a 47K stand-up

Weather Transmission Interference

To trap out weather interference, solder a 4-1/2 turn coil (similar to L307), and a 5pF capacitor in series. Attach this between the antenna input and ground as seen in Figure 18.

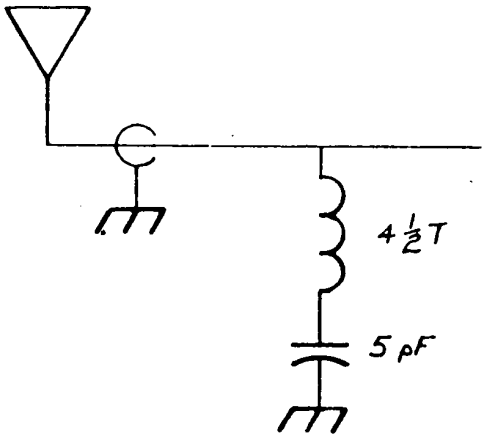


Figure 22 Weather Trap

Hum Reduction

The small amount of audio hum in the MS-2 may be irritating to some persons. To reduce this, install the Hum Reduction Modification Fig. 23 as follows:

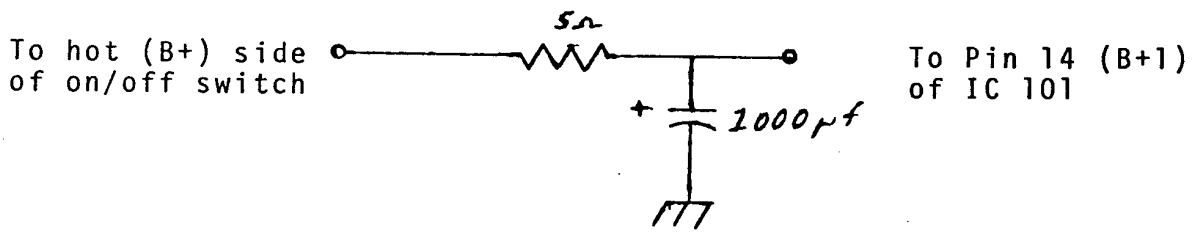


Figure 23: Hum Reduction Circuit

VI. MEMORYSCAN

Troubleshooting Guide

SYMPTOM	CHECK
Audio	
No noise at speaker with squelch full counter-clockwise	IF External speaker jack Audio on Pin 8, IC101. If present, check speaker, if not check 8 volts on pin 1 of IC101, if 8V present change IC101
Low distorted noise at speaker with squelch fully counter-clockwise	Q101 IF
Squelch	
No squelch, audio at speaker	IF Q101 & Q102
Scan	
Does not scan	Squelch Q105 IC102
Stops on one channel	Q230 & Q231 Program
Won't skip	Q106, C114, & C115, R115, & R116
LED won't light in scan	LED Lamp driver Q201 - Q214
LED's 1-6 won't light	IC104
LED's 7-16 won't light	IC103

MS-1 Troubleshooting Guide (continued)

SYMPTOM	CHECK
Program & Memory	
Won't program properly	IC201 - 207
Won't program (LED's will not light)	"0" and "1" switches Q109-Q114 C119 & C120
	Voltages to IC106
Incorrect program	Diodes 113, 114, 115 IC105 Q108
Won't enter properly (LED's light in correct order, but when program button is released then depressed again code is incorrect	IC105 & IC106
Does not remember code	VCO Frequency L321 with counter loop IF VCO is incorrect check IC's 208-215
Code is correct, RF is good, won't receive	Q308-Q310 (antenna switching) IF, low band
Sensitivity MS-1	Q311 & Q312 -- follow VHF Lo alignment
Poor all bands	Q304, Q306, & Q307 -- follow VHF alignment
Poor sensitivity on low band	
Poor sensitivity on high band	

MS-1 Troubleshooting Guide (continued)

SYMPTOM	CHECK
Poor sensitivity on UHF	Q301, Q302, & Q303 -- follow UHF alignment
Poor on HI & UHF, but low is good	60MHz oscillator Q305 CR301
Sensitivity MS-2	
Poor all bands	Q7, Q8, Q9 antenna switching IF low band
Poor sense VHF-low	Q10, Q11, follow VHF-lo alignment
Poor sense VHF-high	Q4, Q5, Q6 follow VHF-hi alignment
Poor sense UHF	Q1, Q2, Q3 follow UHF-hi alignment

PARTS LIST

Prices subject to change without notice

Instruction Manual and Code Book			$ 4.00
AC Power Cord			1.00
19" Antenna			1.00

TRANSISTORS

MSE 521			1.50
2N4124			1.50
2N4126			1.50
2N4871			2.00
MPSH10			1.50
2N301			2.00
MPS U01			1.50

IC's

SN7473			3.00
SN7493			4.00
SN74145			5.00
SN74S112			5.00
MC1357			4.00
MC4044			5.00
LM380			3.00
NM1101			10.00

DIODES

IN270			.50
IN4002			.50
IN4154			.50
IN5231			1.00
IN5235			1.00
IN5239			1.00
MV2209			1.00
HP4850			.75
IN5234			1.00

CRYSTALS & FILTERS

60 MHz	CR301 or X301		5.00
10.245 MHz	CR201		5.00
10.7 MHz Filter	SFE 10.7	CF1 or FL1	4.00
455 kHz Filter	DFM 455	CF2 or FL2	10.00
Quadrature Coil	18-223	L319 (specify S/N)	2.00
IF Transformer	18-216	L318 (specify S/N)	2.00

PARTS LIST (Continued)

MISCELLEANOUS

ON/OFF and Volume Control RP-1	$ 2.00
Squelch Control RP-2	1.50
Channel Lock-out Switch S1-S16	.75
Switch Assembly S-17, 18, 19, 20, 21	3.00
Battery Holder	.75
Antenna Jack	.75
Battery Cable	.50
Speaker	3.00
External Speaker Jack	1.00
Front Panel	4.00
Woodgrained Cabinet	5.00
RF Shield	1.00
Knobs - Volume & Squelch	.75
Knobs - "0", "1", etc.	.75
Two Prong Coil Form	.50
Three Prong Coil Form	.50
Transformer	4.00
Page Size Schematics	1.00

Minimum Order $5.00

Please remit check or money order on all parts orders, shipping charges will be prepaid.

New product or optional equipment inquiries should be directed to your dealer.

ALWAYS specify model and serial number.

National Semiconductor

MOS RAMs

MM1101, MM1101I, MM1101A, MM1101A1, MM1101A2, MM4250

256-bit fully decoded static random access memory

general description

The MM1101 family of fully decoded 256 word x 1-bit random access memories are monolithic MOS integrated circuits using silicon gate low threshold technology to achieve bipolar compatibility. They are static, require no clocks, and hold information indefinitely, subject to the integrity of the power supply voltages.

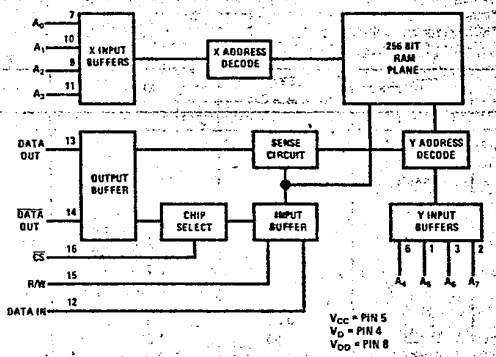
features

- Fast access times
  - MM1101A2 500 ns max
  - MM1101I, MM1101A1 1.0 μs max
  - MM1101, MM1101A 1.5 μs max
  - MM4250 650 ns max
- Improved speed/power product MM1101A2 1/3 of 1101A
- Low power operation 1.5 mW/bit
- Fewer system components – bipolar compatible input and output
- Second source flexibility – MM1101, MM1101A MM1101I, MM1101A1 second sources available
- TRI-STATE™ output – wired OR capability
- Specified ambient temperature 0°C to +70°C for MM1101 family; –55°C to +125°C for MM4250

applications

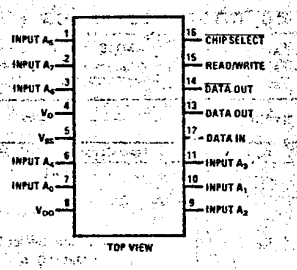
- High speed buffer memories
- Local memory store

block and connection diagrams



V_{CC} = PIN 5
V_D = PIN 4
V_{DD} = PIN 8

Dual-In-Line Package



Order Number MM1101D, MM1101AD, MM1101A1D, MM1101A2D, MM11011D or MM4250D
See Package 3

Order Number MM1101N, MM1101AN, MM1101A1N, MM1101A2N or MM11011N
See Package 15