DJ-480C/T/E

Service Manual

CONTENTS

ALINCO ELECTRONICS INC.

SPECIFICATIONS

1) General

Frequency Coverage:	RX/TX: 440.000 ~ 449.995MHz (DJ-480T only)
	RX/TX: 430.000 ~ 439.995MHz (DJ-480E only)
	RX/TX: 400.000 ~ 519.995MHz (DJ-480C version only)
Frequency Resolution:	5, 10, 12.5, 15, 20, 25kHz steps
Memory Channels:	10 Channels (standard)
Antenna Impedance:	50Ω unbalanced
Signal Type:	F3E (FM)
Power Supply Requirement:	DC 5.5V~13.8V (Rated 7.2V Ni-Cd)
Dimensions:	Approximately 132(H) x 58(W) x 33(D) mm
Weight:	Approximately 350g

2) Transmitter

Output Power:	About 5.0W with Optional 12V Ni-Cd Battery
	About 2.0W with Standard 7.2V Ni-Cd Battery
	(440.000~449.995MHz) ... DJ-480T only
	(430.000~439.995MHz) ... DJ-480E only
	(400.000~420.000MHz) ... DJ-480C1only
	(450.000~470.000MHz) ... DJ-480C2 only
	(430.000~450.000MHz) ... DJ-480C3 only
Modulation System:	Variable Reactance Frequency Modulation
Max. Frequency Deviation:	+/ -5kHz
Tone Frequency:	67.0 to 250.3Hz -38 Subaudible Encoding Tones
	(T version only)
DTMF Encoder:	(T version only)
Tone Burst:	(E version only)

3) Receiver

Receiver System:	Double-Conversion Superheterodyne
Intermediate Frequency:	1st IF: 30.85MHz
	2nd IF: 455kHz
Sensitivity:	12dB SINAD less than -16dBμ
	(440.000~449.995MHz) ... DJ-480T only
	(430.000~439.995MHz) ... DJ-480E only
	(400.000~420.000MHz) ... DJ-480C1 only
	(450.000~470.000MHz) ... DJ-480C2 only
	(430.000~450.000MHz) ... DJ-480C3 only

4) Functions for Each Versions

Function / Version	RX (MHz) Frequency Range (factory setting)	TX (MHz) Frequency Range (factory setting)	Tone Burst	CTCSS	DTMF	BAND	Final Operation
DJ-480T	435~455 (Display 400~520)	440~450	×	○	○	M	R + LA
DJ-480E	430~440	430~440	○	△ (option)	△ (option)	M	R
DJ-480C1	400~430 (Display 400~520)	400~420	×	△ (option)	×	L	R + LA
DJ-480C2	445~475 (Display 400~520)	450~470	×	△ (option)	×	H	R + LA
DJ-480C3	425~455 (Display 400~520)	430~450	×	△ (option)	×	M	R + LA

● **Final Operation**

R: Press and hold the "F" key, and turn on the radio.

R + LA: Press and hold the "F" and "LAMP" keys, and turn on the radio.

Note: The expanded frequency will return to the initial setting, if you reset the radio with "R" operation after "R + LA" operation. To resume the expanded frequency, reset the radio again with "R + LA" operation.

CIRCUIT DESCRIPTION

1) Receiver System

The receiver system is the double superheterodyne.
The first IF is 30.85MHz and the second IF is 455kHz.

1. Front End

The signal from the antenna is passed through a low-pass filter and input to the RF coil L9.
The signal from L9 is amplified by Q12, Q13 and led to the band pass filter (L10, L11, L12, L13), and led to the first mixer base of Q14.

2. First Mixer

The amplified signal (fo) by Q12, Q13 is mixed with the first local oscillator signal (fo -30.85MHz) from the PLL circuit by the first-stage mixer Q14 and so is converted into the first IF signal.
The unwanted frequency band of the first IF signal is eliminated by the monolithic crystal filter (XF1), and led to IF amplifier Q19.

3. IF Amplifier

The first IF signal is amplified by Q19, and input to pin20 of IC1, where it is mixed with the second local oscillator signal (30.395MHz) and so is converted into the second IF signal (455kHz).
The second IF signal is output from pin4 of IC1, and unwanted frequency band of the second IF signal is eliminated by a ceramic filter (FL1).
The resulting signal is then amplified by the second IF limiting amplifier, and detected by quadrature circuit. The audio signal is output from pin11 of IC1.

4. Audio Circuit

The detected signal from IC1 is passed through the low-pass filter and led to the flat amplifier Q21. When the optional Tone Squelch unit is equipped, the tone signal is eliminated by IC701.
Q21 is switched ON/OFF by AFC signal from CPU.
The audio signal is input to the main volume (VR3) and amplified by the power amplifier IC3 to drive the speaker.
The power supply voltage of IC3 is limited by AF regulator consisting of Q22 and Q23 to prevent the speaker from overdriving. The power supply voltage of IC3 is switched ON/OFF by AFP signal.

5. Squelch Circuit

The noise in the audio signal from IC1 is passed through the squelch control variable resistor (VR4) and input to pin12 of IC1. The audio signal is amplified by filter amplifier of IC1 and output to pin14. The desired noise of the audio signal is eliminated by the high-pass filter and amplified by Q20. The resulting signal is rectified by D13 and then input to pin15 of IC1. When the squelch circuit is close, pin16 of IC1 goes to "low". When the squelch circuit is open or a signal is received, pin16 goes to "high", then the signal of pin16 is led to CPU.

2) PLL, VCO Circuit

Output frequency of PLL circuit is set by the serial data (pin9: clock, pin10: data, pin11: load enable) from microprocessor.
PLL circuit consists of VCO Q201, Q203, buffer amplifier Q202.
When PLL is locked, pin7 of IC2 goes to "high" and UNLOCK SW Q901 becomes OFF, then T.MUTE signal goes to "low".
The pulse wave output of charge pump is converted to DC voltage by PLL loop filter circuit, and supplied to D202~D205 of varicap diode in VCO unit.
The VCO tune voltage is applied to the varicaps D7, D8, D9, D10 and D11 in the front end.
The frequency modulation is executed when the audio signal voltage is supplied to the varicap D201.

3) Transmitter System

1. Microphone Amplifier

The voice from the internal or external microphone is led to the pre-emphasis circuit, and then input to the microphone amplifier IC4, which consists of two operational amplifiers.
The amplified signal is input to the low-pass filter IC4.
The output from the microphone amplifier is passed through variable resistors VR2 for modulation adjustment to varicap diode of the VCO, controlling the VCO frequency.

2. Power Amplifier

The signal from VCO is amplified by buffer amplifiers Q1 and Q2, and input to the power module IC6, and then passed through the low-pass filter, the antenna switch circuit and the output low-pass filter. The unwanted harmonics frequency signal is eliminated by the low-pass filter and input to the antenna. The LC matching circuits located between amplifiers of the transmitting circuit make the transmission smooth.

3. Automatic Power Control Circuit

The automatic power control(APC) circuit is used to obtain a stable transmission power. This circuit detects the transmission power by D3. The detected DC voltage is supplied to APC circuit. When the detected voltage goes higher than the settled voltage, the bias voltage of APC amplifier Q7 goes to low. The collector voltage of APC amplifier Q6 goes to low and the power supply voltage of Q1 goes to low, and output power becomes small to prevent from the over power.
At low power the Power Control Switch Q8 lets the base voltage of APC DET Q5 and the collector voltage of APC AMP Q6 down, also switches between high power and low power, and inhibits the transmission.

4) DTMF Encoder Circuit (option)

The DTMF signal corresponding to the combination of the column and row is output from tone output pin17 of IC401 Encoder, producing a frequency-modulated RF output. The Q401 switches the DTMF Encoder when IC401 is active during DTMF transmission.

5) Tone Squelch Circuit (option)

1. Decoder

The second IF signal from pin11 of IC1, and input to the tone squelch decoder IC701.
When the tone squelch decoder IC701 decodes the input tone signal frequency as the programmed frequency, pin13 goes to "Low". The signal is input to pin16(DET) of IC107, and the squelch goes off.
When the Tone squelch decoder IC701 does not decode the input tone signal frequency as the programmed frequency, pin13 goes to "High".

2. Encoder

The tone signal is output from pin16 of IC701, producing a frequency-modulated RF output.

6) Microprocessor (CPU) and Peripheral Circuit

Refer to "Terminal Function of Microprocessor" about each terminal function.

1. BS Mode

When the Squelch is closed for more than 5 seconds, the radio goes into the BS(Battery Save) mode automatically. Pin11(R5C) and pin19 become High or Low periodically. Open the Squelch, and the radio does not go into the BS mode.

2. Backup Reset

When the voltage detector circuit IC303 detects a decrease in the C5V line, CPU RAM data is stored in the EEPROM IC, IC601. IC 302 is also the voltage detector circuit and it detects the lower voltage than IC303. The circuit detects a increase in the C5V line when power is turned on, and then the CPU will be initialized.

3. Reset

Press and hold the "F" key, then turn on the power. The radio will reset to initial factory settings.
Even if you expanded the frequency, it will return to the initial setting. To resume the expanded frequency, press and hold the "F" and "Lamp" keys, then turn on the power.

7) Terminal Function of Microprocessor

Name	I/O	Description	Pin No.	Pin Name	H	L
TBST	O	1750Hz Tone Burst Output	9	P57/PWM3	Normal: H(HiZ)	Output: Pulse
BEEP	O	Beep Tone Output	10	P56/PWM2	Normal: H(HiZ)	Output: Pulse
R5C	O	RX5V ON/OFF	11	P55/PWM1	ON	OFF
T5C	O	TX5V ON/OFF	12	P54/PWM0	ON	OFF
AFP	O	AF Power Amplifier ON/OFF	13	P53/SIG	ON	OFF
AFC	O	IF Mute Output	14	P52/CNT2	Mute OFF	Mute ON
M. MUTE	O	Microphone Mute Output	15	P51/CNT1	during Tone Burst Tansmission	Normal
RE1	I	Rotary Encoder Input 1	16	P50/INT3		
LAMP	O	Lamp ON/OFF Switch	17	P37/$\overline{\text{SRDY}}$	ON	OFF
BAT	I	Battery Low Indicator Input	18	P36/CLK	Low	Normal
P5C	O	PLL Power ON/OFF	19	P35/SOUT	ON	OFF
EICD	I	EEPROM Unit Detection	20	P34/SIN	Equipped	Nothing
XWR	I	External EEPROM Write Cycle Detection	21	P33/T	Normal	Write Cycle
RE2	I	Rotary Encoder Input 2	22	P32/INT2		
SCOM	O	Band Plan Scan Output	23	P31/XCIN	H (Hiz)	Low Active
P.H/L	O	Transmit power Switch	24	P30/XCOUT	Low Power	High Power
$\overline{\text{BU}}$	I	Backup Mode Input	25	INT1	Normal	Negative Edge Triggered
			26	CNVss		
$\overline{\text{RES}}$	I	Reset Input	27	$\overline{\text{RESET}}$	at Work	on Reset
		Clock Input 3.58MHz	28	XIN		
		Clock Output 3.58MHz	29	XOUT		
		Ground	30	Vss		
$\overline{\text{TSQD}}$	I	Tone Detection Input	31	P17	Undetected	Detected
TICD	I	Tone Unit Detection	32	P16	Nothing	Equipped
BP1	I	Band Plan (TX)	33	P15	Expanded	Normal
BP2	I	Band Plan (RX)	34	P14	Expanded	Normal
BP3	I	Band Plan (TX, RX)	35	P13	Expanded	Normal
BP4	I	Band Plan (Channel step)	36	P12	Expanded	Normal

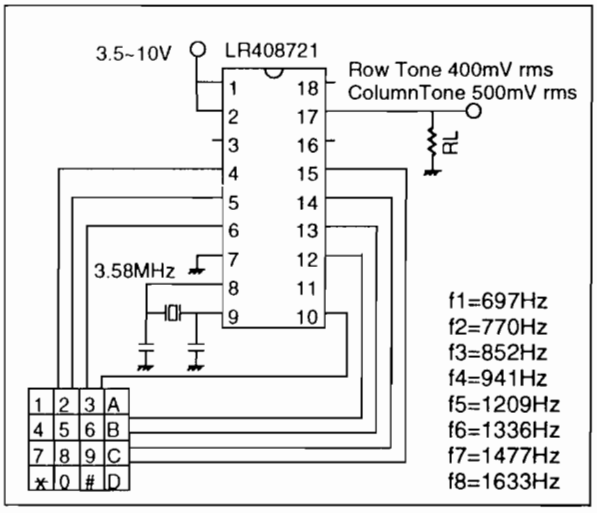
Name	I/O	Description	Pin No.	Pin Name	H	L
BP5	I	Band Plan (Offset Freq.)	37	P11	Expanded	Normal
CH	I	Band Plan (Channel Disp.)	38	P10	Expanded	Normal
SLC	O	Clock for EEPROM IC	39	P07	Normal: Hiz	Output: Pulse
SDA	I/O	Data for EEPROM IC	40	P06	Normal: Hiz	Output: Pulse
CLK	O	Clock for PLL, TONE IC	41	P05	Output: Pulse	Normal: L
DTA	O	Data for PLL, TONE IC	42	P04	Output: Pulse	Normal: L
STB1	O	Strobe for PLL IC	43	P03	Output: Pulse	Normal: L
STB2	O	Strobe for TONE IC	44	P02	Output: Pulse	Normal: L
$\overline{\text{FUNC}}$	I	Function Key Input	45	P01	OFF	ON
SD	I	Signal Detection Input	46	P00	Received	Nothing
$\overline{\text{TBST}}$	I	Tone Burst Key Input	47	P27	OFF	ON
$\overline{\text{CALL}}$	I	CALL (APO)	48	P26	OFF	ON
$\overline{\text{LAMP}}$	I	LAMP (FL/PL)	49	P25	OFF	ON
$\overline{\text{MONI}}$	I	MONI (P. H/L)	50	P24	OFF	ON
$\overline{\text{TONE}}$	I	TONE (MW)	51	P23	OFF	ON
$\overline{\text{V/M}}$	I	V/M (OFFSET)	52	P22	OFF	ON
$\overline{\text{T. SCAN}}$	I	T.SCAN (CH STEP)	53	P21	OFF	ON
$\overline{\text{PTT}}$	I	PTT Key Input	54	P20	OFF	ON
			55	VL3		
			56	VL2		
			57	VL1		
COM0	O	Common Output	58	COM0		
COM1	O	Common Output	59	COM1		
COM2	O	Common Output	60	COM2		
			61	COM3		
SEG0	O	Segment Output	62	SEG0		
SEG1	O	Segment Output	63	SEG1		
SEG2	O	Segment Output	64	SEG2		
SEG3	O	Segment Output	65	SEG3		
SEG4	O	Segment Output	66	SEG4		
SEG5	O	Segment Output	67	SEG5		
SEG6	O	Segment Output	68	SEG6		
SEG7	O	Segment Output	69	SEG7		

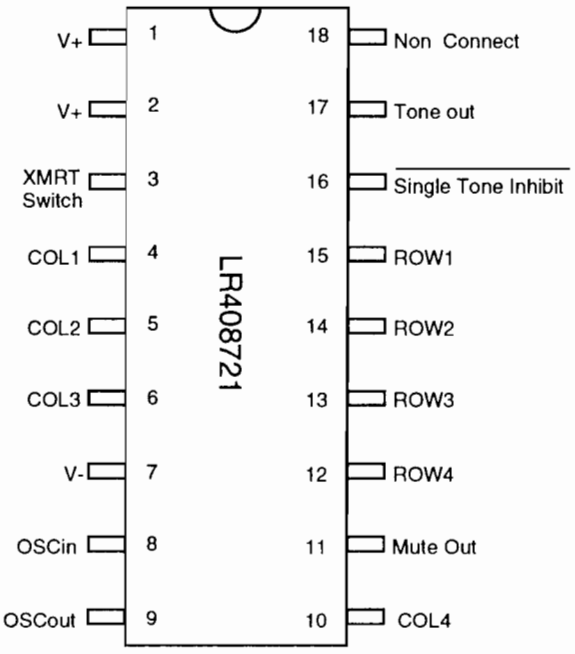
Name	I/O	Description	Pin No.	Pin Name	H	L
SEG8	O	Segment Output	70	SEG8		
SEG9	O	Segment Output	71	SEG9		
SEG10	O	Segment Output	72	SEG10		
SEG11	O	Segment Output	73	SEG11		
SEG12	O	Segment Output	74	SEG12/P43		
SEG13	O	Segment Output	75	SEG13/P42		
SEG14	O	Segment Output	76	SEG14/P41		
SEG15	O	Segment Output	77	SEG15/P40		
SEG16	O	Segment Output	78	SEG16/IN7		
SEG17	O	Segment Output	79	SEG17/IN6		
SEG18	O	Segment Output	80	SEG18/IN5		
SEG19	O	Segment Output	1	SEG19/IN4		
SEG20	O	Segment Output	2	SEG20/IN3		
SEG21	O	Segment Output	3	SEG21/IN2		
SEG22	O	Segment Output	4	SEG22/IN1		
SEG23	O	Segment Output	5	SEG23/IN0		
		Ground	6	AVss		
		+4V	7	Vref		
		+4V	8	Vcc		

SEMICONDUCTOR DATA

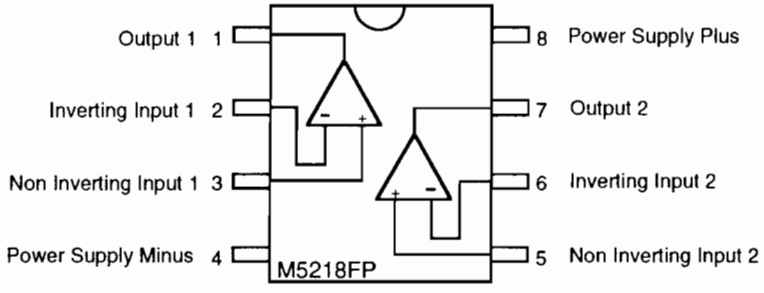
1) LR408721 (XA0042)
Tone Dialer

Test Circuit



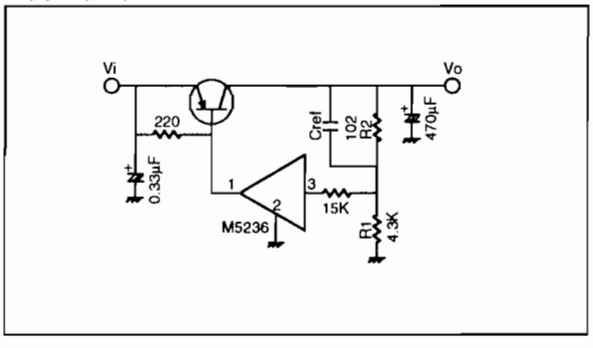


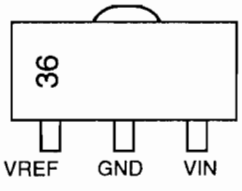
2) M5218FP (XA0068)
Dual Low Noise
Operational Amplifiers



3) M5236ML (XA0104)
Voltage Regulator

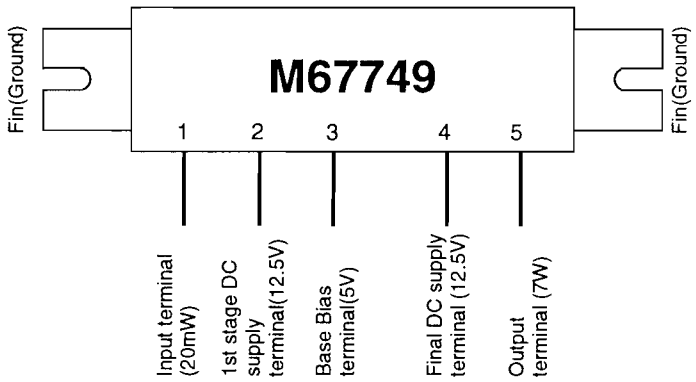
Test Circuit



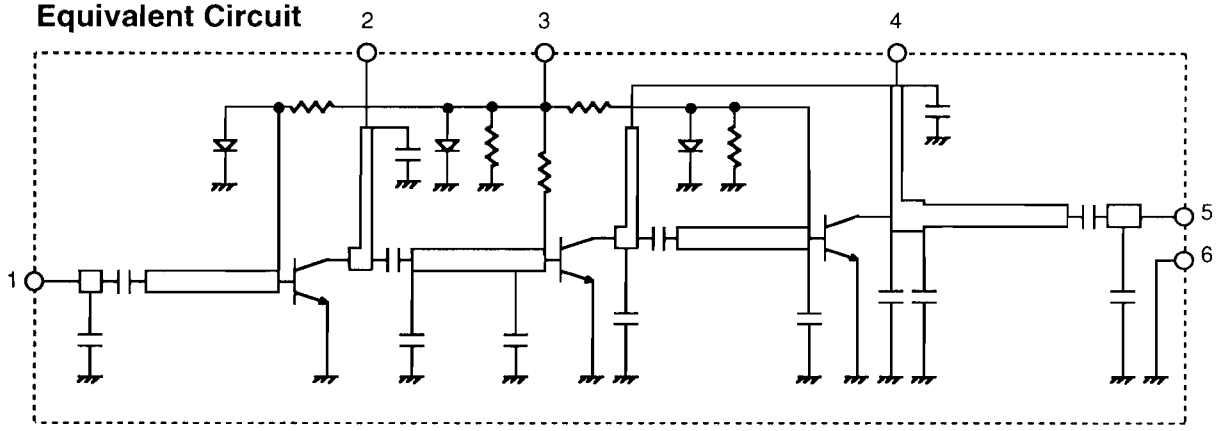


M5236ML

4) M67749L (XA0177) 400 ~ 430MHz 7W RF Power Module
M67749M (XA0143) 430 ~ 450MHz 7W RF Power Module
M67749H (XA0178) 450 ~ 470MHz 7W RF Power Module



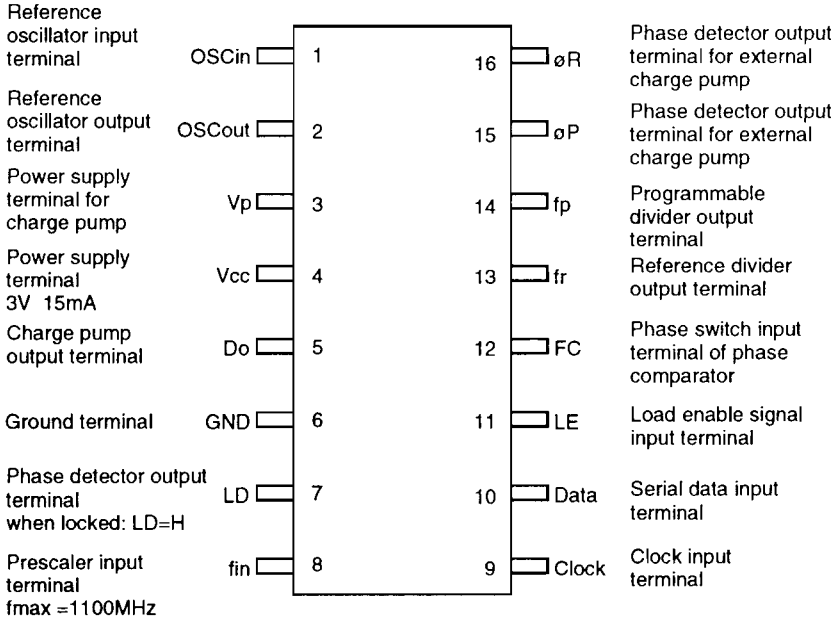
Equivalent Circuit



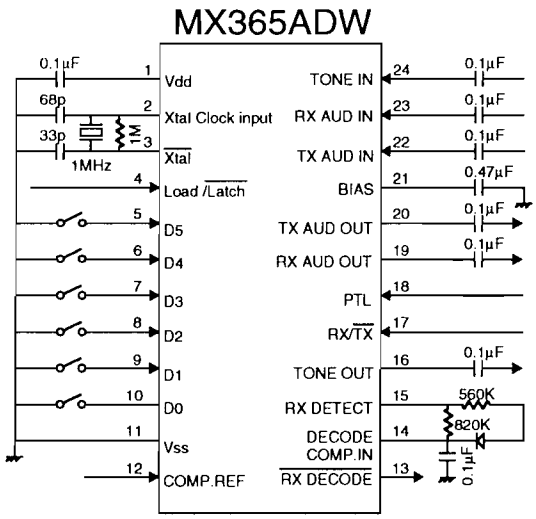
5) MB1504LPF-G-BND-TF (XA0145)
Frequency Synthesizer

Function Table

FC input	P.D.input	Do output
High or Low	fr=fp	Hi Z
High	fr>fp	High
High	fr<fp	Low
Low	fr>fp	Low
Low	fr<fp	High



6) MX365 (XA0203)
CTCSS Encoder/Decoder



Decode Comparator Ref: This pin is internally biased to VDD/3 or 2VDD/3 via 1M resistors depending on the logical state of the Rx Tone Decode Out pin. Rx Tone Decode Out = 1 will bias this input 2VDD/3; a logic "0" will bias this input VDD/3. This input provides the decode comparator reference voltage, and switching of bias voltages provides hysteresis to reduce "chatter" under marginal conditions.

$\overline{\text{RX Tone Decode Out}}$: This is the gated output of the decode comparator. This output is used to gate the RX Audio path. A logic "0" on this pin indicates a successful decode and that the Decode Comparator Input pin is more positive than the Decode Comparator Ref. input.

Decode Comparator Input: This is the inverting input of the decode comparator. This pin is normally connected to the integrated output of the Rx Tone Detect line.

Rx Tone Detect : In Rx mode this pin will go to logic '1' during a successful decode. It must be externally integrated to control response and deresponse times.

Tx Tone Out: The CTCSS sinewave output appears on this pin under the control of the Rx/$\overline{\text{Tx}}$ pin. This pin, when not transmitting a tone, may be biased to VDD/2 - 0.7V or O/C .

Rx/$\overline{\text{Tx}}$: This input (in parallel mode) selects Rx or Tx modes . In serial mode this function is serially loaded. This pin is internally pulled to VDD via a 1 MΩ resistor.

PTL: In parallel Rx mode this pin operates as a 'Press To Listen' function by enabling the Rx audio path, thus overriding the tone squelch function. In parallel Tx mode this pin reverses the phase of the transmitted CTCSS tone (used for squelch tail elimination). In serial mode this function is serially loaded.

Rx Audio Out: This is the high pass filtered receive audio output pin. This pin outputs audio when Rx TONE DECODE = 0, or PTL = 1, or when Notone is programmed. In Tx mode this pin is biased to VDD/2.

Tx Audio Out: This is the high pass filtered transmit audio output pin. In Tx mode this pin outputs audio present at the Tx Audio Input pin. In Rx mode this pin is biased to VDD/2.

Bias: This pin is the output of an internally generated VDD/2 bias level and would normally be externally decoupled to Vss via C7.

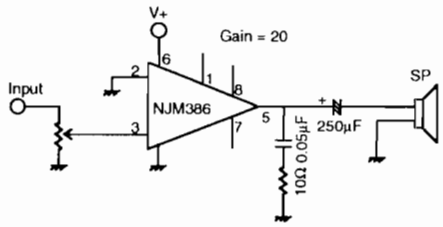
Tx Audio In: This is the Tx Audio input pin. In Tx mode it may be prefiltered, using the Tx audio path, thus helping to avoid talk off due to intermodulation of speech frequencies with the transmitted CTCSS tone. This pin is internally biased to VDD/2.

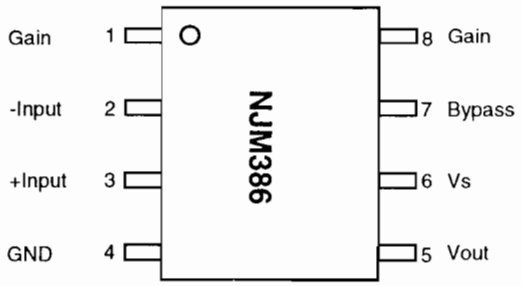
Rx Audio In: This is the input to the audio high pass filter in Rx mode. It is internally biased to VDD/2.

Tone Input: This is the input to the CTCSS tone detector. It is internally biased to VDD/2.

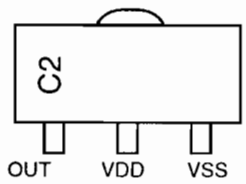
7) NJM386 (XA0061)
Power Amplifiers

V+=9V RL=16Ω Po=500mW



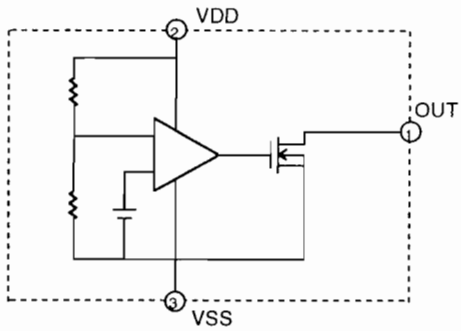


8) RH5VA32AA-T1 (XA0198)
C-MOS Voltage Detector

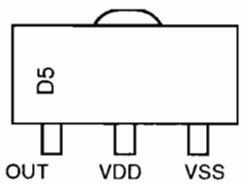


RH5VA32AA

Equivalent Circuit

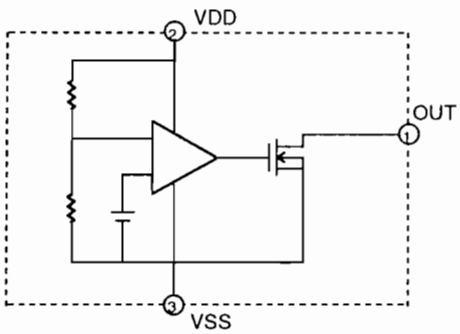


9) RH5VA45AA-T1 (XA0208)
C-MOS Voltage Detector



RH5VA45AA

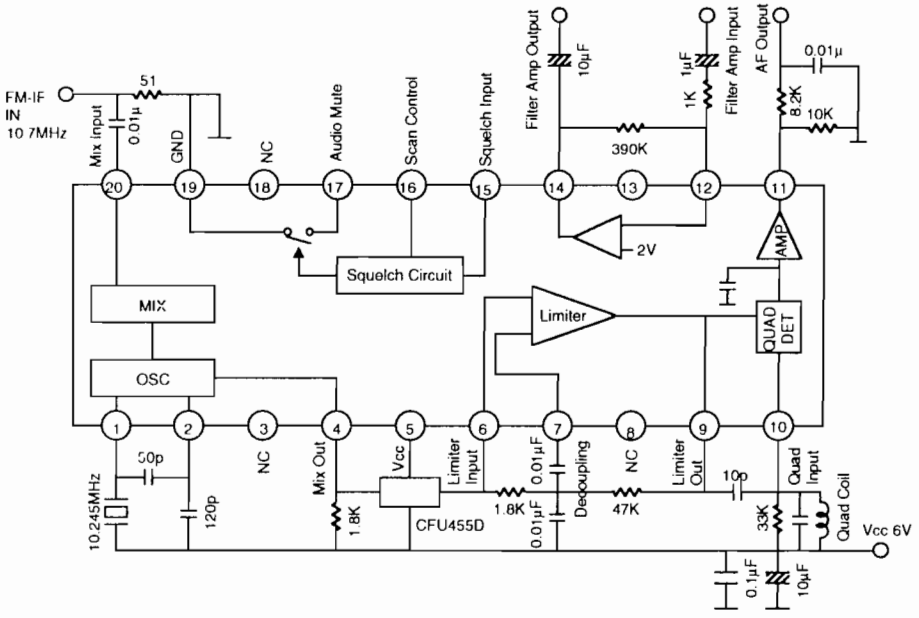
Equivalent Circuit

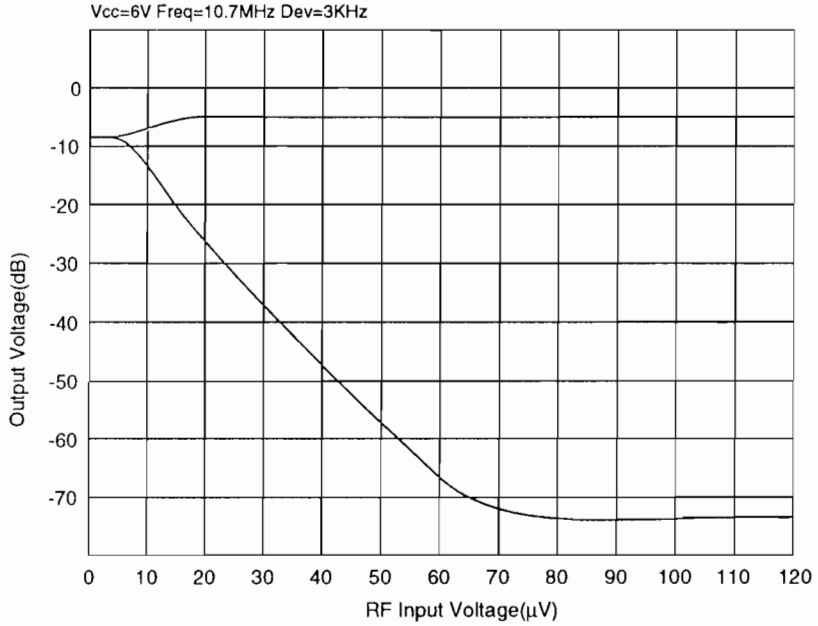


10) TK10420MTR (XA0234)

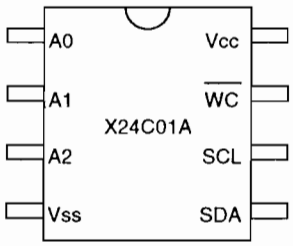
Narrow Band FM IF IC

Characteristic	Symbol	Typical
Supply Current	Icc	4.0mA
Limiting Sensitivity	Limit	3.0μV
Output Impedance	Zout	400Ω
Output Voltage	Vout	550mVrms
Filter Gain	Fgain	46dB
Mute Switch Resistance	ML	15Ω
Scan Control Voltage	SL	0V
Mixer Conversion Gain	Mg	20dB
Mixer Input Impedance	Mg	3.3KΩ
Mixer Input Capacitance	Mim	2.2pF
Frequency Range	Fop	455KHz ~ 60MHz





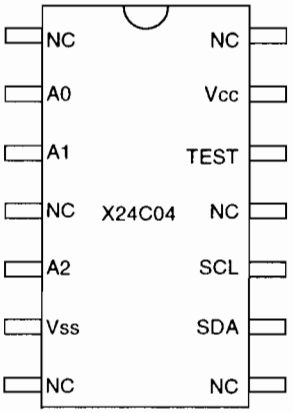
11) X24C01A (XA0199)
EEPROM 1024Bit



Pin Names

A0 ~ A2	Address inputs
SDA	Serial Data
SCL	Serial Clock
WC	Write Control
Vss	Ground
Vcc	+5V

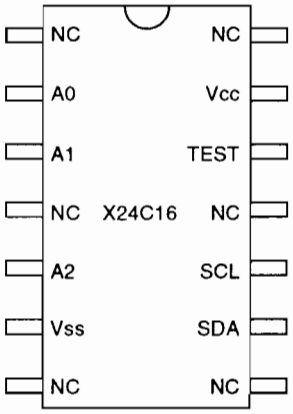
12) X24C04S14 (XA0200)
EEPROM 4096Bit



Pin Names

A0 ~ A2	Address inputs
SDA	Serial Data
SCL	Serial Clock
TEST	Hold at Vss
Vss	Ground
Vcc	+5V
NC	No Connect

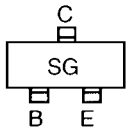
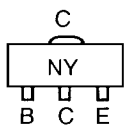
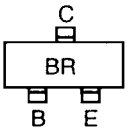
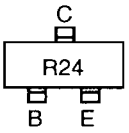
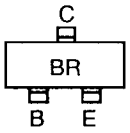
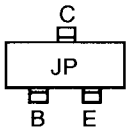
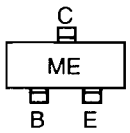
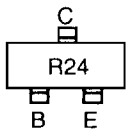
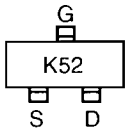
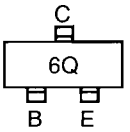
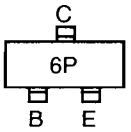
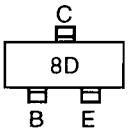
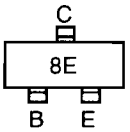
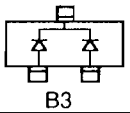
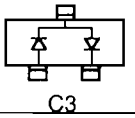
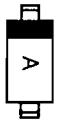
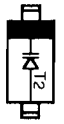
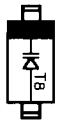
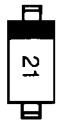
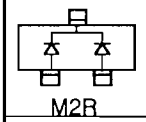
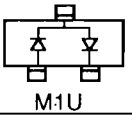
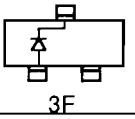
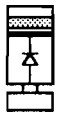
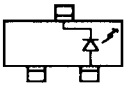
13) X24C16S14 (XA0201)
EEPROM 16384Bit



Pin Names

A0 ~ A2	Address inputs
SDA	Serial Data
SCL	Serial Clock
TEST	Hold at Vss
Vss	Ground
Vcc	+5V
NC	No Connect

14) Transistor, Diode and LED Outline Drawings

2SA1162	2SA1213	2SC2412	2SC3356	2SC4081	2SC4099	2SC4393	2SC4226
XT0068	XT0088	XT0037	XT0030	XT0095	XT0096	XT0097	XT0106
							
2SK508	UN211L	UN211H	UN2214	UN2215			
XE0010	XU0039	XU0040	XU0038	XU0037			
							
1SS184	1SS226	1SS355	1SV214	1SV215	1SV229	DTZ2.4A	DTZ6.2A
XD0057	XD0103	XD0254	XD0131	XD0132	XD0133	XD0147	XD0137
							
MA704WK	MA716	RB450F	RLS135	SLM-13MWS			
XD0120	XD0118	XD0134	XD0066	XL0016			
							
XN111F	XN1213	XN1214	XN1401
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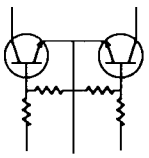
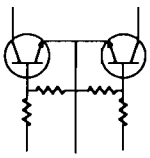
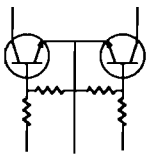
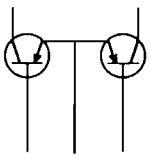
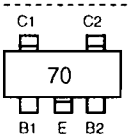
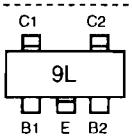
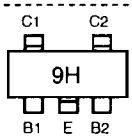
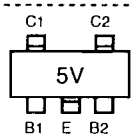
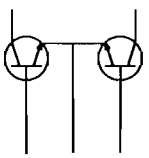
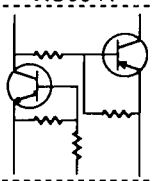
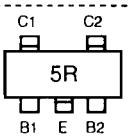
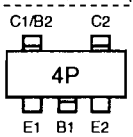
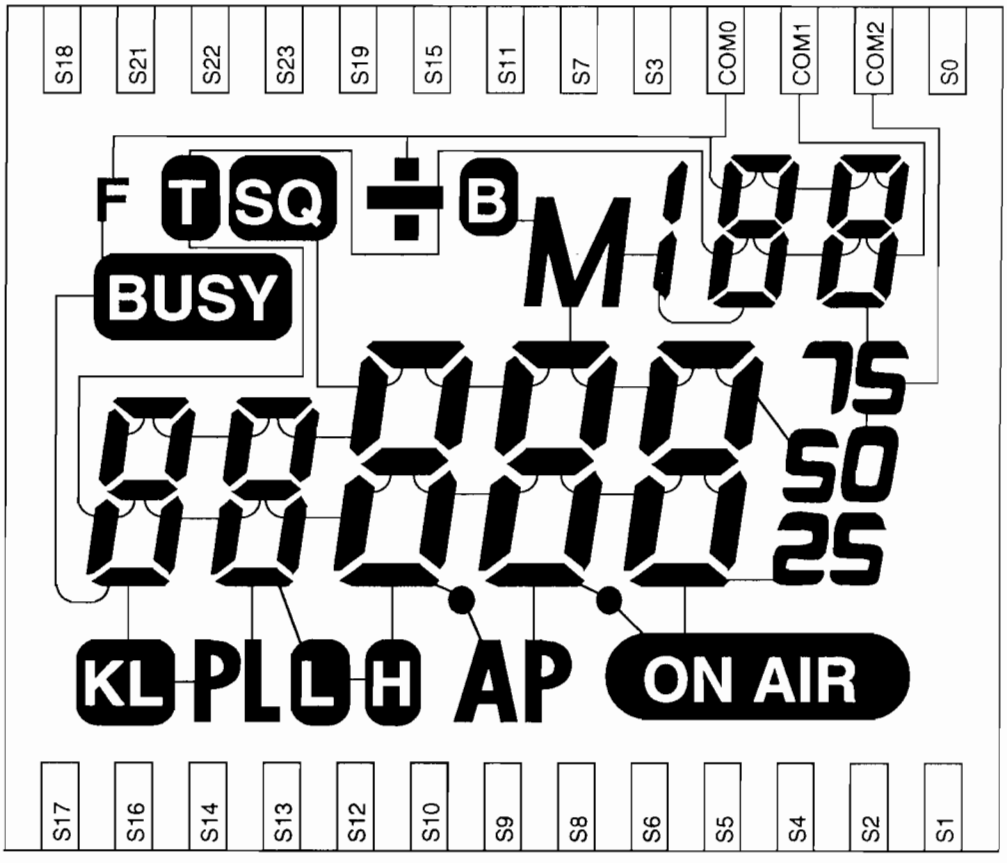
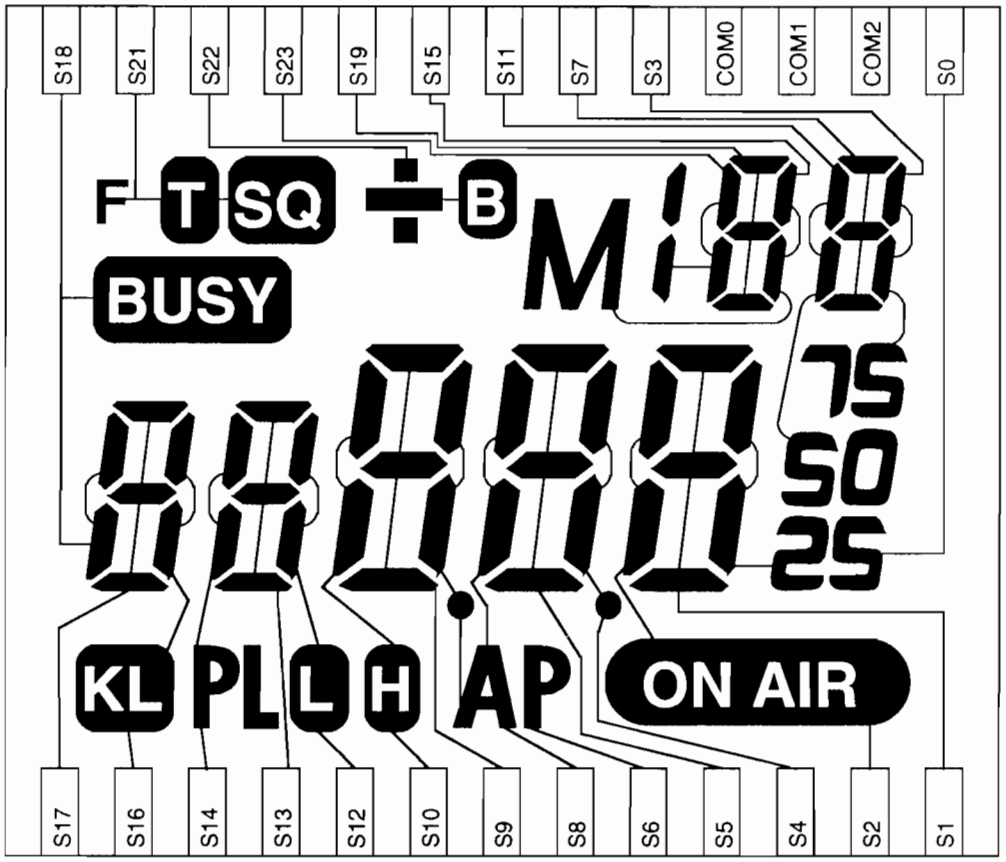
XU0036	XU0054	XU0035	XT0034
			
			
XN1501	XN1A312		
XU0053	XU0041		
			
			

15) LCD Connection

COMMON

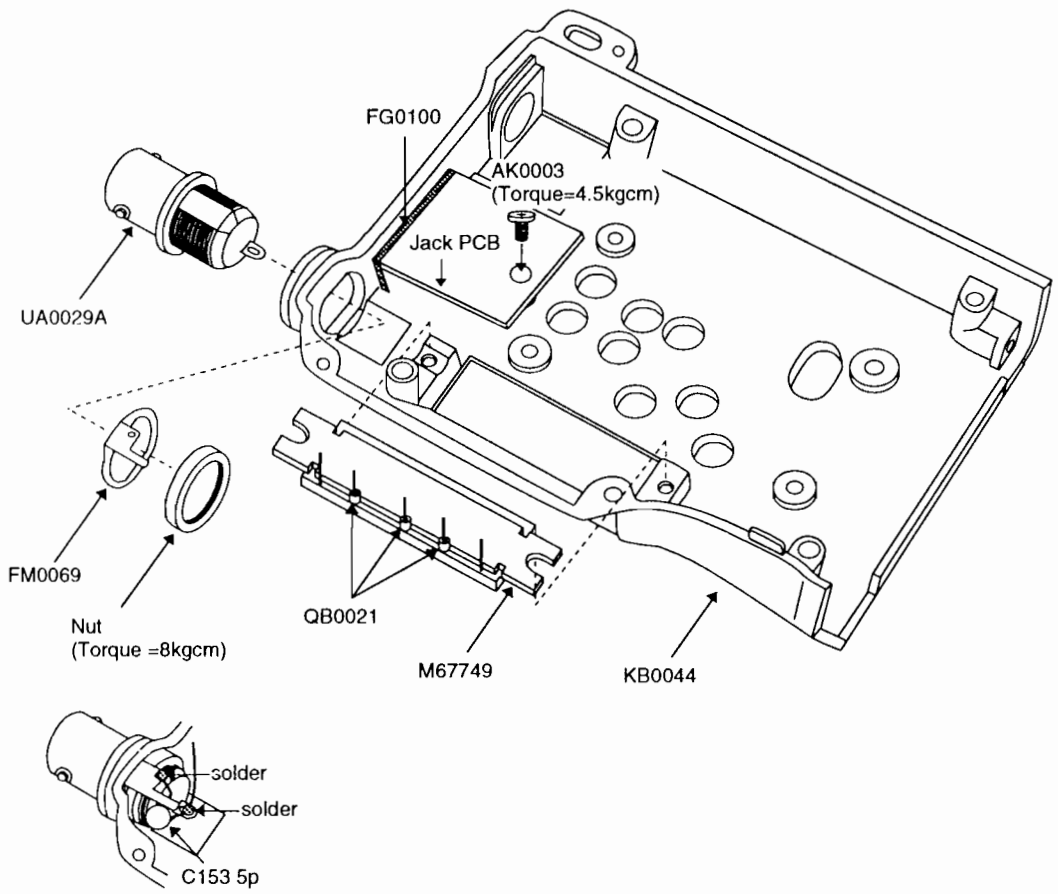


SEGMENT

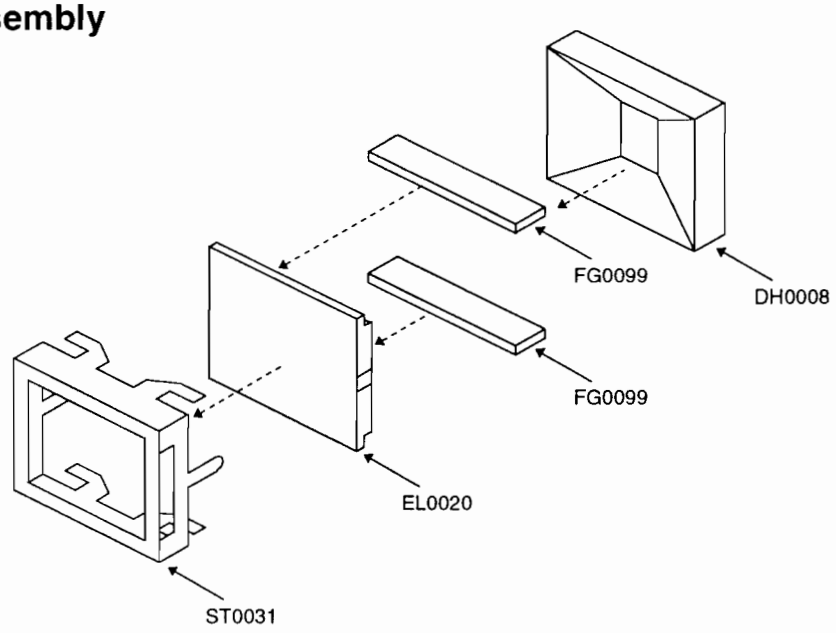


EXPLODED VIEW

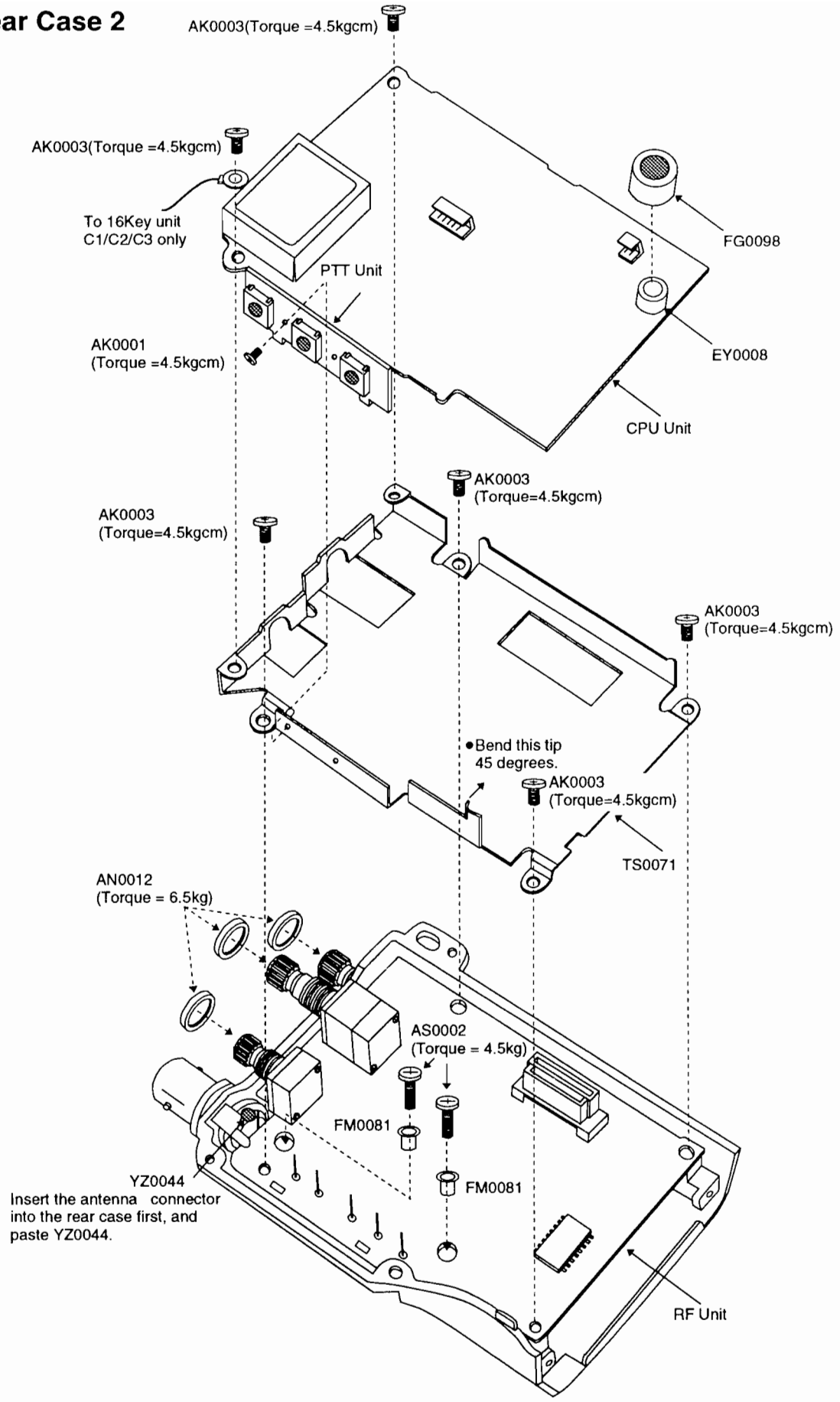
1) Rear Case 1



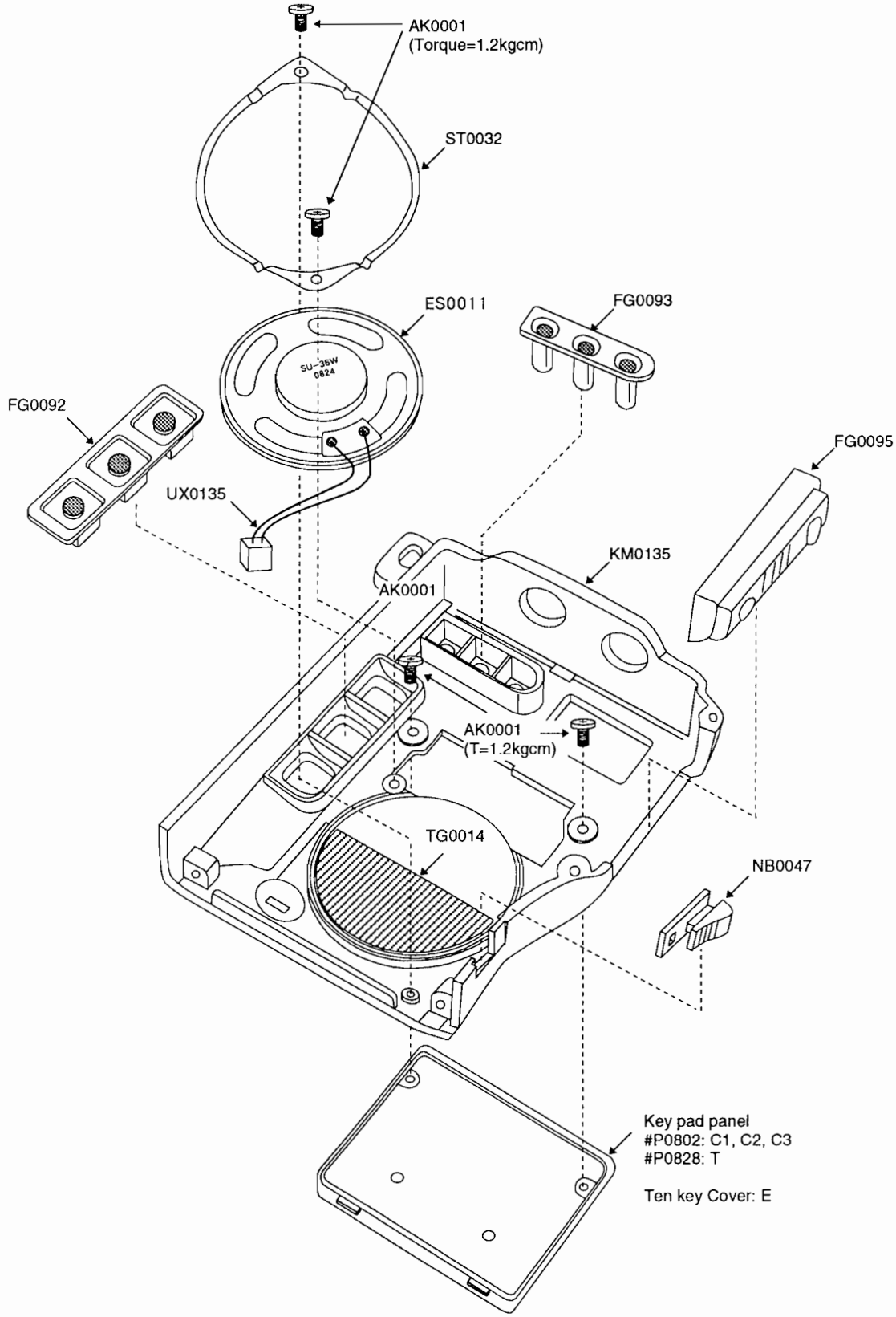
2) LCD Assembly



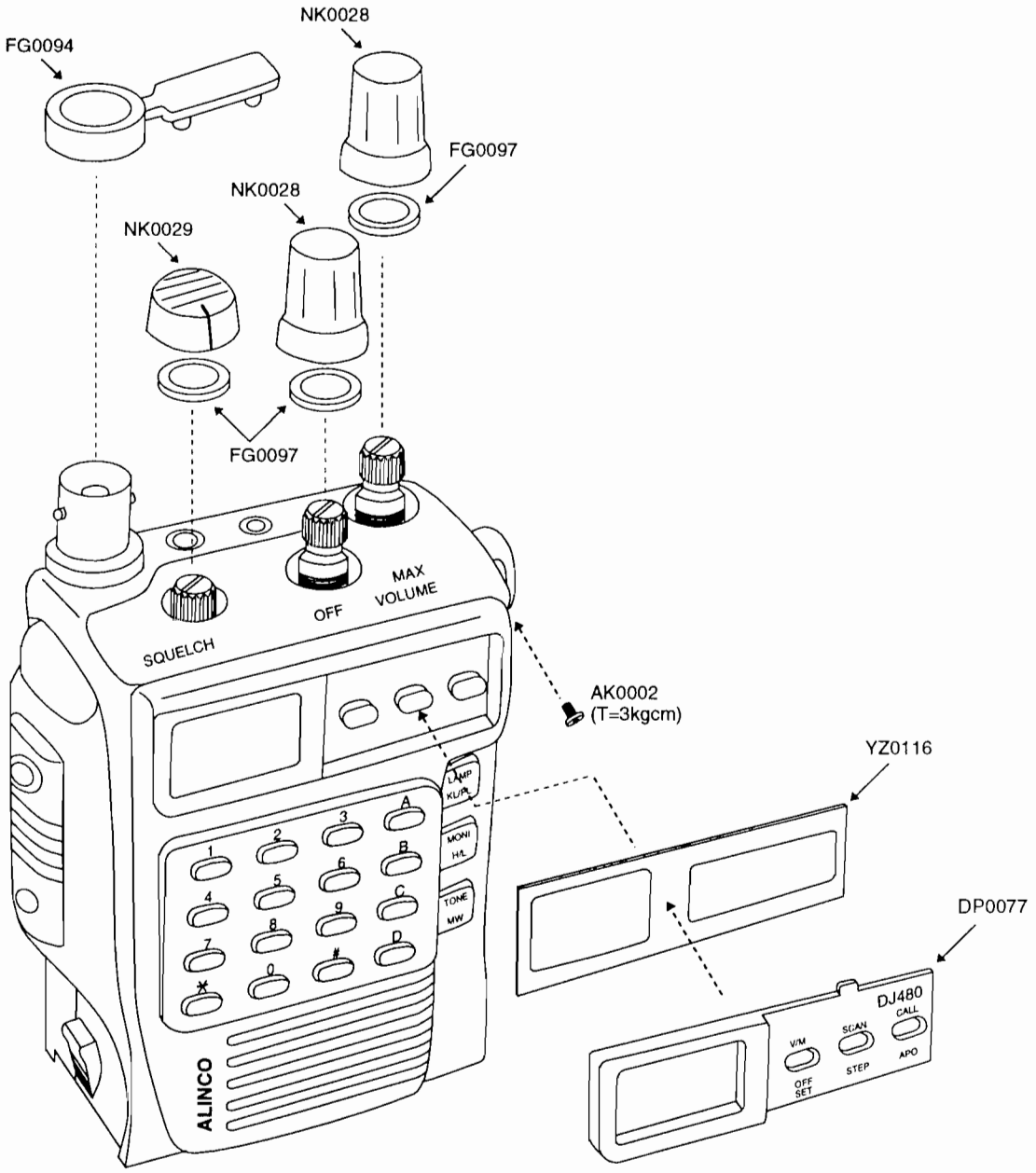
3) Rear Case 2


AK0003(Torque =4.5kgcm)
AK0003(Torque =4.5kgcm)
To 16Key unit
C1/C2/C3 only
PTT Unit
AK0001
(Torque =4.5kgcm)
FG0098
EY0008
CPU Unit
AK0003
(Torque=4.5kgcm)
AK0003
(Torque=4.5kgcm)
AK0003
(Torque=4.5kgcm)
•Bend this tip
45 degrees.
AK0003
(Torque=4.5kgcm)
TS0071
AN0012
(Torque = 6.5kg)
AS0002
(Torque = 4.5kg)
FM0081
FM0081
YZ0044
Insert the antenna connector
into the rear case first, and
paste YZ0044.
RF Unit

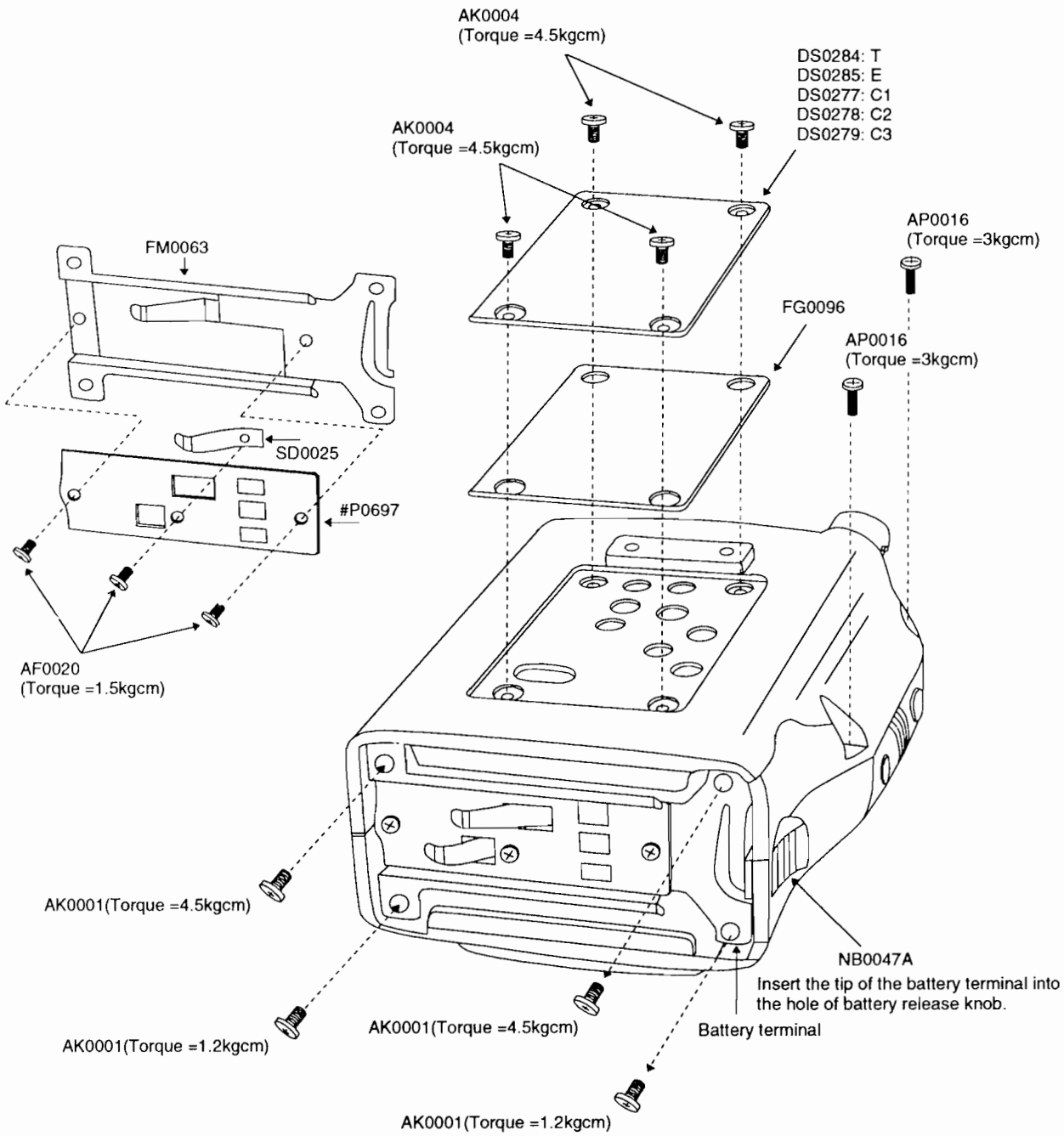
4) Front Case 1



5) Front Case 2

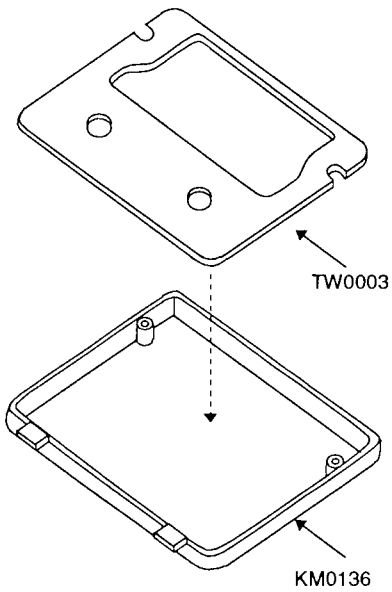


6) Rear Case 3 and Battery Terminal

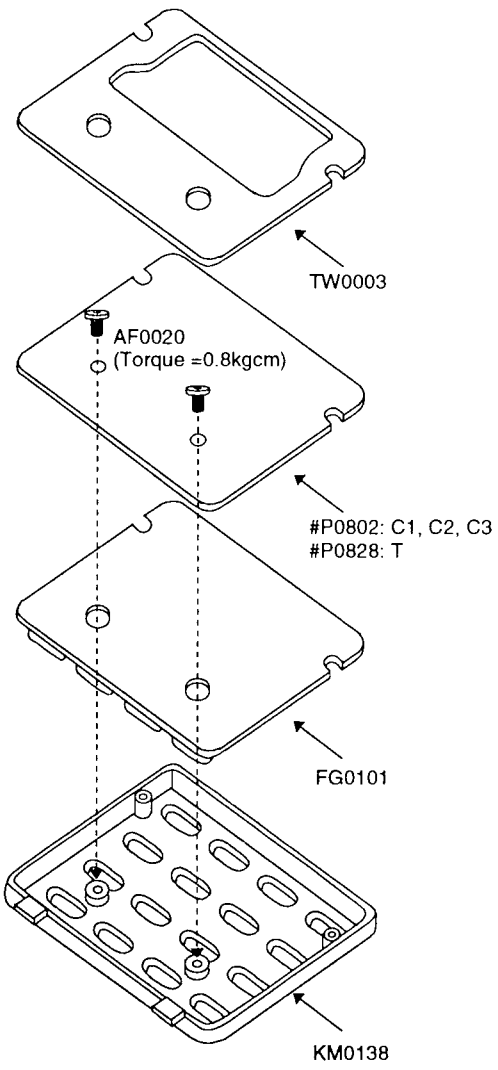


7) Ten Key Cover and Key Pad Panel

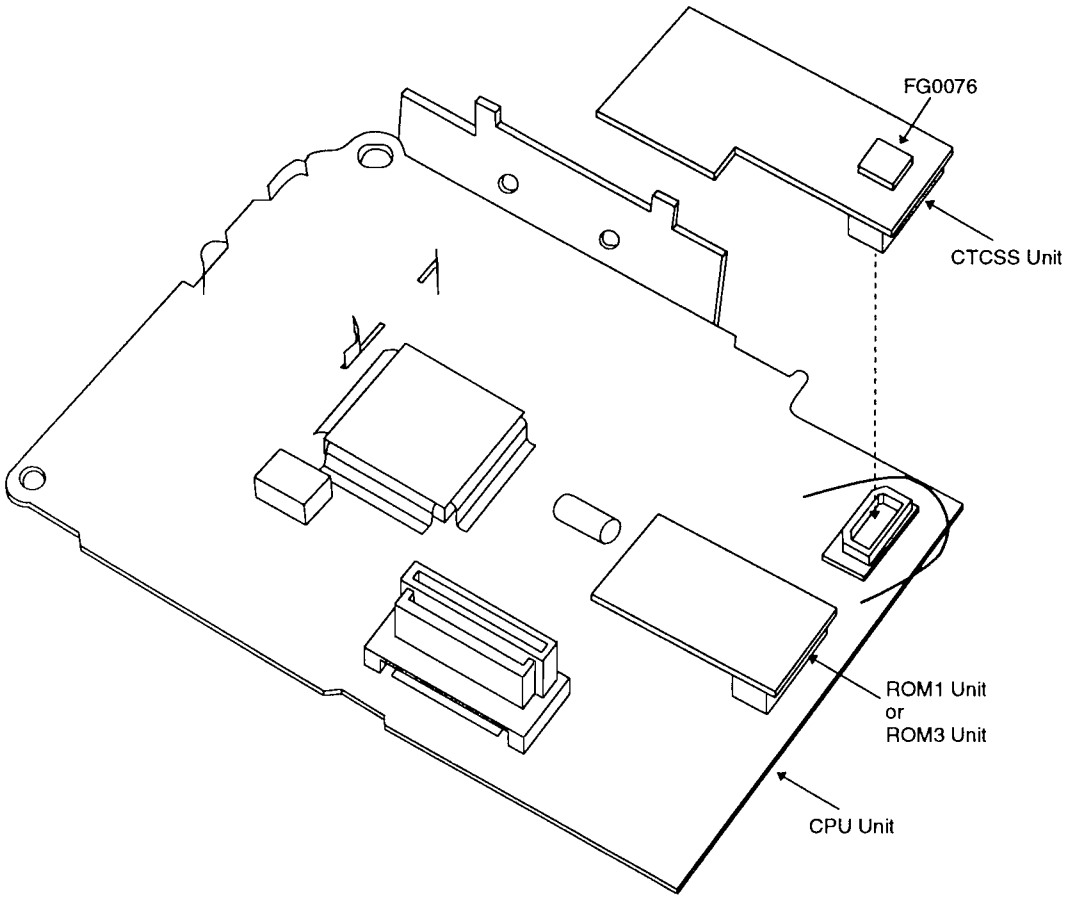
Ten Key Cover (E)



Key Pad Panel



8) CTCSS Unit and ROM Unit

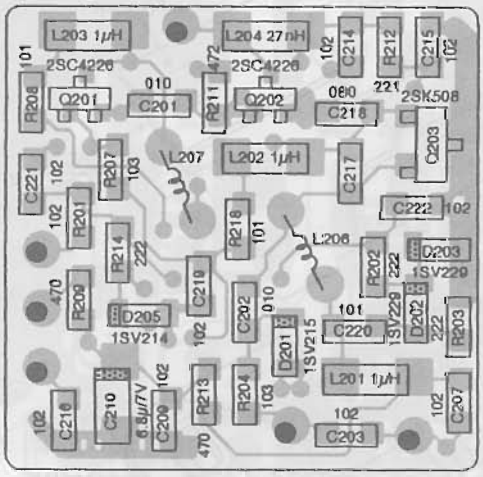


Model No.	DJ-480				
Destination	T	E	C1	C2	C3
CTCSS Unit	1	0	0	0	0
ROM1 Unit	1	1	0	0	0
ROM3 Unit	0	0	1	1	1

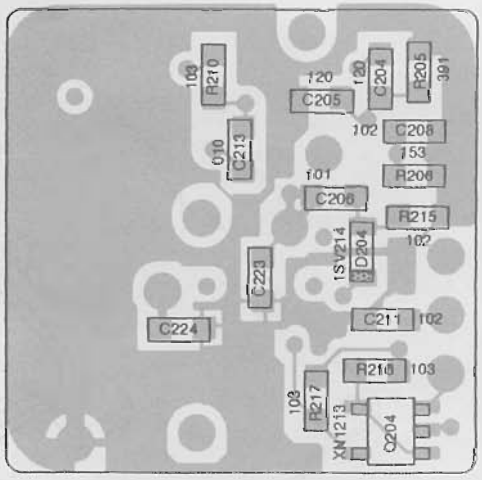
PC BOARD VIEW

1) VCO Unit

Side A



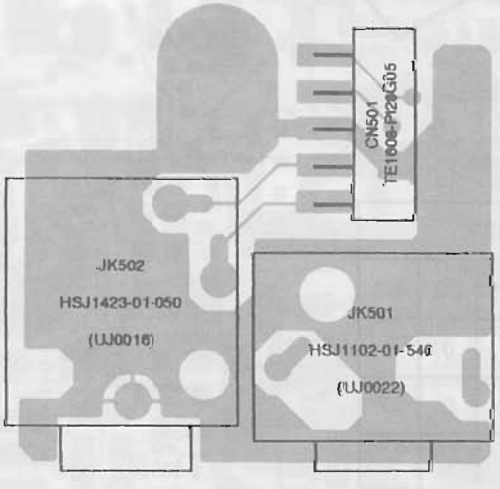
Side B



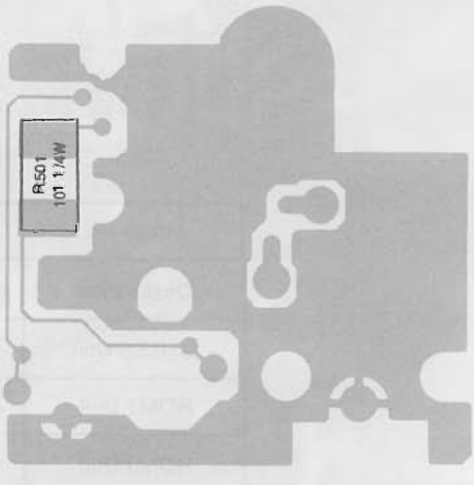
	C217	C223	C224	L206	L207
C1	5p	-	-	45B	45B (2.0 4.5T 0.5)
C2	5p	-	-	35B	35B (2.0 3.5T 0.5)
C3/T/E	6p	2p	2p	35B	35B (2.0 3.5T 0.5)

2) Jack Unit

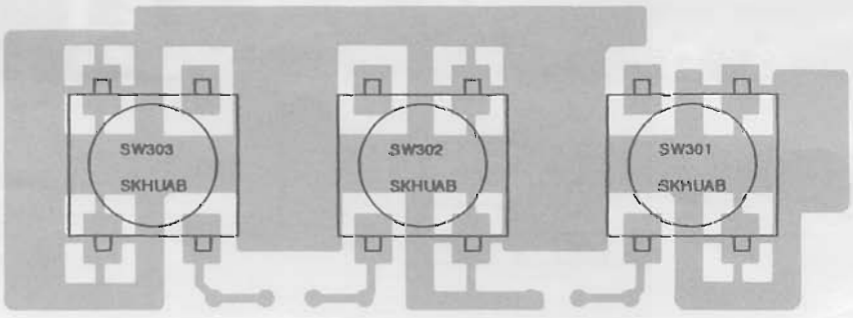
Side A



Side B



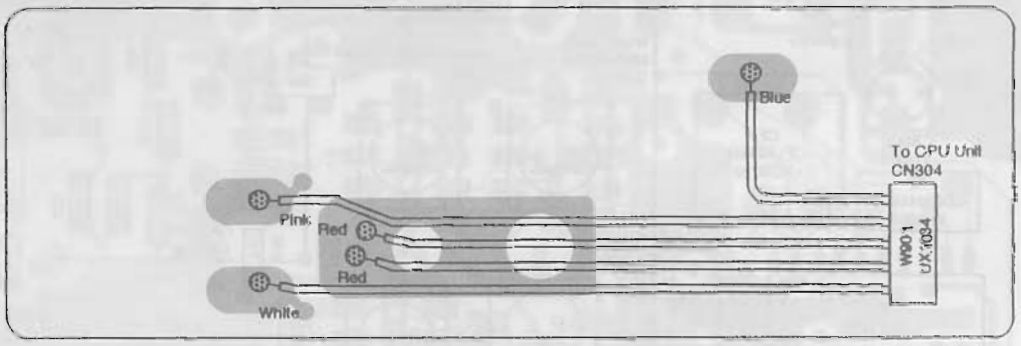
3) PTT Unit Side B



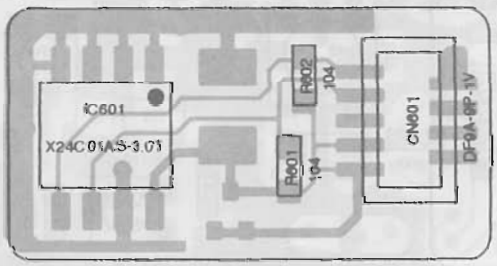
4) PS Unit

Side A

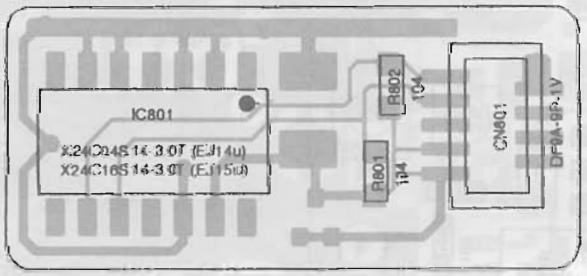
Side B



5) ROM1 Unit Side B



6) ROM2 Unit Side B (EJ-14u / EJ- 15u)



7) ROM3 Unit Side B (C1/C2/C3 only)