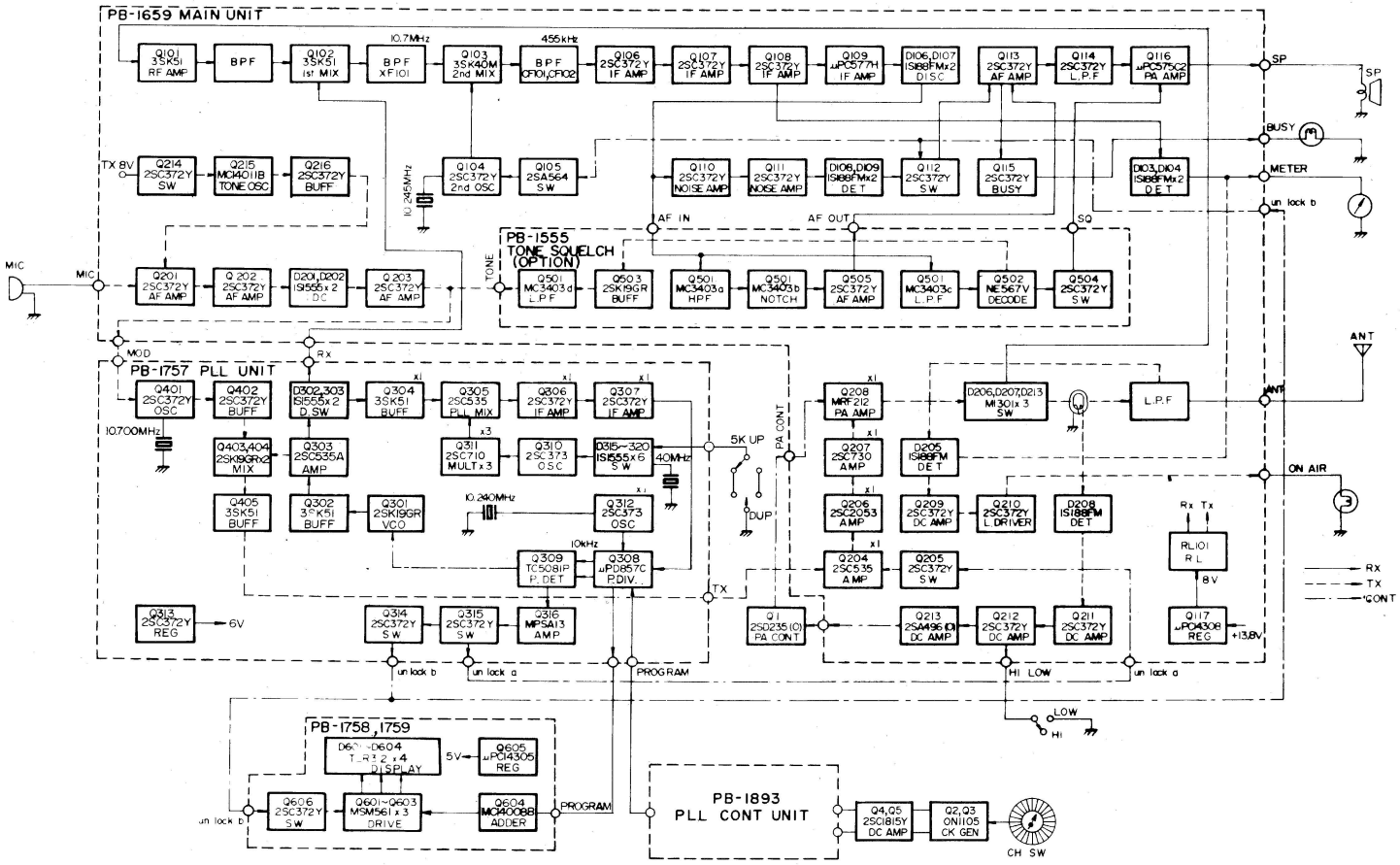


FT-227RB MEMORIZER BLOCK DIAGRAM

The digital phase comparator, Q_{309} (TC5081P), compares the phase of the PLL IF signal with that of the reference signal, and any difference is converted into an error-correcting voltage. This error-correcting voltage is fed to varactor diode D_{301}, which changes the output signal phase to lock with that of the reference signal.

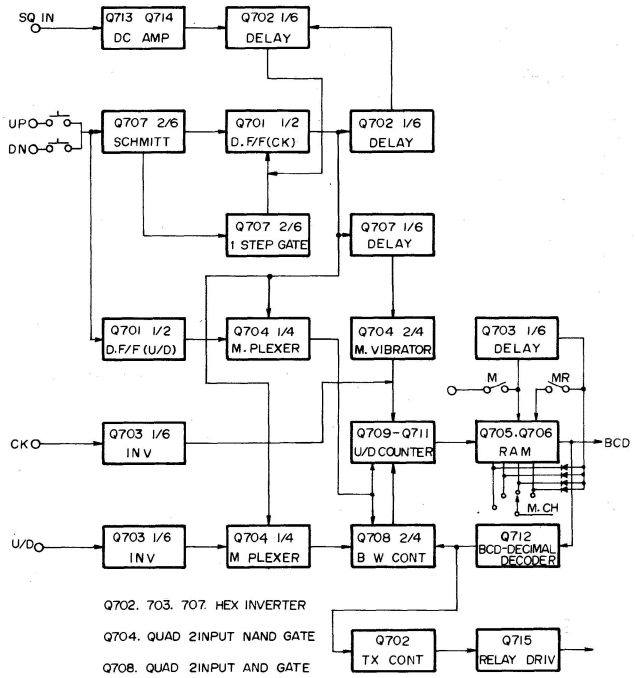
When the VCO is locked, the constant voltage at pin 4 of Q_{309} is applied to Q_{316} (MPSA13), causing it to conduct; in turn, Q_{315} (2SC372Y) cuts off. The H voltage at the collector of Q_{315} causes Q_{205} (2SC372Y) to conduct, supplying DC voltage to exciter stages Q_{204} and Q_{206}. When the VCO is unlocked, the DC voltage at the emitter of Q_{205} drops, preventing normal operation of Q_{204} and Q_{206}.

The output voltage from Q_{315} is reversed in polarity by Q_{314} (2SC372Y), and applied to Q_{606} (2SC372Y), keeping the collector of Q_{606} at the H level, in order to drive Q_{601}–Q_{603} (MSM561) for the display of the channel frequency. The voltage is also applied to Q_{105} (2SA564), which supplies DC voltage to the second heterodyne oscillator, Q_{104} (2SC372Y).

When the VCO is unlocked, the collector of DC voltage drops, causing the LEDs to turn off. Simultaneously, the second heterodyne oscillator ceases to oscillate. The receiver is thus muted until VCO lock occurs.

PLL CONTROL UNIT

Please refer to the PLL Control Unit logic diagram for questions regarding the operation of this circuitry. A complete treatment of every logic state is beyond the scope of this manual.



Crystal	Frequency	PLL Het. Freq.	Remarks
X301	44.10000 MHz	132.300 MHz	Simplex
X302	43.90000 〃	131.700 〃	TX –600 kHz shift
X303	44.30000 〃	132.900 〃	TX +600 kHz shift
X304	44.10166 〃	132.305 〃	Simplex 5 kHz up
X305	43.90166 〃	131.705 〃	TX –600 kHz 5 kHz up
X306	44.30166 〃	132.905 〃	TX +600 kHz 5 kHz up

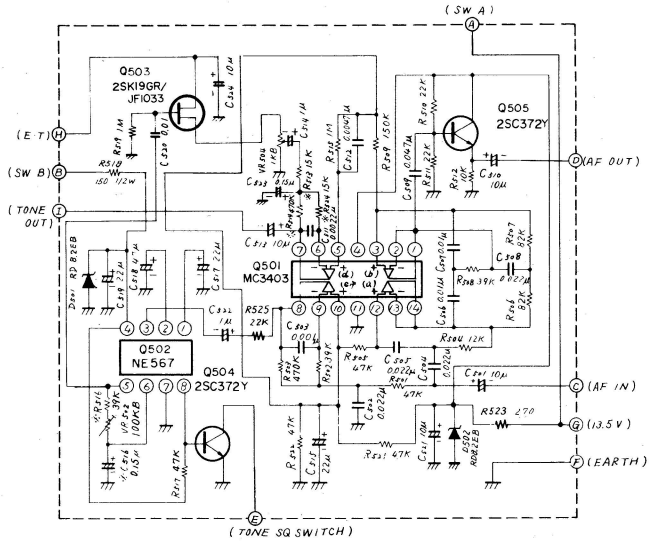
POWER SUPPLY

A 13.8 volt DC supply is used for the audio power amplifier, Q_{116}, as well as the relay and lamps. The supply voltage for the final amplifier is fed through voltage regulator Q_1 (2SD235D), which is controlled by the automatic final protection unit.

Voltage regulator Q_{605} (μPC14305) regulates the supply voltage at 5 volts, to supply Q_{308} and the display unit. Q_{313} (2SC372Y) and D_{301}(RD6.8EB) regulates the supply voltage at 6 volts for the VCO and phase comparator. The 5 volt supply for the PLL control unit is regulated by zener diode D_3 (WZ050), and is connected directly (not via the power switch) for memory backup purposes.

A regulated 8 volt circuit using Q_{117} (μPC14308) is used for all other circuits.

When the transceiver is used in the memory mode, D_4 and D_5 (WZ050) supply 5 volts to the receiver and transmitter, respectively.



TONE SQUELCH (PB-1555A) OPTION

	C516*	R516*	R513*	R514*	R524*
70Hz / 160Hz	0.15μF	39KΩ	15KΩ	470KΩ	15KΩ
160Hz / 250Hz	0.1μF	33KΩ	8.2KΩ	270KΩ	8.2KΩ

Table 2

TONE SQUELCH UNIT (OPTION)

The tone squelch circuit disables the audio circuit of the receiver until a preset, subaudible tone is received. On transmit, a subaudible tone is superimposed on the output audio signal. The frequency of this tone can be set to any frequency between 70 Hz and 250 Hz.

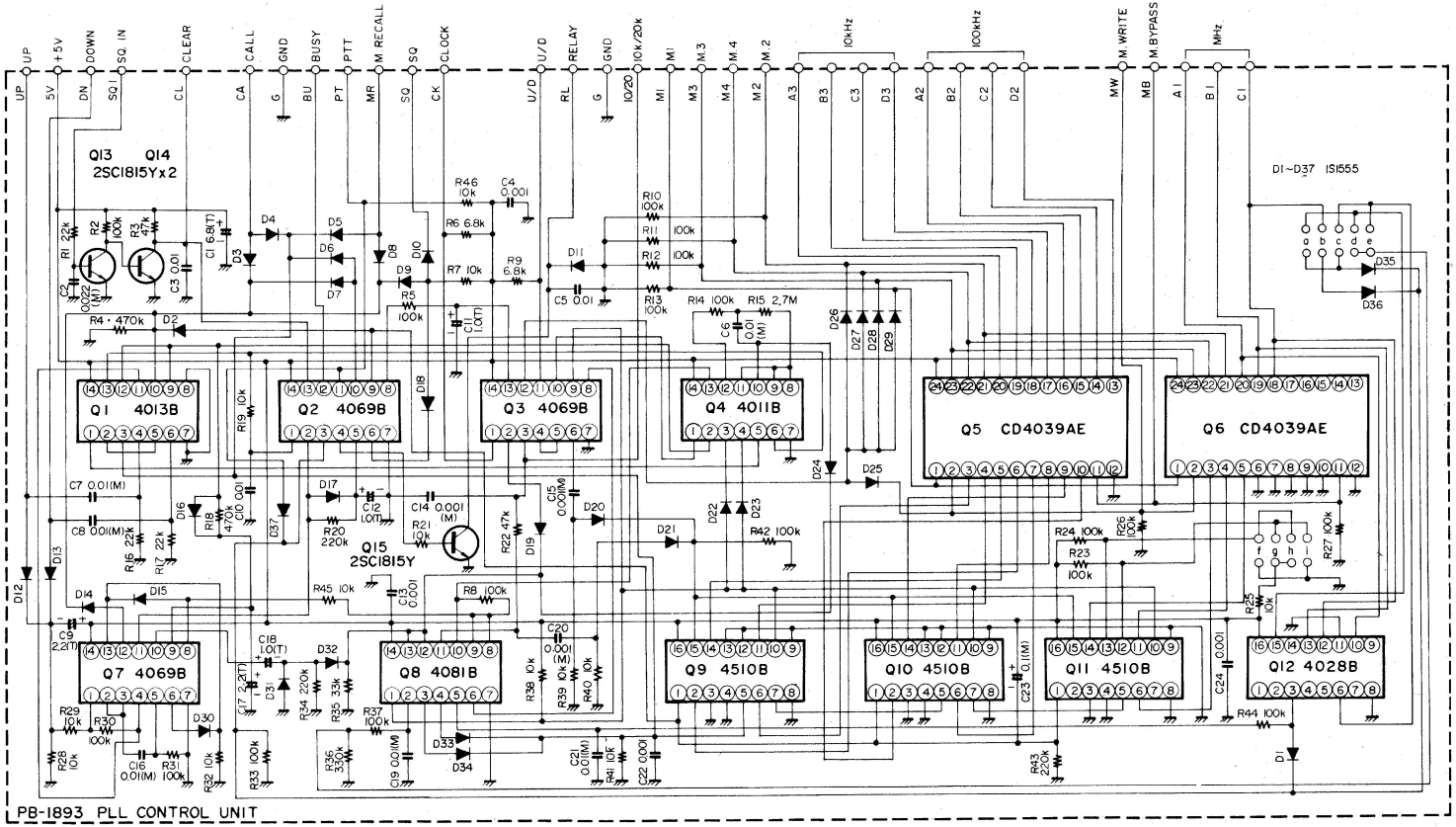
The tone signal is generated by Q_{502} (NE567), and its frequency is set by R_{516}, VR_{502}, and C_{516}. The level of the tone signal is set by VR_{504}, and the signal is subsequently fed through buffer amplifier Q_{503} (2SK19GR) to a low pass filter on unit "d" of operational amplifier Q_{501} (MC3403). The tone signal is then superimposed on the speech signal at Q_{202}. The constants for setting the subaudible tone frequency are shown in Table 2.

The audio output signal from the receiver discriminator is fed to unit "a" of Q_{501}. Unit "a" of Q_{501} acts as a high-pass filter, while unit "b" acts as a T-notch filter. These filters remove the subaudible tone from the audio signal, which is then fed through audio amplifier Q_{505} (2SC372Y) to amplifier Q_{113}.

The subaudible tone then passes through a low-pass filter at unit "c" of Q_{501}, and is fed to Q_{502}. When the tone frequency is the same as that preset for transmission, the voltage at pin 8 of Q_{502} becomes low, causing Q_{504} (2SC372Y) to turn off. In turn, proper bias voltage is applied to Q_{119}, allowing normal operation.

When the proper tone signal is not present, Q_{504} conducts, removing the bias from Q_{119}, thus disabling the audio circuit.

As the conventional carrier-controlled squelch is still in operation, irrespective of the condition of the tone squelch, the BUSY lamp will light up when any carrier is received. This feature alerts the operator that the channel is occupied, though no signal may be heard.



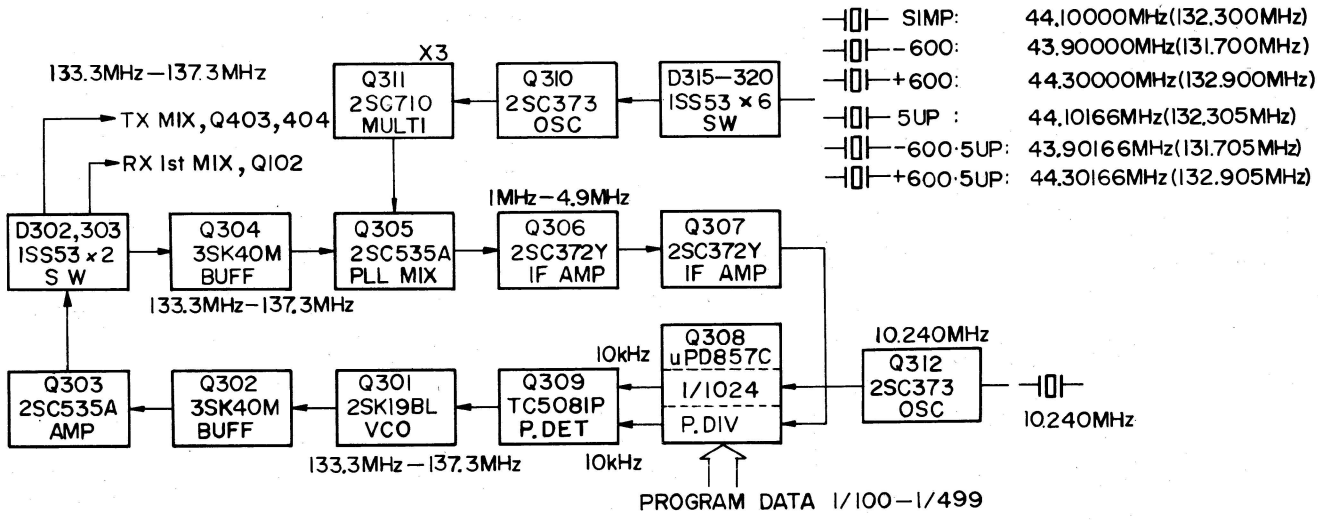
PLL CONTROL UNIT PB-1893

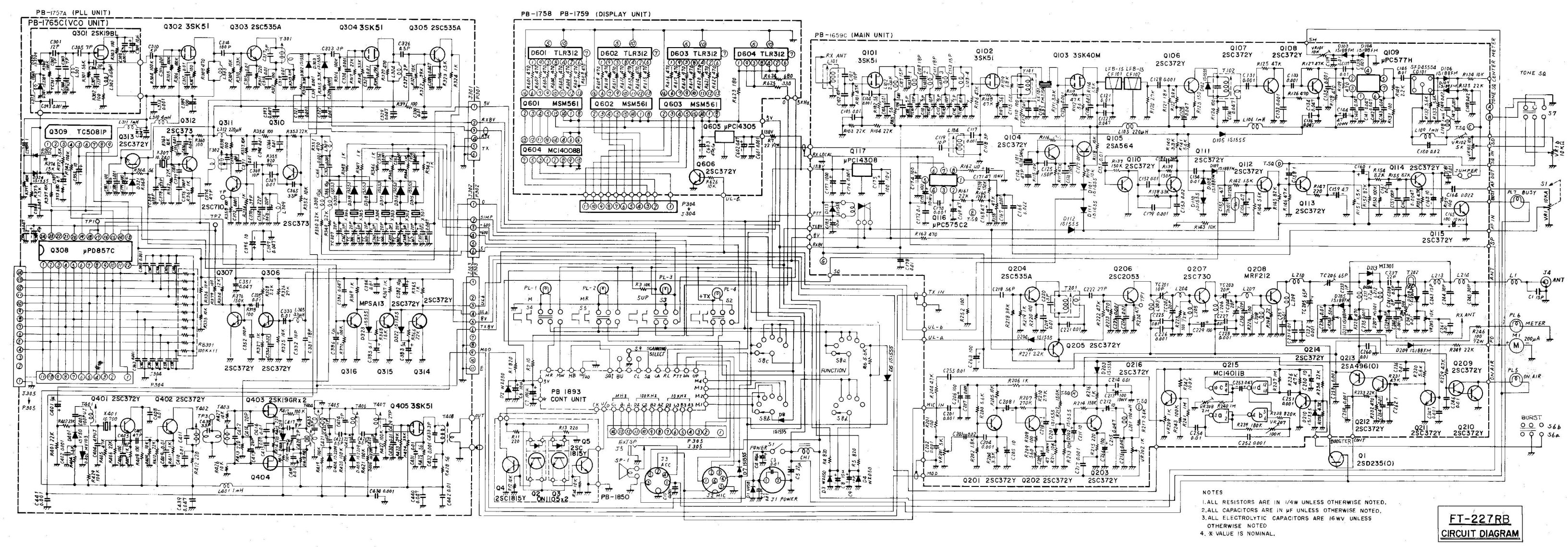
CRYSTAL DATA FT-227RB

FUNCTION	HOLDER	RANGE (MHz)	MODE	LOAD C	SERIES R	DRIVE LEVEL
REFERENCE (X_{407})	HC-18/U	10.240	Fundamental	30 pF	25 Ω	2 mW
2nd Local (X_{101})	HC-18/U	10.245	Fundamental	30 pF	25 Ω	2 mW
Carrier (X_{401})	HC-18/U	*10.700	Fundamental	30 pF	20 Ω	2 mW
PLL Local (X_{301})	HC-18/U	44.100	3rd overtone	20 pF	40 Ω	2 mW
PLL Local (X_{302})		43.900				
PLL Local (X_{303})		44.300				
PLL Local (X_{304})		44.10166				
PLL Local (X_{305})		43.90166				
PLL Local (X_{306})		44.30166				

*ACTUAL FREQUENCY: 10.740 MHz
Load Capacitor: 30 pF, 40 kHz UP (Decided by circuit)

PLL CIRCUIT FREQUENCY RELATIONS





NOTES

1. ALL RESISTORS ARE IN 1/4W UNLESS OTHERWISE NOTED.
2. ALL CAPACITORS ARE IN μF UNLESS OTHERWISE NOTED.
3. ALL ELECTROLYTIC CAPACITORS ARE 16WV UNLESS OTHERWISE NOTED
4. ※ VALUE IS NOMINAL.

FT-227RB
CIRCUIT DIAGRAM