Technical Manual

SSB Main Receiver
DEBEG 2000

DEBEG

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DEBEG

INSTALLATION AND OPERATION MANUAL
FOR
DEBEG MODEL 2000
RECEIVER

DEBEG GMBH
BEHRINGSTRASSE 120
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DEBEG
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ESB EMPFÄNGER DEBEG 2000

Bedienungsanleitung

1. FUNKTION DER BEDIENUNGS- UND ANZEIGE-ELEMENTE

BATT	Sicherung für 24 V-Speiseleitung
MAIN	Sicherung für 110/220 V-Speiseleitung
BATT OPER	Anzeigelampe, leuchtet auf bei 24 V-Betrieb
PHONES	Kopfhörer zum Anschluß von nieder- oder hochohmigen Kopfhörern mit 6 mm-Klinkenstecker, mit Abschaltkontakt für den eingebauten, jedoch nicht für den externen Lautsprecher
SPEAKER OFF	Kippschalter zum Abschalten des eingebauten Lautsprechers
0 bis 9	Drucktasten zur Eingabe der Empfangsfrequenzen und Speicherplätze
500	Drucktaste zur Schnellwahl der MW-Notfrequenz 500 kHz
2182	Drucktaste zur Schnellwahl der GW-Notfrequenz 2182 kHz
RCL	Drucktaste zum Abruf (RECALL) einer Frequenz aus dem Speicher
FREQ	Drucktaste zur Eingabe einer neuen Empfangsfrequenz
SCAN	Drucktaste zum Starten und Unterbrechen der Frequenzabtastung
STO	Drucktaste zur Eingabe einer Frequenz in den Speicher
CLR	Drucktaste zum Zurückschalten auf die vorher gespeicherte Frequenz oder zum Löschen von Eingabefehlern (CLEAR)
PRES	Drucktaste zum Ein- oder Ausschalten der Vorkreisabstimmung (PRESELECTOR). Diese kann zur Anpassung an die Antennenimpedanz oder zur Unterdrückung starker Störsignale benutzt werden und ist wirksam in den Frequenzbereichen 160 - 525 kHz und 1,6 - 30 MHz. Die Vorkreisabstimmung wird bei Eingabe einer neuen Frequenz automatisch abgeschaltet.
REM	Drucktaste zum Einschalten der Fernbedienung (REMOTE CONTROL). Diese Taste schaltet gleichzeitig alle Bedienelemente am Empfänger ab. Sie ist nur bei angeschlossenem Fernbediengerät wirksam.

FREQUENCY kHz — Anzeigefeld, 6-stellig, zur Anzeige der eingestellten Empfangsfrequenz oder des Speicherplatzes sowie folgender zusätzlicher Funktionsanzeigen:

FCN — (ab Gerät Nr. 137 FCN)
leuchtet nach jeder nicht abgeschlossenen (beendeten) Eingabe auf. Erlischt, wenn die Eingabe durch die entsprechende Taste beendet ist.

SCAN — leuchtet auf bei Abtastbetrieb, nach Drücken der SCAN-Taste.

ERROR — leuchtet auf bei Bedienungsfehlern am Drucktastenfeld.

SC/ON — leuchtet auf
a) nach Tastendruck SC/ON
b) bei Abruf eines Speicherplatzes über die RCL-Taste, wenn dieser in den SCAN-Betrieb eingespeichert ist. Es werden alle zur Abtastung eingegebenen Speicherplätze, die über die RCL-Taste abgerufen werden, angezeigt.

S-METER — Drehspulinstrument zur Anzeige der relativen Stärke des Empfangssignales bei eingeschalteter automatischer Verstärkungsregelung (AVR).

BW — 4 beleuchtete Drucktasten zur Wahl der ZF-Bandbreite

VN	VERY NARROW (sehr schmal)	: Bandbreite 0,3 kHz
N	NARROW (schmal)	: Bandbreite 1,0 kHz
I	INTERMEDIATE (mittel)	: Bandbreite 2,4 kHz oder SSB bei Mode A3A/A3J
W	WIDE (breit)	: Bandbreite 5,4 kHz

MODE — 4 beleuchtete Drucktasten zur Wahl der Demodulationsart

A1	Telegrafie (unmoduliert) in Verbindung mit Feinabstimmung (BFO)
A2H/A3H	Amplitudenmodulation Telegrafie moduliert/Einseitenband-Telefonie mit vollem Träger oder Zweiseitenband-Telefonie (A3).
A3A/A3J	Einseitenband-Telefonie (oberes Seitenband) in Verbindung mit der Feinabstimmung (CLARIFIER)
F1 (A7J)	Schmalband-Frequenzumtastung (FSK) Fernschreib-Betrieb in Verbindung mit SITOR-Gerät

DIMMER	Drehknopf zum Einstellen der Helligkeit der Leuchtanzeigen, der Leuchttasten und der Beleuchtung des Anzeige-Instruments (S-METER)
VOLUME-OFF	Drehknopf zur Lautstärke-Einstellung, kombiniert mit Drehschalter zum Ein- und Ausschalten des Empfängers.
SENSITIVITY	Drehknopf zum Einstellen der ZF-Verstärkung, ist wirksam bei ein- und ausgeschalteter automatischer Verstärkungsregelung. Durch Ziehen des Knopfes wird die AGC (AVR) abgeschaltet.
CLARIFIER/BFO	Drehknopf zur Feineinstellung der Frequenz bei A1, A2H, A3J, F1. Ziehbereich: $\geq\pm$ 150 Hz bei A2H, A3J, F1 $\geq\pm$ 1,5 kHz bei A1
PRESELECTOR	Drehknopf zur Vorkreisabstimmung. Dieser ist wirksam, wenn die rote Signallampe PRESELECTOR nach Drücken der Taste PRES aufleuchtet.
TUNE	Drehknopf mit Federvorspannung zum Abstimmen der Empfangsfrequenz. Diese steigt bei Rechts- und fällt bei Linksdrehung. Die Änderung der Frequenz erfolgt normalerweise in 100 Hz-Schritten, und zwar um so schneller, je weiter der Drehknopf TUNE nach links oder rechts aus seiner Mittellage verdreht wird. Bei der Betriebsart A2H und gedrückter Bandbreitentaste W erfolgt die Abstimmung in 1 kHz-Schritten. Die minimale Frequenzänderung beträgt 1 Schritt/sek., die maximale Änderung ca. 60 Schritte/sek.
Verweilzeit-Einstellung	für den Abtastbetrieb (SCAN-Taste gedrückt) läßt sich mit einem Schraubenzieher, der in die kleine Öffnung rechts neben der F1-Taste gesteckt wird, die gewünschte Verweilzeit von ca. 0,5 sek. bis ca. 15 sek einstellen.

2. ZUSAMMENFASSUNG DER BEDIENUNGSMETHODEN

A1-Betrieb

Für A1-Telegrafie-Empfang wird (bei bekannter Stationsfrequenz) die Frequenz über die numerische Tastatur eingegeben. Ist die gewählte Frequenz eine Seefunkfrequenz, so wird die dazu gehörige Sendeart (A1) und Bandbreite vom Empfänger automatisch gewählt. Die Bandbreiten(Filter) VN, N, I oder W können auch beliebig von Hand über die entsprechenden Drucktasten gewählt werden.

Das Frequenz-Display zeigt - unabhängig von der Einstellung des Reglers "Clarifier/BFO" - ständig die eingegebene, bzw. eingestellte Frequenz an. Der Drehknopf "Clarifier/BFO" (bei SSB-Empfang) wird in der Regel auf "Mitte" eingestellt und dient zur Feinabstimmung innerhalb der 100 Hz Schritte. Bei A1-Empfang kann mit diesem Drehknopf die gewünschte Tonfrequenz eingestellt werden.

Bei unbekannter Sendefrequenz kann das betreffende Seefunkband - nach Grobeinstellung der Frequenz mit der numerischen Tastatur - mit dem TUNE-Drehknopf abgesucht werden. Ist die Station gefunden und identifiziert, kann die Bandbreite beliebig von Hand gewählt werden. In den Frequenzbereichen 160 - 525 kHz oder 1605 - 30000 kHz kann die Vorkreisabstimmung (PRESELECTOR, Taste PRES) benutzt werden, um optimale Empfindlichkeit zu erzielen, oder um Störsignale zu unterdrücken. Dann Drehknopf PRESELECTOR auf größte Lautstärke bzw. maximale S-METER Instrument-Anzeige abstimmen. Bei A1-Empfang kann man die automatische Verstärkungsregelung (AGC) ein- oder ausgeschaltet lassen. Die Drehknöpfe SENSITIVITY und VOLUME (HF- und NF-Verstärkung) sind je nach Stärke des Empfangssignals und gewünschter Lautstärke einzustellen.

A2H/A3H-Betrieb (gilt auch für A3-Empfang

Die Frequenz der gewünschten Sendestation ist im allgemeinen bekannt und kann über das Drucktastenfeld eingegeben werden. Wenn nötig, (bei Frequenzen außerhalb der Seefunkbänder) wählt man manuell die Sendeart A2H/A3H und Bandbreite W (BREIT). Der Knopf CLARIFIER wird auf Mitte gestellt. Die angezeigte Frequenz entspricht genau der empfangenen Sendefrequenz.

Wenn die Sendefrequenz unbekannt ist, dann kann das Frequenzband mit dem TUNE-Drehknopf bei Bandbreite W (BREIT) abgesucht werden. Wenn eine Station gefunden ist und der Empfänger nach Maximum-Anzeige des Abstimmindikators (S-METER) abgestimmt ist, kann danach auch eine schmalere Bandbreite (I oder N) gewählt werden.

Die automatische Verstärkungsregelung (AGC) läßt man normalerweile eingeschaltet, wobei der Knopf SENSITIVITY auf Rechtsanschlag und der Knopf VOLUME auf die gewünschte Lautstärke eingestellt wird.

A3A/A3J-Betrieb (Einseitenband-Telefonie, oberes Seitenband)

Die Frequenz der gewünschten Station ist im allgemeinen bekannt und kann über das numerische Tastenfeld eingegeben werden. Bei Seefunkfrequenzen erfolgt die Wahl der Sendeart (A3J) und der Bandbreite (I) automatisch, außerhalb der Seefunkbänder manuell über die entsprechenden BW/MODE-Drucktasten. Der Knopf CLARIFIER wird auf 'Mitte' gestellt.

In diesem Abstimmzustand des Empfängers entspricht die im Leuchtziffernfeld angezeigte Empfangsfrequenz der Trägerfrequenz (des unterdrückten Trägers) der empfangenen Sendestation.

Bei unbekannter Stationsfrequenz sucht man diese mit dem Drehknopf TUNE, wie unter Sendeart A3H beschrieben. TUNE und CLARIFIER sind auf optimale Sprachqualität abzustimmen.

In den Frequenzbereichen der KW-Seefunkbänder (4-22MHz) werden bei der Frequenzeingabe automatisch die zugehörigen Duplexfilter eingeschaltet, die die entsprechenden Sendefrequenzen unterdrücken sollen.
Die Vorkreisabstimmung (PRESELECTOR) wird normalerweise nicht benutzt, kann jedoch zur Erzielung optimaler Empfindlichkeit oder in jedem beliebigen Frequenzband zur Störfrequenzunterdrückung verwendet werden, wie im Abschnitt A1-Betrieb beschrieben.

Der Drehknopf SENSITIVITY kann etwas nach links gedreht werden, wenn starke Signale empfangen werden, um das Hochrauschen des Empfängers in den Sprechpausen bei eingeschalteter AVR (AGC) zu vermeiden.

A7J-Betrieb (SITOR-Telex)

Die Einstellung des Empfängers erfolgt wie bei A3J-Betrieb (SSB).

F1-Betrieb (FSK-Telex)

Der Empfang von F1-Fernschreibsignalen ist möglich, wenn der Empfängerausgang AUDIO LINE (Rückseite des Gerätes) an ein SITOR-Zusatzgerät angeschlossen wird. Der direkte Anschluß einer Fernschreibmaschine an den Empfänger ist nicht möglich, da dieser keinen eingebauten F1-Demodulator besitzt. Die Abstimmung des Empfängers erfolgt wie bei SSB-Betrieb (A3J), wenn erforderlich, kann eine Feinabstimmung mit Hilfe des Drehknopfes CLARIFIER erfolgen.

Für die Vorkreisabstimmung gelten die im Abschnitt A3A/A3J genannten Möglichkeiten. Die AGC bleibt eingeschaltet.

Empfänger DEBEG 2000 Bedienung (Kurzform), ohne Tune - Lampe.

A

Frequenz - Eingabe

Reihenfolge	Taste
1.)	Ziffern (in kHz, mit 100Hz-Stelle)
2.)	FREQ.

(BW und Mode wie erwünscht)

B

Frequenz, BW und Mode - Eingabe in Speicher (Store)

Reihenfolge	Taste
1.)	Nr. des Stores (30 Plätze)
2.)	STO

C

Frequenz, BW und Mode-Abruf aus Speicher (Store)

Einzel-Abruf

Reihenfolge	Taste
1.)	Nr. des Stores
2.)	RCL

durchgehender Abruf

Taste RCL

Nach jedem Tastendruck erscheint die Store Nr. und hiernach der in diesem Store gespeicherte Inhalt.

D

Eingabe der Speicherplätze mit ihrem Inhalt zur Abtastung (SCAN)

Reihenfolge	Taste	Anzeige:
1.)	Nr. des Stores	Store Nummer und Lampe FCN (Function) leuchtet.
2.)	RCL	Lampe FCN erlischt, Freq., BW + Mode aus gewähltem Store.
3.)	SC/ON	Lampe SC/ON leuchtet.
4.)	RCL	Lampe SC/ON erlischt.

Es erscheint das im nächsten Store Eingegebene !

E

Abtastung (SCAN) der Speicherplätze (inklusive Inhalt)

Start: Taste: SCAN

Stop: Taste: SCAN bei gewünschter Freq.

F

Löschung der Speicherplätze mit ihrem Inhalt von der Abtastung (SCAN)

Reihenfolge	Taste	Anzeige:
1.)	Nr. des Stores	Lampe FCN leuchtet, Store Nr.
2.)	RCL	Lampe FCN erlischt, Lampe SC/ON leuchtet, Freq., BW + Mode aus gewähltem Store.
3.)	SC/ON	Lampe SC/ON erlischt.
4.)	RCL	Es erscheint der nächste Store-Inhalt

Änderung des Speichers, wie BW + Mode zur Frequenz

Reihenfolge	Taste
1.)	neue, gewünschte BW und Mode
2.)	Nr. des Stores der Frequenz
3.)	STO

Eingabeänderungen (Freq. oder BW oder Mode) innerhalb eines zur Abtastung eingegebenen Speicherplatzes löscht diesen Speicherplatz von der Abtastung! Neueingabe: siehe unter D.

Hinweise zu C, D 4.) und F 4.):

Die Lampe SC/ON leuchtet bei jeder Store-Nr. (und dessen Inhalt), die zur Abtastung (SCAN) eingegeben ist.

Empfänger 2000, mit Tune - Lampe und Tune - Taste

A

Frequenz - Eingabe

Reihenfolge	Taste
1.)	FREQ
2.)	Ziffern (in kHz, mit 100 Hz Stelle)
3.)	FREQ

B

Frequenz - Eingabe+Mode+BW in Speicher (Store)

Reihenfolge	Taste
1.)	STO
2.)	Nr. des Stores (30 Plätze)
3.)	STO

C

Frequenz - Abruf aus Speicher (Store)

Reihenfolge	Taste
1.)	RCL
2.)	Nr. des Stores
3.)	RCL

D

Eingabe der Speicherplätze (Stores) zur Abtastung (Scan)

Reihenfolge	Taste
1.)	RCL
2.)	Nr. des Stores (z.B. 3 von 30)
3.)	Scan

E

Frequenz - Abtastung

Start: Taste: Scan

Stop : Taste: Scan, bei gewünschter Frequenz.

Wenn Abtastung zu langsam: durch 2-maliges, schnelles drücken der Taste Scan rückt die nächste zur Abtastung eingegebene Frequenz vor.

F

Löschung der Abtastung

Es werden alle zur Abtastung eingegebenen Speicherplätze (Stores) von der Abtastung gelöscht.

(Neueingabe: siehe unter D)

Die Belegung der Speicherplätze (1 - 30) mit ihren Frequenzen bleibt erhalten.

Reihenfolge	Taste
1.)	CLR
2.)	RCL
3.)	SCAN (gedrückt halten)
4.)	CLR

3. SSB Main Receiver DEBEG 2000 - Operation Table

3a. Without TUNE Lamp and TUNE Key
(from Serial No. 137 upwards)

A — Frequency Entry

Sequence	Key
1.	Numeric keys (in kHz, with 100 Hz digit)
2.	FREQ.
3.	Change BW and MODE (if necessary)

B — Frequency, BW and MODE-Entry into Memory (Store)

Sequence	Key
1.	No. of Store (30 memory locations)
2.	STO

C — Frequency, BW and MODE - Recall from Memory (Store)

Single Recalling

Sequence	Key
1.	No. of Store
2.	RCL

Step-by-step Recalling (several stores)

Sequence	Key	Remarks
1.	RCL	After each pressing
2.	RCL	of RCL the display
3.	RCL	will show the Store No. and then the stored frequency

D — Entry of Memory Locations (Stores) with their contents for Scanning (SCAN)

Sequence	Key	Display
1.	No. of Store	Store No. and Lamp FCN (FUNCTION) lights up
2.	RCL	Lamp FCN off, Frequ. BW+MODE of selected Store
3.	SC/ON	Lamp SC/ON lights up
4.	RCL	Lamp SC/ON off The entered data of next Store is displayed

E — Scanning (SCAN) of Memory Locations (Stores) with their entered contents (FREQ, BW, MODE)

Start: Key: SCAN | Stop: Key: SCAN, at wanted frequency.

F

Clearing of Memory Locations (Stores) with their contents from scanning (SCAN)

Sequence	Key	Display
1.	No. of Store	Lamp FCN and Store No. light up
2.	RCL	Lamp FCN off, Lamp SC/ON lights up, Frequ., BW+MODE of selected Store No.
3.	SC/ON	Lamp SC/ON off
4.	RCL	Data contents of next Store No. is displayed.

Remarks to A, B: Changing of stored data such as BW or MODE for a stored frequency:

Sequence	Key
1.	new, wanted BW and MODE function keys
2.	No. of Store of the entered frequency
3.	STO

Changing of data entries (Frequ. or BW or MODE) for a memory location store which has been entered for scanning (SCAN) will clear the scanning of this store! New entry: see section D.

Remarks to C, D4.) and F4.):
The lamp SC/ON lights up at each Store No. (and its content), which has been entered for scanning (SCAN) by D1.) ...4.)

3. SSB Main Receiver DEBEG 2000 - Operation Table

3b. With TUNE lamp and TUNE key (up to Serial No. 136)

A

Frequency Enter

Sequence	Key
1.	FREQ
2.	Numeric keys (in kHz, with 100 Hz digit)
3.	FREQ

B

Frequency, wanted BW and MODE-Entry into Memory (Store)

Sequence	Key
1.	STO
2.	No. of Store (30 memory locations)
3.	STO

C

Frequency, BW and MODE - Recall from Memory (Store)

Sequence	Key
1.	RCL
2.	No. of Store
3.	RCL

D

Entry of Memory Locations with contents for scanning (SCAN)

Sequence	Key
1.	RCL
2.	No. of Store
3.	SCAN

E

Scanning of Memory Locations (Stores) with their entered contents (FREQ, BW, MODE)

Start: Key: SCAN | Stop: Key: SCAN, at wanted frequency

F

Clearing of Scanning (SCAN Mode)

All memory locations (Stores) entered for scanning will be cleared from the scanning. (New entry: see procedure D). The previous entry of frequencies, BW and MODE into the memory locations (Store 1-30) remains stored, as programmed in procedure B.

Sequence	Key
1.	CLR
2.	RCL
3.	SCAN (depress and hold)
4.	CLR

DEBEG 2000 VERSION A-I

Bis Seriennummer 136 / until Serial Number 136
Mat.Nr. o6o14o3
Version A: Standard (mit Tune Taste und Tune Lampe)
Version A: Standard (with Tune Key and Tune Lamp)

Mat.Nr. o611476
Version B: modifizierte Version A,für Küstenfunkstellen
Version B: modified Version A,for Coast Stations

Ab Seriennummer 137/ from Serial Number 137
Mat.Nr. o6112o4
Version C: Standard (ohne Tune Lampe, mit Taste SC/ON)
Version C: Standard (without Tune Lamp, with key SC/ON)

Mat.Nr. o61o8o1
Version D: modifizierte Version C, mit LSB Filter,Telex mit schmaler BW, usw.
Version D: modified Version C, with LSB Filter,Telex with narrow BW (N/VN) etc.

Mat.Nr. o611668
Version E: modifizierte Version D, für Küstenfunkstellen
Version E: modified Version D, for Coast Stations

Mat.Nr.: o613134
Version F: modifizierte Version C, ZF-Ausgang modifiziert
Version F: modified Version C, IF-Output modified

Mat.Nr. o613142
Version G: wie Version D, mit modifiziertem ZF-Ausgang
Version G: as Version D, with modified IF-Output

Mat.Nr. o6315o
Version H: wie Version E, mit modifiziertem ZF-Ausgang
Version H: as Version E, with modified IF-Output

Mat.Nr. o613169
Version I: wie Version E, mit Side-Tone-Eingang
Version I: as Version E, with Side-Tone-Input

Revisions

31 January 1983

As a result of the experience gained during the production to date of the 2000 Receiver, certain changes have been made in the unit to further optimize its performance. These changes are listed on these pages.

CHASSIS ASSEMBLY 101560

1. The cable shield connection to J7-10 is connected instead to J7-9.
2. Pins 1 and A of J9 are connected to ground.
3. An 8.2 uH inductor (part no. V30141-Z96-F835-*-B900) is in séries with the cable connection to J8-B.

RF FILTER BOARD ASSEMBLY 101594

1. C4 is 3 pF (part no. V30141-Z101-B30-*-B900).
2. C20 is 2 pF (part no. V30141-Z101-B20-*-B900).

PRESELECTOR BOARD ASSEMBLY 101591

1. C24 is 100 pF (part no. V30141-Z77-B101-*-B900).
2. C30 is 18 pF (part no. V30141-Z77-B180-*-B900).
3. R12 is 10 ohms (part no. V30141-Z1-A100-*-B900).
4. R12 and L12 are interchanged.
5. A 100 uH inductor (part no. V30141-Z96-B102-*-B900) is added from the junction of R12 and L12 to the ungrounded end of C29.
6. L3 and L4 are tunable coils.

FIRST MIXER ASSEMBLY 101648

1. Mixer A1 is part no. V30141-Z114-A1-*-B900.

38MHZ IF BOARD ASSEMBLY 101588

1. C4 is part no. V30141-Z101-L270-*-B900.
2. C16, 18-20, 25, 30-31, 34-35 are part no. V30141-Z79-E104-*-B900.
3. C32 is 3 pF (part no. V30141-Z101-B30-*-B900).

4. L11 is 3.9 uH (part no. V30141-Z96-B395-*-B900).
5. R22 is 390 ohms (part no. V30141-Z1-A391-*-B900).
6. A capacitor C38, 27 pF (part no. V30141-Z77-B270-*-B900) is connected from the junction of R12 and R13 to ground.

1.4MHZ IF FILTER ASSEMBLY 101570

1. C2-4, 6-12, 15-20 are part no. V30141-Z79-E104-*-B900.

1.4MHZ IF/DEMOD ASSEMBLY 101585

1. L2 is 5.6 uH (part no. v30141-Z96-B565-*-B900).
2. R8 is 56 ohms (part no. V30141-Z1-A560-*-B900).
3. R40 is 18K ohms (part no. V30141-Z1-A183-*-B900).
4. R41 is 25K ohms (part no. V30141-Z75-F253-*-B900).
5. U10 is part no. V30141-Z76-A380-*-B900.
6. R44 is a 4.7K ohms resistor (part no. V30141-Z1-A472-*-B900) connected between U12-11 and U12-16.

REFERENCE BOARD ASSEMBLY 101573

1. C23 and C25 are selected at test (150pF, 270pF, 330pF or 470pF).
2. L11 is 3.9 uH (part no. V30141-Z96-B395-*-B900).
3. R43 is 220 ohms (part no. V30141-Z1-A221-*-B900).
4. R44 is 100 ohms (part no. V30141-Z1-A101-*-B900).
5. R44 is returned to +5V, not ground.

PROGRAMMABLE DIVIDER ASSEMBLY 101576

1. R3 is 2.2K ohms (part no. V30141-Z1-A222-*-B900).
2. A220 ohm resistor (part no. V30141-Z1-A221-*-B900) is in series with L2.

VCO BOARD ASSEMBLY 101579

1. C4 is 33 pF (part no. V30141-Z77-B330-*-B900).
2. C60 is 150 pF (part no. V30141-Z77-B151-*-B900).
3. C61 is 1000 pF (part no. V30141-Z77-B102-*-B900).
4. L1 is 6.8 uH (part no. V30141-Z96-B685-*-B900).
5. L21 is replaced by a jumper.

6. R3 is 2.7K ohms (part no. V30141-Z1-A272-*-B900).
7. R4 is 1.5K ohms (part no. V30141-Z1-A152-*-B900).
8. R23 is 1K ohms (part no. V30141-Z1-A102-*-B900).
9. Certain circuitry is altered as in figure R-1. The following are the part numbers of the added components:

   C67-33 pF capacitor - V30141-Z77-B330-*-B900
   C68-150 pF capacitor - V30141-Z77-B151-*-B900
   FL2 Ceramic filter - V30141-Z60-B2-*-B900
   L28 1.5 uH inductor - V30141-Z96-B155-*-B900
   L26, L27 .22 uH inductors - V30141-Z96-A224-*-B900
   R62 1.0K ohm resistor - V30141-Z1-A102-*-B900

CHASSIS INTERCONNECTION BOARD ASSEMBLY 101603

1. C19, C20, and C21 are deleted.
2. R2 is 3.0K (part no. V30141-Z1-A302-*-B900).
3. R5 is 270 ohms (part no. V30141-Z1-B271-*-B900).
4. A .01 uF capacitor (part no. V30141-Z41-H1-*-B900) is connected from pin A of J2 to ground.
5. A 4.7K resistor (part no. V30141-Z1-A472-*-B900 is connected between J9-H and J9-B and between J9-F and J9-B.

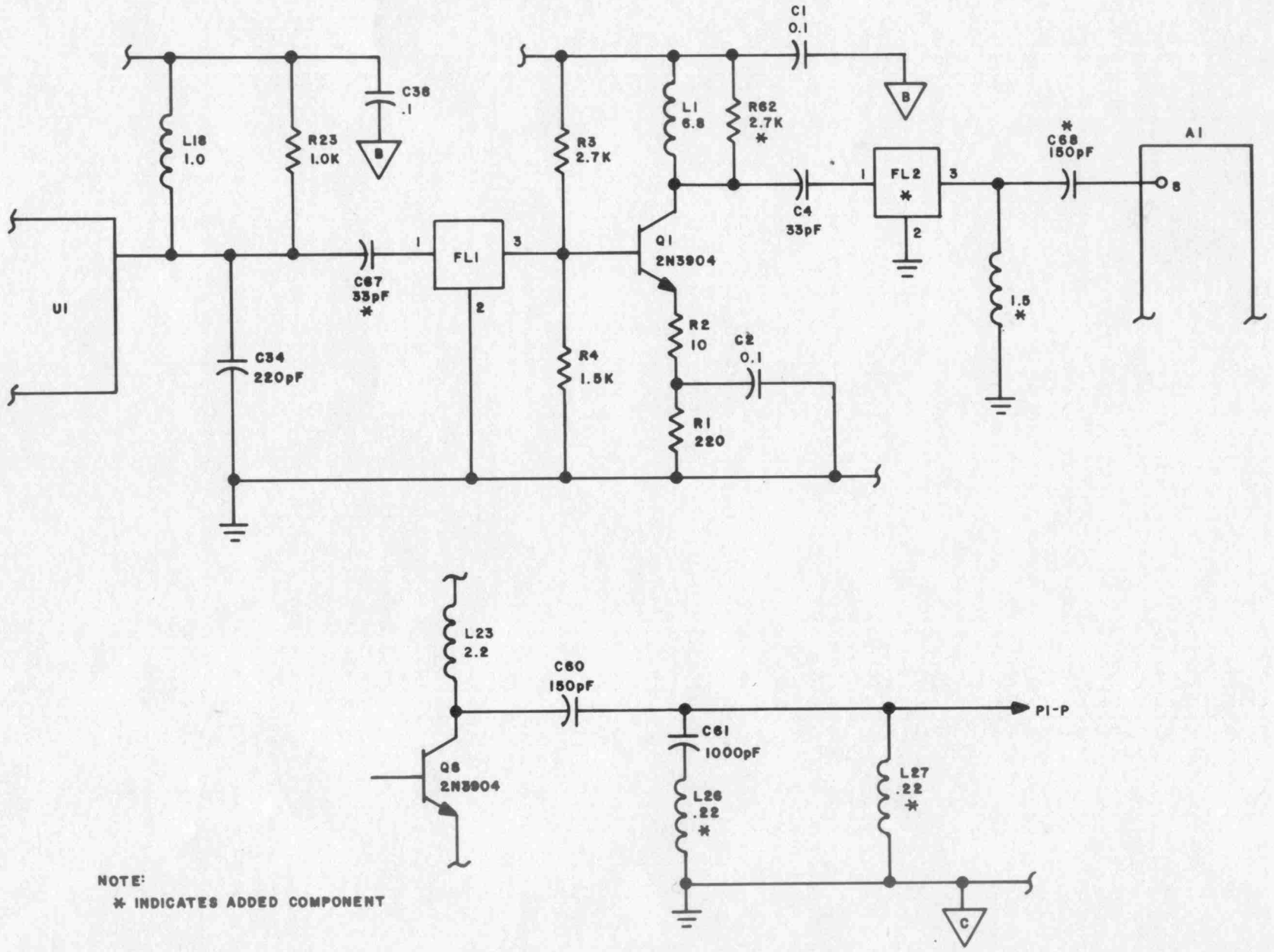

Figure R-1 Circuitry Revision to VCO Board Assembly 101579

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LIST OF ILLUSTRATIONS

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SECTION 1
GENERAL INFORMATION

1.1 INTRODUCTION

This manual describes the DEBEG Model 2000 Receiver which represents the latest state of the art for communications receivers. In addition to the primary goals of receiver performance, a major emphasis in the design has been placed on convenience of operation. The 2000 receiver is shown in figure 1-1.

1.2 FUNCTIONAL DESCRIPTION

The 2000 receiver is a high-performance, low cost fully synthesized, microprocessor based unit capable of reception and demodulation of CW, AM, SSB, and FSK transmissions in the frequency range from 10 kHz to 30 MHz. The unit incorporates keyboard entry of frequency, mode and bandwidth, as well as a unique form of manual tuning for convenient yet versatile operation. Correlation between tuned frequency, RF band, mode and IF bandwidth is fully automatic (although manual selection is also possible), minimizing the number of operations a user must perform to change frequency or mode of operation. Additionally, up to 30 commonly used operating frequency/mode/bandwidth combinations may be operator stored for convenient, rapid recall and the receiver is further capable of automatic scanning of any or all of these combinations. The unit incorporates built-in antenna matching, a built-in speaker, is capable of full remote operation and may be operated from both AC or DC power sources with automatic switching to DC in the event of an AC line failure.

1.3 PHYSICAL DESCRIPTION

The receiver is a rack mounted unit 133mm h x 483mm w x 349mm deep. The receiver consists of a front panel assembly, a main chassis, a pc interface board and plug-in printed circuit

boards for the RF/IF/audio path, the synthesizer and the microprocessor. The main chassis contains the power transformer, the power supply circuit boards, connectors for both the RF/IF/audio path and the synthesizer, some interconnecting wiring, and the rear panel mounted connectors, as well as the speaker, phone jack and fuses. The front panel assembly contains the keyboard and displays and their interface logic, and the manual tuning control. The interface board contains the majority of the front panel controls, as well as the power regulators and mating connectors for the plug-in pc boards.

Figure 1-1 Model 2000 Main Receiver

1.4 SPECIFICATIONS

NOTE: All receiver input voltages given are open circuit generator or antenna voltages

Frequency Range:	10 kHz to 29.9999 MHz
Tuning Increments:	100 Hz with continuous tuning between increments
Tuning Accuracy:	±50 Hz
Input Impedance:	50 ohms, except high impedance when preselector used 160 kHz to 525 kHz or 1605 kHz to 4000 kHz
Absolute Maximum Input:	30V rms

Sensitivity:

Frequency	Mode	BW	SND/ND	INPUT
.10 MHz - .16 MHz	A1	Narrow	10 dB	30 dBuV
.16 MHz - .53 MHz	A1	Narrow	10 dB	20 dBuV
	A2H/ A3H	Intermediate	10 dB	30 dBuV
.53 MHz - 1.6 MHz	A2H/ A3H	Intermediate	10 dB	30 dBuV
1.6 MHz - 4.0 MHz	A2H/ A3H	Wide	20 dB	30 dBuV
	A3A/ A3J	Intermediate	20 dB	16 dBuV
4.0 MHz - 30 MHz	A1	Narrow	10 dB	0 dBuV
	A2H/ A3H	Wide	20 dB	24 dBuV
	A3A/ A3J	Intermediate	20 dB	11 dBuV

Image Rejection:	50 dB minimum
IF Rejection:	60 dB minimum
Spurious Rejection:	60 dB minimum
Blocking Level:	100 dBuV minimum
Crossmodulation Level:	90 dBuV minimum

	Type	6 dB BW Min.	60 dB BW Max.
IF Bandwidth:	Wide	5.4 kHz	20 kHz
	Intermediate (SSB)	2.4 kHz	4.3 kHz
	Narrow	1 kHz	7 kHz
	Very Narrow	0.3 kHz	4 kHz

AF Bandwidth (6dB): .35 kHz - 2.7 kHz

LO Leakage: 1 nW maximum

IF Output: 1.4 MHz, 50 ohms

AGC Range: A 70 dB increase in signal strength above the specified sensitivity results in a maximum 10 dB increase in audio output.

BFO Range: ±1.5 kHz

Audio Output: Speaker--1.5 W @ 4 ohms at 10% distortion

Line-- +10 dBm @ 600 ohms at 10% distortion

Power Requirements: 110V/220V ±10%, 47 Hz - 63 Hz, 50 W

24 VDC -10%, +30%, 50 W

Operating Temperature Range: 0°C to +50°C

Dimensions: 133mm h x 483mm w x 349mm d

Weight: 13.6 kg

1.5 OPTIONAL EQUIPMENT

An rf noise generator is available which, when activated by depressing the preselector control, allows peaking of the preselector in the absence of atmospheric noise.

A remote interface board is available to allow connection of a suitable remote control unit to the receiver. Remote control of the receiver is possible from distances up to 30 meters.

1.6 SYMBOLS AND ABBREVIATIONS

Design conventions used: ANSI-Y14.5

Logic symbols: ANSI Y32.5

SECTION 2
INSTALLATION

2.1 UNPACKING

Carefully remove the receiver from the shipping carton and examine it for evidence of damage. If any damage is discovered, immediately notify the transportation company that delivered the receiver. Be sure to keep the shipping carton and packing material, as the transportation company will want to examine them if there is a damage claim. Also, having the original carton available makes packing the receiver much easier should it ever be necessary to store it or return it to the factory for service.

2.2 POWER REQUIREMENTS

CAUTION

DO NOT PLUG THE RECEIVER INTO ANY VOLTAGE OUTLET WITHOUT CHECKING THE REAR OF THE CHASSIS FOR THE CORRECT INPUT VOLTAGE.

The receiver is shipped from the factory wired for 220 VAC 50/60 Hz and 24 VDC operation, unless specified otherwise. To operate on 110 VAC, make the wiring change at the power relay board, as illustrated in figures A-23, 5-1, and 5-17. That is, on the power relay board:

a. Install W1.
b. Install W2.
c. Remove W3.

If the above change has been made for 110-volt operation and it is intended to operate the receiver on DC reserve power, R1 on the power relay board must be adjusted for the correct switch over point to DC operation. This is accomplished in the following manner.

WARNING

HAZARDOUS VOLTAGES ARE PRESENT IN THE POWER SUPPLY SECTION.

a. Connect a suitable +24 VDC supply to the receiver.
b. Connect the receiver to the 110 VAC lines by means of a variac.
c. Adjust the variac to set the AC input voltage to 94 VAC.
d. Turn R1 slowly counterclockwise until the receiver switches to DC operation. This is indicated by the front panel BATT OPER indicator.
e. Check the adjustment by raising the AC input voltage and observe that the receiver switches back to AC operation.
f. This completes the adjustment.

Wire the power connectors as shown in figure 2-1. Refer to the rear view of the receiver in figure 2-2 when making external connections to the receiver.

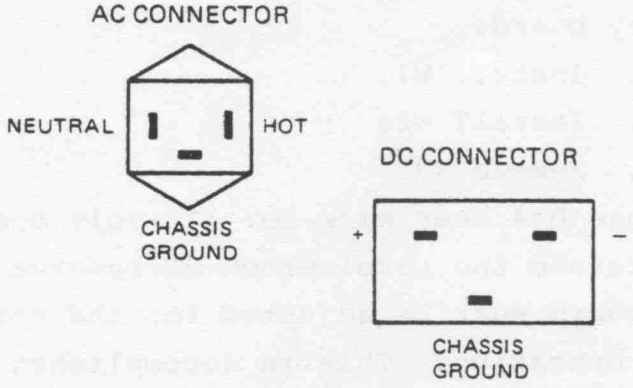

Figure 2-1. Power Connector Wiring

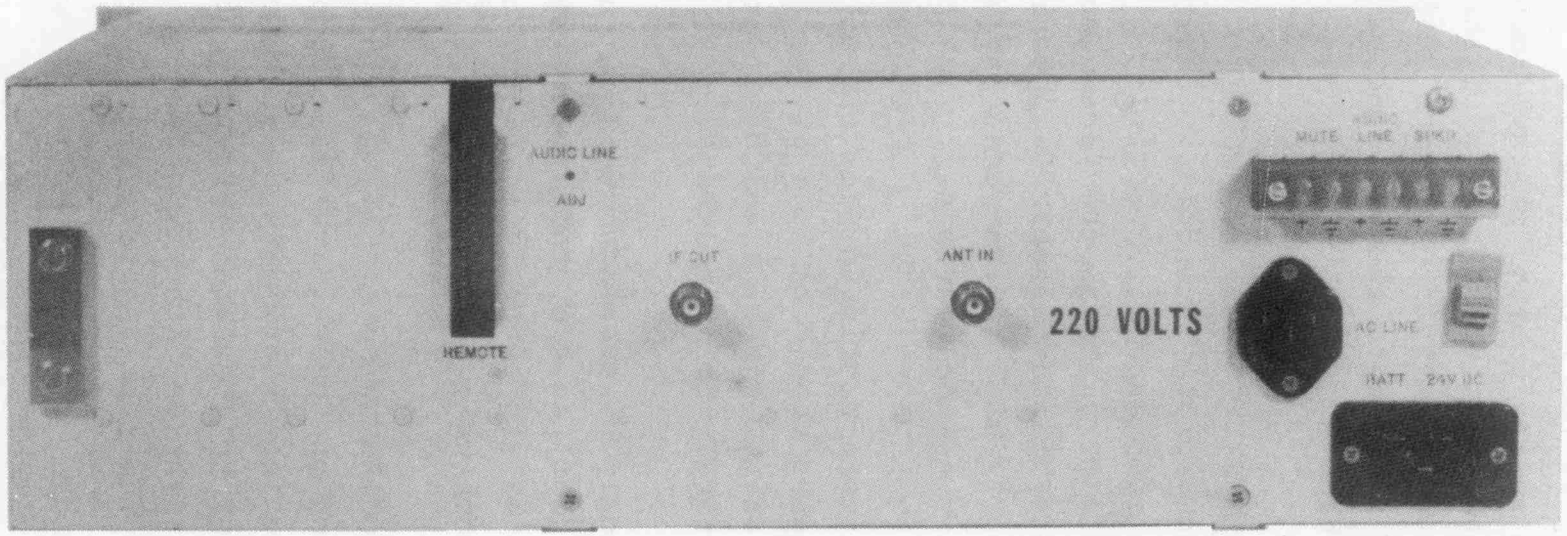

Figure 2-2 2000 Receiver, Rear View

2.3 MOUNTING THE RECEIVER

Mount the receiver in a standard 483mm rack. Space requirements are 133mm of panel height and 349mm of depth. Do not attempt to support the receiver only by the front panel. Provide braces in the cabinet or rack to support the rear of the unit. In general, the location of the receiver is not critical, however, provision should be made for a reasonable circulation of air around the unit and extremely hot locations should be avoided.

2.4 ANTENNA REQUIREMENTS

The receiver is capable of excellent performance with either 50-ohm or high impedance antennas below 4 MHz and 50-ohm antennas above 4 MHz. Bring the receiving antenna in by a length of coaxial cable, as short as possible, especially in the case of short (high impedance)antennas, and connect to the ANT IN connector on the rear panel.

To minimize interference in duplex operation, transmitting and receiving antennas should be kept as far away from each other as possible. Stays, wires, steel masts etc. should be either grounded effectively or insulated.

The antenna should be suspended well in the clear, away from objects whose influence on the antenna may vary, such as cranes etc. Insulators should be of the best type having low leakage even when wet.

2.5 GROUND REQUIREMENTS

The ground clamp on the receiver is located at the back of the receiver at the left rear. Use a length of braid to connect the ground clamp to a separate ground screw. Do not share this ground lead connection with any other equipment. Run the ground lead as far from any transmitter ground leads as is practicable.

Other cables should be run as far away from the receiver ground lead as possible and under no circumstances parallel with it, closer than 0.2m.

2.6 IF OUTPUT

The IF output is available at the IF OUT connector on the rear panel. The output frequency is 1.4 MHz and the output impedance is 50 ohms. The IF output signal level is 15 dB greater than that at the receiver input.

2.7 EXTERNAL SPEAKER

The receiver has a built-in 4-ohm speaker. However, SPKR terminals on the rear of the unit provide for connecting an external speaker rated at 4-ohm/2 W or 8-ohms/2 W. The external speaker terminals are connected in parallel with the built-in speaker; therefore the built-in speaker must be switched off if full audio power at the external speaker is utilized. One of the speaker terminals is connected to chassis ground.

2.8 AUDIO LINE

The audio line output is available from AUDIO LINE terminals on the rear panel barrier terminal strip. One terminal is connected to chassis ground. The output will drive a 600-ohm load and is adjustable from no output to +10 dBm. A small hole on the rear panel, marked AUDIO LINE ADJ, gives access to the potentiometer.

2.9 MUTING

The receiver audio outputs may be muted by connecting together the two rear panel terminals labeled MUTE. One terminal is connected to ground. The open circuit voltage at these terminals is +12 V, while the closed circuit current is 2.5 mA.

2.10 REMOTE OPERATION

The receiver is capable of remote operation via a suitable remote control unit and an optional remote interface board which plugs into the receiver chassis. The remote control cable is attached to a connector on the Remote Interface Board, which is accessible at the rear panel chassis cut out labeled REMOTE.

SECTION 3

OPERATION

3.1 INTRODUCTION

Instructions for operating the receiver are provided in three phases. The front panel controls and indicators are identified in figure 3-1 and their functions are briefly stated in a tabular listing. Procedures for operating the receiver via the keyboard are furnished with a brief description of receiver action during keyboard operation. Lastly, a summary of operating techniques is furnished.

3.2 CONTROLS AND INDICATORS

Refer to figure 3-1 and table 3-1.

Figure 3-1 2000 Receiver Controls and Indicators

Table 3-1. Controls and Indicators

Name	Function
BATT	Fuse for the 24 VDC input line.
MAIN	Fuse for the 110/220 VAC input line
BATT OPER	Lamp indicator illuminates when the receiver is operating from 24 VDC input.
PHONES	Phone jack for connection of either low or high impedance headphones fitted with a standard 6mm phone plug. Insertion of the phone plug automatically disconnects the local (but not the remote) speaker.
SPEAKER OFF	Switch disables the local (but not the remote) speaker.
0 through 9	Pushbuttons used to specify receiver frequencies or receiver memory locations.
500	Depressing this pushbutton causes the receiver to immediately tune to 500 kHz.
2182	Depressing this pushbutton causes the receiver to immediately tune to 2182 kHz.
RCL	Pushbutton initiates the recall of a frequency from memory.
FREQ	Pushbutton initiates the setting of a new receiver tuned frequency.
SCAN	Pushbutton starts and stops receiver scanning.
STO	Pushbutton initiates the storing of a frequency in memory.
CLR	Pushbutton returns the receiver to the previous tuned frequency or eliminates an error.
PRES	Pushbutton enables or disables the pre-selector. Preselector may be used to match impedance of electrically short antennas or to reject strong interfering signals. Preselector may be used over the following frequency ranges: 160.0 kHz - 525.0 kHz 1605.0 kHz - 29999.9 kHz

Table 3-1. Controls and Indicators (continued)

Name	Functions
	Preselector is automatically disabled when a new receiver tuned frequency is entered via the keyboard, either directly or from memory.
SC/ON	Pushbutton turns on or off the SC/ON indicator.
REM	When depressed, REM pushbutton disables all receiver local controls and enables control from a remote unit. Control is effective only when a remote unit is connected.
FREQUENCY kHz	This 6-digit display indicates the receiver tuned frequency or receiver memory location and also contains the following indicators:
	FCN — When illuminated, indicator shows that a keyboard data entry is in process.
	SCAN — When illuminated, indicator shows that the receiver is in the SCAN mode.
	SC/ON — When illuminated, indicator shows that a related memory location will be scanned.
	ERROR — When illuminated, indicator shows that an operator error has been made in receiver operation.
S-METER	Meter gives a relative indication of received signal strength when the receiver AGC is on.
BW	Four illuminated pushbuttons select the receiver IF bandwidths, as follows:
	VN (Very Narrow) — Selects the 0.3 kHz bandwidth.
	N (Narrow) — Selects the 1.0 kHz bandwidth.

Table 3-1. Controls and Indicators (continued)

Name		Function
	I (Intermediate)	Selects the 2.4 kHz, USB or optional telex bandwidth, as follows: If mode A1 or A2H is selected, I pushbutton selects the 2.4 kHz bandwidth. If mode A3J is selected, I pushbutton selects the USB bandwidth. If mode F1 is selected, and the optional telex filter has been installed, I pushbutton selects the telex bandwidth, otherwise the 2.4 kHz bandwidth will still be selected.
	W (Wide)	Selects the 5.4 kHz bandwidth.
MODE		These illuminated pushbuttons select the receiver demodulation mode.
	A1	Selects CW demodulation in conjunction with the BFO.
	A2H/A3H	Selects AM demodulation.
	A3A/A3J	Selects USB demodulation in conjunction with the CLARIFIER.
	F1	Selects FSK demodulation.
DIMMER		Variable control for illumination of the display, all front panel indicators (except BATT OPER), and the S-METER.
VOLUME-OFF		Turns the receiver off and on and varies the audio level to the speaker and headphones.
SENSITIVITY		Varies the maximum IF gain of the receiver, whether the AGC is on or off. Pulling the control outward disables the AGC.
CLARIFIER/BFO		In the A2H, A3J, and F1 modes, fine tunes the receiver over an approximately ±150 Hz range. However, this frequency change will not be shown on the display. In the A1

Table 3-1. Controls and Indicators (continued)

Name	Function
	mode, varies the frequency of the BFO over an approximately ±1.5 kHz range.
PRESELECTOR	This control tunes the preselector. The lamp indicator above the control lights when the preselector has been enabled. If the optional RF noise generator has been installed, the generator provides a test signal for tuning the preselector in the absence of a received signal. Pushing the preselector control inward actuates the RF noise generator.
TUNE	This control tunes the received frequency. The control is spring-loaded, so that it is self-centering. Turning the control CW from center causes the receiver frequency to increase; turning the control CCW from center causes the receiver frequency to decrease. The farther the control is rotated away from center, the faster will be the rate of frequency increase or decrease. The basic unit of increase or decrease is 0.1 kHz unless mode A2H and the wide bandwidth are selected, in which case the basic unit of increase or decrease is 1.0 kHz. The minimum rate of increase is approximately 1 increment per second, while the maximum rate is approximately 60 imcrements per second.
SCAN DWELL TIME ADJUSTMENT	A small hole to the right of the F1 mode pushbutton provides access to this screwdriver adjustment. It is used for setting the amount of time the receiver remains on a given channel in the scan function. Dwell times range from approximately 0.5 seconds to approximately 15 seconds.

3.3 AUTOMATIC OPERATION

3.3.1 Automatic RF Bandswitching

All RF bandswitching is fully automatic, based on the tuned frequency. The receiver will operate in one of three wideband RF bands unless the selected frequency corresponds to a frequency in one of the six standard marine coast station duplex transmit bands. In this case a narrow band filter is selected to provide rejection of the ship's transmitter in duplex operation. The RF bandswitching is automatically performed regardless of whether frequency selection is made via the keyboard or the tuning control.

3.3.2 Automatic IF Bandwidth Selection

IF bandwidth selection is automatically made as a function of the reception mode as follows:

Selected Mode	Automatic IF Bandwidth Selection
A1	N
A2H/A3H	W
A3A/A3J	I (USB)
F1	I (or telex filter, if installed)

The automatic selection is made only at the instant a new mode is selected as a result of a new frequency entry via the keyboard (either directly, or as a recall from memory, or during scanning).

This automatic selection may be overridden at any time by the operator however, by merely depressing the pushbutton corresponding to the desired bandwidth.

3.3.3 Automatic Mode Selection

Mode selection is automatically made as a function of tuned frequency. The selection corresponds to the internationally-agreed-upon modes to be used within the maritime bands. Outside the maritime bands, the mode A2H/A3H will always be selected. The automatic selection will only be made as a

result of a frequency entry via the keyboard (either directly, or via memory recall, or during scanning). Selection will not be made while the frequency is being altered via the tuning control. Additionally, the automatic selection may be overridden at any time by the operator by depressing the pushbutton corresponding to the desired mode.

3.4 KEYBOARD OPERATION

3.4.1 Power On

At turn on, the receiver will automatically select the frequency to which it was last tuned, as follows:

Key	Display	BW	Mode	Audio
Turn Power ON	4188.5	N	A1	4188.5, N, A1

The previous frequency has been selected, together with its mode and bandwidth.

3.4.2 Selecting a New Receiver Frequency

To select a new frequency, press the indicated keys.

Key		Display	BW	Mode	Audio
		4188.5	N	A1	4188.5, N, A1
Press: 4	FCN	.4	--	--	4188.5, N, A1
5	FCN	4.5	--	--	4188.5, N, A1
4	FCN	45.4	--	--	4188.5, N, A1
0	FCN	454.0	--	--	4188.5, N, A1
Press FREQ		454.0	W	A2H/A3H	454.0, W, A2H/A3H

The new frequency has been selected, together with its mode and bandwidth.

3.4.3 Storing Frequencies In Memory

Thirty locations (1 to 30) are available for frequency storage. The current frequency to which the receiver is tuned may be stored in these memory locations, together with the selected mode and bandwidth. Storage of the current frequency is accomplished by entering the memory location, and depressing the STO key.

Key	Display	BW	Mode	Audio
	454.0	W	A2H/A3H	454.0, W, A2H/A3H
Press 1.	FCN .1	--	--	454.0, W, A2H/A3H
9	FCN 1.9	--	--	454.0, W, A2H/A3H
STO	454.0	W	A2H/A3H	454.0, W, A2H/A3H

Frequency 454.0, A2H, W has been stored in memory location 19.

It is not necessary to erase a memory location prior to entering a new frequency since this occurs automatically when new information is stored.

3.4.4 Recalling a Stored Frequency

A stored frequency is recalled in the following sequence.

Key	Display	BW	Mode	Audio
	454.0	W	A2H/A3H	454.0, W, A2H/A3H
Press 2	FCN .2	--	--	454.0, W, A2H/A3H
0	FCN 2.0	--	--	454.0, W, A2H/A3H
RCL	1625.0	I	A3A/A3J	1625.0, I,A3A/A3J
	SC/ON			

The stored frequency has been recalled, together with its mode and bandwidth. Note that the SC/ON indicator is on, showing that location 20 was previously designated to be scanned in the scan mode.

After an initial recall of a memory location, subsequent depressions of RCL will cause following locations to be recalled without entering any further location numbers. When Location 30 has been reached, the next depression of RCL recalls Location 1 and the process continues. The number of the memory location being recalled will automatically be momentarily displayed prior to the display of the recalled frequency.

Following turn on, or any other function, depression of RCL will cause this sequence to begin, automatically starting at Location 1..

Assuming Location 20 was previously recalled, the sequence is as follows:

Key	Display	BW	Mode	Audio
	1625.0	I	A3A/A3J	1625.0, I,A3A/A3J
Press RCL	2.1/4405.0 SC/ON	I	A3A/A3J	4405.0, I,A3A/A3J
RCL	2.2/6515.5 SC/ON	I	A3A/A3J	6515.5, I,A3A/A3J
RCL	2.3/8766.8 etc.	I	A3A/A3J	8766.8, I,A3A/A3J

Note that two of the locations have previously been designated to be scanned.

3.4.5 Selection Of Distress Frequencies

Selection of either of the two distress frequencies, 500 kHz or 2182 kHz, is accomplished merely by pressing the corresponding pushbuttons as shown on next page.

Key	Display	BW	Mode	Audio
	1625.0	I	A3A/A3J	1625.0, I, A3A/A3J
Press 500	500.0	W	A2H/A3H	500.0, W, A2H/A3H
Press 2182	2182.0	W	A2H/A3H	2182.0, W, A2H/A3H

The frequency to which the receiver was tuned prior to the distress frequencies may be recalled via the CLR key.

3.4.6 Scanning

The receiver is capable of scanning any or all of the frequencies stored in memory. While scanning, the receiver will tune to the first designated stored frequency, selecting the correct mode and bandwidth, remain tuned to the frequency for an amount of time determined by the SCAN DWELL TIME control, and then tune to the next designated stored frequency. Frequencies are always selected in numerically increasing order of memory location beginning with the lowest specified location, but the actual frequencies themselves need not be in any particular order. When tuning to a given frequency, the display momentarily indicates the memory location number and then the frequency to which it is tuned.

Frequencies to be scanned must be stored in memory via the standard procedure. The memory location may be designated to be scanned by two possible means.

1. While storing a frequency, turn on the SC/ON indicator, using the SC/ON key at any time prior to depressing STO, i.e., either before entry of memory location number or afterward. If it is desired that the location not be scanned, the SC/ON indicator should be extinguished at any time prior to depressing STO.

2. During a RCL, RCL, RCL sequence, altering the state of the SC/ON indicator between depressions of RCL will, on the subsequent depression of RCL, cause the scan status of the previously recalled location to be altered in the same fashion. For example:

	Key	Display	BW	Mode	Audio
Press	2	FCN .2	--	--	8766.8, I, A3A/A3J
	0	FCN 2.0	--	--	8766.8, I, A3A/A3J
	RCL	1625.0	I	A3A/A3J	1625.0, I, A3A/A3J
		SC/ON			
	SC/ON	1625.0	I	A3A/A3J	1625.0, I, A3A/A3J
	RCL	2.1/4405.0	I	A3A/A3J	4405.0, I, A3A/A3J
		SC/ON			
	SC/ON	4405.0	I	A3A/A3J	4405.0, I, A3A/A3J
	RCL	2.2/6515.5	I	A3A/A3J	6515.5, I, A3A/A3J
	SC/ON	6515.5	I	A3A/A3J	6515.5, I, A3A/A3J
		SC/ON			
	RCL	2.3/8766.8	I	A3A/A3J	8766.8, I, A3A/A3J

Memory Locations 20 and 21 will thus no longer be scanned, but Location 22 will be scanned.

Once memory locations have been designated for scanning, scanning may be started by depressing the SCAN pushbutton. The dwell time may be adjusted as required. The receiver can be stopped on a given frequency be pressing the SCAN pushbutton a second time. Where the selected dwell time is long, the receiver may be rapidly advanced to the next scanned frequency by pressing the SCAN pushbutton rapidly two times.

3.4.7 Error Conditions

The following operations will cause an error indication. Eliminate the errors by pressing the CLR key.

a. Attempted entry of a frequency less than 10.0 kHz or greater than 29999.9 kHz.

b. Attempted use of the N or VN bandwidth in the F1 mode.

c. Attempted entry of a memory location less than 1 (for store) or greater than 30 (for recall or store).

d. Attempted selection of the preselector at frequencies less than 160.0 kHz or between 525.1 kHz and 1605.0 kHz.

3.5 SUMMARY OF OPERATING TECHNIQUES

3.5.1 A1 (CW) Operation

The excellent selectivity characteristics of the receiver can be more fully utilized in A1 operation than in A2H or A3J (voice) operation where the bandwidths are relatively wide. For CW operation, when the desired station frequency is known, the frequency is entered in the keyboard and the A1 mode and N bandwidth selected.

With the CLARIFIER/BFO control set to the center position, the frequency display indicates the frequency of the received carrier when the audio output is zero beat. In A1 reception, the CLARIFIER/BFO control is adjusted for the desired audio pitch by the operator. The VN, N, I, or W filters may be used.

When the frequency is unknown, the band may be scanned by the TUNE Control with the W (wide) bandwidth. When a station is found, the N or VN bandwidth may be selected. From 160.0 kHz to 525.0 kHz or 1605 kHz to 4000 kHz, the preselector may be used for optimum sensitivity, or it may be used at any frequency to reject strong interfering signals.

For A1 reception, the AGC may be left on or off and the SENSITIVITY control used together with the VOLUME control to set a suitable audio level.

3.5.2 A2H/A3H (MCW or AM) Operation

The frequency of the desired station is generally known and can be entered via the keyboard. For A2H/A3H reception, the A2H/A3H mode and wide (W) bandwidth should be selected and the CLARIFIER control set to the center position. In this condition, the frequency indicated by the frequency display on the front panel is that of the station being received.

When a station frequency is not known, the band can be scanned by the TUNE control with the W (wide) bandwidth selected. When a station is found and peaked on the S-meter, it may be possible to utilize a narrower bandwidth.

The AGC is usually left on, with the SENSITIVITY control set to maximum and the VOLUME control adjusted for a suitable audio level.

3.5.3 A3A/A3J (USB) Operation

The frequency of the desired station is generally known and can be entered via the keyboard. For A3A/A3J reception, the A3J mode and intermediate (I) bandwidth should be selected and the CLARIFIER set to the center position. In this condition, the frequency indicated by the frequency display on the front panel is that (of the suppressed carrier) of the station being received.

When a station frequency is not known, the band can be scanned by the TUNE control with the wide (W) bandwidth selected. When a station is found, and peaked on the S-meter, the receiver can be returned to the normal A3A/A3J operating condition by depressing the I pushbutton. The TUNE and CLARIFIER may then be adjusted for optimum intelligibility.

The preselector is normally not used. However, the preselector may be used from 1605 kHz to 4000 kHz for optimum sensitivity or at any frequency where rejection of an interfering signal is

required. In general, the preselector will also give improved sensitivity within the duplex bands although rejection of the ship's transmitter will not be as great as that obtained with the internal automatic duplex filters.

The SENSITIVITY control may be turned counter clockwise somewhat for strong stations to keep the receiver noise from increasing between voice syllables and the AGC left on. The VOLUME control should be adjusted for a suitable audio level.

3.5.4 F1 (FSK) Operation

The frequency of the desired station is generally known and can be entered via the keyboard. For F1 reception, the F1 mode and the intermediate (I) bandwidth should be selected and the CLARIFIER set to the center position. In this condition, the frequency indicated by the display on the front panel is that of the station being received.

When a station frequency is not known, the band can be scanned by the TUNE control with the W (wide) bandwidth selected. When a station is found and peaked on the S-meter, the receiver can be returned to the normal F1 operating condition by depressing the intermediate (I) pushbutton. The normal audio output frequency is 1.7 kHz and the CLARIFIER may be adjusted to correct for small tuning errors and exactly achieve this frequency.

The preselector may be used from 160.0 kHz to 525.0 kHz or 1605.0 kHz to 4000 kHz for optimum sensitivity or it may be used at any valid frequency to reject strong interfering signals.

The AGC should be left on and VOLUME control set for a suitable audio level. The input to a telex demodulator may be taken from the rear panel AUDIO LINE terminals and the level set by the AUDIO LINE ADJ control on the rear panel.

SECTION 4
PRINCIPLES OF OPERATION

4.1 INTRODUCTION

For presentation in this section, the receiver circuits are divided into five major sections: RF/IF, synthesizer, microprocessor, display, and the power supply. Each section is briefly described in conjunction with a block diagram, followed by a more detailed description with reference to the logic diagram.

Logic diagrams for each circuit board are located in the Appendix to this manual. Each logic diagram, some consisting of several sheets, represents a complete printed circuit board. Logic symbols of integrated circuit modules are identified by a reference designator (U). Circuits within a module are referenced by an alpha character following the designator number (U1A, U1B, etc.). Also, the manufacturer's part number is included below the logic symbol or within the logic symbol.

4.2 RF/IF SECTION

4.2.1 Block Diagram Discussion (See figure 4-1.)

The input from the antenna is applied via a bandstop filter either to bandpass filters used to reject transmitter emissions in duplex operation, three wide band filters used to limit the bandwidth of the received frequency spectrum in non-duplex operation, or five tunable preselector filters used to reject strong interfering signals or to match the receiver to the antenna. A serial to parallel shift register recognizes data from the microprocessor and latches are activated to select one of the above filters via diode switches. A low pass filter and first conversion mixer, followed by an IF preamplifier, produce the 38 MHz IF signal.

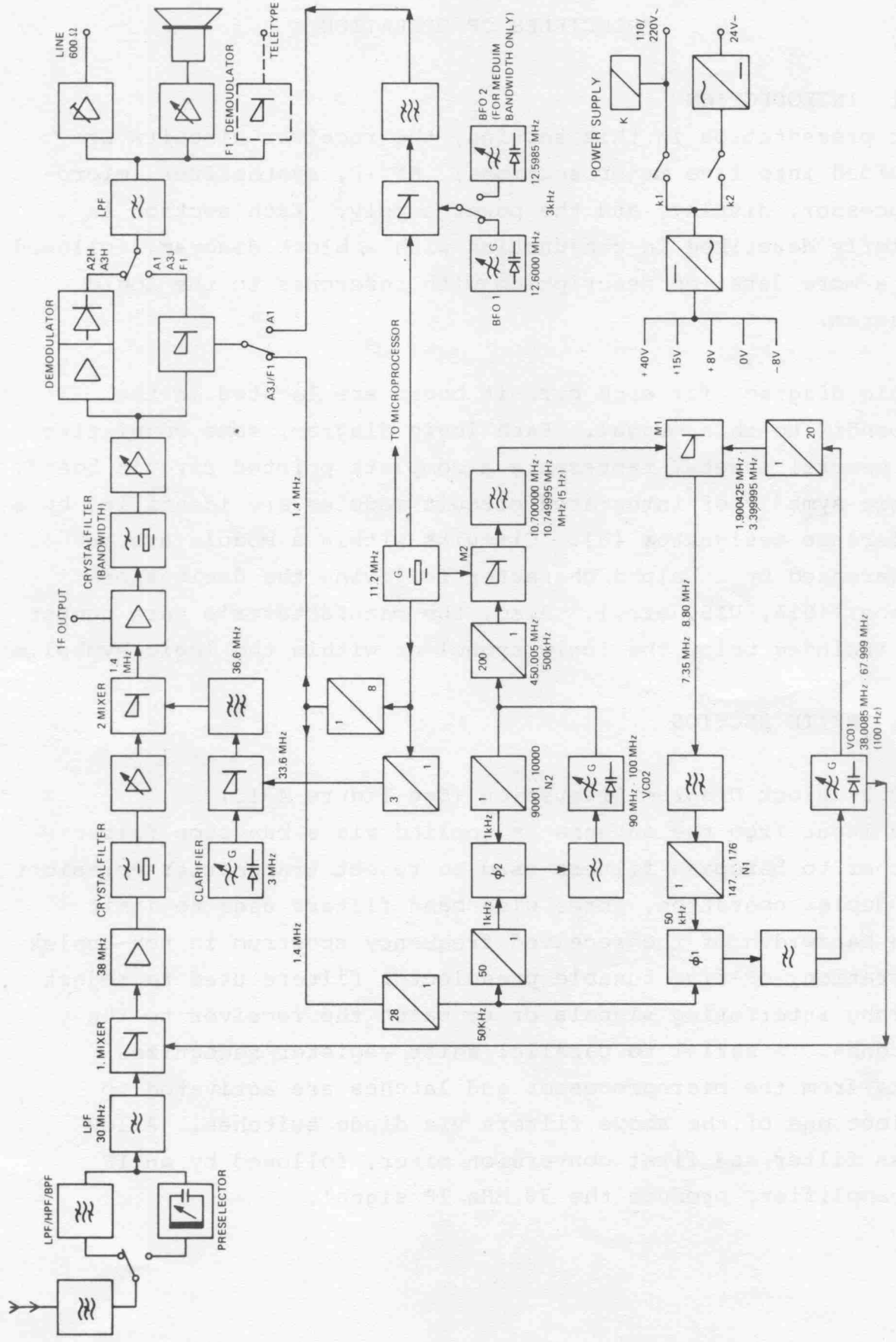

Figure 4-1 Model 2000 Receiver, Block Diagram

The 38 MHz IF signal is passed through a crystal bandpass filter, pin diode attenuator, and an amplifier to the second conversion mixer. A 3 MHz VCXO serves as a clarifier. This frequency is mixed in a balanced mixer with a 33.6 MHz signal from the synthesizer, passed through a bandpass filter and amplifier, and is applied to the mixer as the second LO. The output of the mixer is the 1.4 MHz IF signal.

The 1.4 MHz IF signal is applied to an amplifier, one output of which is connected to the IF OUT connector at the rear panel of the receiver. The other amplifier output is applied to one of five crystal filters which are selected by a binary to decimal decoder, in response to signals from the microprocessor calling for a specific filter.

The 1.4 MHz IF signal from the filter is amplified in a variable gain amplifier and applied to a product detector and envelope detector. Serial to parallel conversion of information from the microprocessor is used to select the appropriate detector. The selected audio output is applied to an active low pass filter and then to the line amplifier, or, through the VOLUME control, to the speaker amplifier.

4.2.2 RF Filter Board

Refer to the logic diagram, figure A-2. Limited RF signals are applied to one of nine filters via P2-B. Two lowpass filters and one highpass filter are used for wideband operation. Six bandpass filters are used for duplex operation. The filters are individually selected by diodes CR1 through CR18.

Serial data from the microprocessor board is applied to shift and store register U4 at P1-D. From U4, the serial synthesizer data is available for the synthesizer board at P1-F. Also, four stored parallel outputs of U4 are applied to 4-to-16 decoder U1. U1 generates a positive output to turn on a given pair of diodes via inverting darlington array U5 or U2. Current

to turn on the diodes flows through R11/L13 and R1/L1, while all other diodes are reverse biased via pull-up resistors in U3 and U6. Filtered RF signals from the RF filter board are taken from P2-K.

Two outputs of U4 supply bandswitch information for the synthesizer board via P1-7 and P1-8.

4.2.3 Preselector Board

Refer to the logic diagram, figure A-3. The antenna input is applied to P2-K. If a preselector is not used, or for all preselectors except 160 kHz to 290 kHz and 290 kHz to 525 kHz, the signal is first applied via K3 to the input power limiter composed of diodes CR18 through CR29 and FET Q1. At high input levels, the voltage multiplier CR18 through CR29 develops sufficient voltage on the gate of Q1 to cause it to begin to conduct and shunt the input.

From the power limiter, the signal is either applied to the wide band and duplex filters via P2-H or applied to one of the three MF/HF preselectors. These three voltage controlled filters are tuned via varicap arrays VVC1 through VVC3 and VVC6 through VVC12 and switched via diodes CR1 through CR3 and CR10 through CR12. The current to turn on the diodes is obtained from the RF filter board.

If a preselector is selected with frequency range 160 kHz to 290 kHz or 290 kHz to 525 kHz, relay K3 routes the signal to the input power limiter composed of diodes CR13 and CR14. The output of this limiter is then applied to relay K1, which in turn sends the signal to one of the two preselectors composed of T4 and T5. These filters are also voltage controlled and tuned by varicap array VVC4 and VVC5. The filter outputs are switched via diodes CR4 and CR5.

Quad bilateral switch U2 selects either local or remote preselector controls. The output of U2 is applied to the

inverting-tuning voltage driver composed of Q2 and operational amplifier U1, which supplies tuning voltage to all preselectors.

The output of the desired preselector or the desired wideband or duplex filter (from P2-B) is routed thru a 30 MHz lowpass filter to the first mixer module A1. The output of the mixer module is then available as the 38 MHz signal to the 38 MHz IF board.

4.2.4 First Mixer Board.

Refer to the schematic diagram, figure A-4. The 10 kHz to 30 MHz RF input to the first mixer is applied through a VHF lowpass filter to the double balanced mixer A1. The 38-68 MHz local oscillator input to the mixer is applied through a second VHF lowpass filter. The mixer output at 38 MHz is routed to low noise amplifier Q1 and then outputted.

4.2.5 38 MHz IF Board

Refer to the logic diagram, figure A-5. The 38 MHz input is first applied to 38 MHz crystal filter FL1. The output of the filter is applied to a PIN diode attenuator composed of CR1 and CR2, then to the grounded gate amplifier Q1. The output of Q1 is one input to the double balanced mixer A1.

LO drive for mixer A1 is obtained as follows: 33.6 MHz input frequency at P1-K is one input to balanced modulator U1, which is used as a mixer. The other input to U1 is obtained from the 3 MHz voltage controlled oscillator (clarifier) composed of Q3, Q5, and Q6.

The output of U1 at 36.6 MHz is passed through a bandpass filter and then amplifier Q2, before being applied to A1. Thus, the second LO is varied slightly in frequency by means of the clarifier oscillator.

Quad bilateral switch U2 selects either remote or local control of the clarifier (or BFO via P1-5) and also disables the clarifier tuning when the BFO is desired.

4.2.6 1.4 MHz IF Filter Board

Refer to the logic diagram, figure A-6. The 1.4 MHz input at P2-7 is applied to a cascode amplifier composed of Q2 and Q1. The output of Q1 drives the selected IF filter, which is switched by diodes CR1 through CR12.

BCD-to-decimal decoder U3 accepts binary coded information as to the filter to be selected and drives inverting darlington driver U2 with the decoded information. U2 causes current to flow through the appropriate diodes to select the correct IF filter. U2 also generates an output via CR14 to control the BFO.

The output of the selected filter is sent from the board via P2-3 to the 1.4 MHz IF/DEMOD board. For external use, transformer T2 couples the 1.4 MHz IF signal to the IF output jack on the receiver rear panel.

4.2.7 1.4 MHz IF/Demodulator Board

Refer to the logic diagram, figure A-7. The input frequency at 1.4 MHz is applied to U16, a gain controllable If amplifier. The output of U16 is applied to U4, a wide band amplifier, limiter, detector, audio amplifier, utilized as a product detector. The other input to the product detector is the 1.4 MHz local carrier signal via P2-8.

A buffered IF output from U4 is applied to the AM/AGC detector composed of Q2 and CR3. The product detector audio output and the AM detector output are applied to quad bilateral switch U9, which selects which input is applied to active low pass filter U8D. U9 also mutes the audio output when desired.

The output of U8D is applied to line amplifier U10 and, via the

receiver volume control, to speaker amplifier U17. The AM detector output at CR3 is also applied to amplifier U8C and then quad bilateral switch U3. U3, together with U5 and U2A through U2C, selects between local and remote control of AGC/MGC functions.

The output of U3 is applied via a time constant network to amplifier U8B, the output of which serves as the 38 MHz AGC output at P1-13 and also is applied to the gain control input of U16 via U8A.

Quad differential line receiver U12 accepts serial differential signals from the microprocessor and supplies single-ended versions of these signals to U13 and to other receiver circuits.

Shift and store register U13 accepts serial information from U12 and outputs parallel demodulation mode information, BCD IF bandwidth information, and scan mode identification. Demodulation mode information is used to control U9 while IF bandwidth information is outputted to the 1.4 MHz IF filters.

Scan mode information is applied to dual monostable multivibrator U7A which, together with U7B and U2D through U2F, mute the receiver and reset the AGC during scan frequency changes.

Normal muting is effected by Q1, which in turn opens switch U9 and also reduces the gain of U16 via CR6.

Single ended serial data to the RF filters is outputted from J13 via P1-T.

4.2.8 Remote Interface Board

Refer to the logic diagram, figure A-8. The optional remote interface board provides connections between a remote unit and the receiver. All receiver control lines, both digital and analog, are applied to board-mounted connector J1, are filtered as required, and are applied to P1.

4.3 FREQUENCY SYNTHESIZER

4.3.1 Block Diagram Discussion (See figure 4-1.)

The frequency synthesizer is made up of four circuit boards--the reference board, the programmable divider board,the divide by 20 board, and the VCO board. The purpose of the frequency synthesizer is to generate all local oscillator, carrier, and reference frequencies required by the receiver.

Circuitwise, the frequency synthesizer consists of two programmable phase lock loops. VCO2, divide-by-N2 and phase detector 2 on the programmable divider board form phase lock loop 2, which operates from 90.001 MHz to 100,000 MHz in 9,999 one-kilohertz steps. VCO2 is divided by 200 on the reference board, mixed with the 11.2 MHz reference on the VCO board (M2), and filtered to produce a frequency from 10.700000 MHz to 10.749995 MHz in 9,999 five-Hertz steps. This frequency is injected into the frequency summing loop consisting of VCO1 (on the VCO board), divide-by-20 (on the divide by 20 board),(M1), the 7.35 MHz to 8.8 MHz bandpass filter (both on the VCO board), divide-by-N1, and phase detector 1 (both on the programmable divider board). VCO1 operates from 38.0085 MHz to 67.9999 MHz in 100-Hertz steps. The output of VCO1 serves as a variable LO injection frequency feeding the first mixer stage of the receiver.

Assuming both loops are locked, the following equations describe the operation of the synthesizer.

N1	=	Quantity by which N1 divides
N2	=	quantity by which N2 divides
FVCO1	=	frequency of VCO1
FVCO2	=	frequency of VCO2
M2 OUT	=	output frequency of mixer U1 on the VCO board
FVCO2	=	N2(1000)
M2 OUT	=	$11.2 \times 10^6 - \frac{FVCO2}{200}$

$$M2\ OUT = 11.2 \times 10^6 - \frac{N2(1000)}{200}$$

$$\frac{VCO1}{20} = M2 - N1(50{,}000)$$

$$\frac{VCO1}{20} = 11.2 \times 10^6 - \frac{N2(1000)}{200} - N1(50{,}000)$$

$$VCO1 = 224 \times 10^6 - 100N2 - 1 \times 10^6 N1$$

Thus decrementing N1 by 1, increases FVCO1 by 1 MHz while decrementing N2 by 1 increases FVCO1 by 100 Hz.

The displayed receiving frequency of the receiver may be described as:

F display = abcde.f kHz

The desired frequency for VCO1 is:

FVCO1 = 38,000.0 kHz + abcde.f kHz
Since the first IF frequency is 38 MHz and the LO always operates above the IF.

The relationship of N1 and N2 to the received frequency is as follows:

N1 = 176 - ab
N2 = 100,000 - cdef

Therefore, the LO output frequency may be expressed in terms of the desired received frequency as:

$$FVCO1 = 224 \times 10^6 - 100(1 \times 10^5 - cdef) - 1 \times 10^6 (176 - ab)$$

For example, if the desired received frequency is 02182.0 kHz, ab = 02, cdef = 1820, so:

$$FVCO1 = 224 \times 10^6 - 100(1 \times 10^5 - 1820 - 1 \times 10^6 (176 - 02)$$
$$= 224 \times 10^6 - 9.818 \times 10^6 - 174 \times 10^6$$
$$= 40.182 \times 10^6$$
$$= 38.000 \times 10^6 + 2.182 \times 10^6$$

Two exceptions to this operating principle exist, however. The USB filter is utilized as the intermediate bandwidth for reception modes other than A3J and, since this filter is centered approximately 1.5 kHz away from the center of the IF, the synthesizer output frequency must be offset by this amount so that the received frequency display is correct. Thus, when the I bandwidth is selected with A1 or A2H, the synthesizer output frequency is reduced by 1.5 kHz from the expected value to achieve the desired relationship. In order to retain correct BFO operation under this condition, the BFO must be offset by 1.5 kHz also. This is accomplished via the two voltage controlled crystal oscillators in the BFO circuitry, one oscillator being offset by 1.5 kHz from the other.

A second exception exists with respect to F1 operation in that the desired audio output frequency is 1.7 kHz. In order to be able to use the existing 1.4 MHz signal (which is developed from the 11.2 MHz oscillator) for F1 demodulation, the synthesizer output frequency is reduced by 1.7 kHz from the expected value when the F1 mode is selected.

Additionally, the synthesizer supplies all reference frequencies for its own use and for use by the remainder of the receiver. The output of an 11.2 MHz temperature compensated crystal oscillator on the reference board is applied to a divide-by-8 circuit to generate 1.4 MHz for use as a local carrier for A3J and F1 demodulation. This is in turn divided by 28 to develop a 50 kHz signal for use by phase lock loop 1 (the summing loop) and the 50 kHz is further divided by 50 to obtain 1 kHz for use by phase lock loop 2. The 11.2 MHz oscillator output is also multiplied by 3 to obtain 33.6 MHz for use by the 38 MHz IF in generating the second local oscillator. The output of one of two voltage controlled crystal oscillators controlled by the CLARIFIER/BFO control at approximately 12.6 MHz is mixed with 11.2 MHz to generate a variable 1.4 MHz BFO signal for A1 demodulation. The output of the 11.2 MHz oscillator is also filtered and then outputted for use by the microprocessor as a

clock signal. Serial data from the microprocessor, after passing through the RF/IF circuitry of the receiver, is applied to a serial to parallel shift register on the programmable divider. The parallel outputs of the register supply the N1 and N2 counters, while the serial output is applied to the line driver on the reference board. The differential line driver output is sent to the microprocessor as a data echo for data verification.

4.3.2 Reference Board (See figures A-9 and A-10)

The reference board contains the 11.2 MHz temperature compensated crystal oscillator and a fixed frequency divider chain to develop the 1.4 MHz local carrier and the 50 kHz and 1 kHz reference frequencies for the two phase locked loops in the synthesizer. Another fixed frequency divider located on the reference board provides for division by 200 of the VCO2 frequency. The reference board also contains the BFO circuit which supplies a variable 1.4 MHz local carrier when the receiver is operated in the A1 mode.

The BFO circuit consists of mixer/oscillator U4 which forms a VCXO at 12.6000 MHz or 12.5985 MHz and mixes with 11.2 MHz to produce the variable 1.4 MHz. The divide by 200 circuit uses U9 which divides by 100 and U10 which divides by 2. Line driver U8 converts data echo information for differential transmission to the microprocessor.

The TCXO assembly (A1) supplies an 11.2 MHz TTL signal to U1. U1 buffers 11.2 MHz into four outputs. One output passes through an 11.2 MHz BPF to provide a sinusoidal signal used as an injection in the synthesizer. A second output feeds a 33.6 MHz BPF which selects the third harmonic of the 11.2 MHz square wave and supplies a 33.6 MHz sinusoid to be used as an injection signal in the receiver. Another output of U1 supplies 11.2 MHz as an injection frequency used by the BFO circuit. The fourth output of U1 drives the frequency divider chain consisting of U2, U3, U5, U6, and U7. U2 divides 11.2 MHz by

8 and supplies two 1.4 MHz outputs. One is filtered to produce sinusoidal 1.4 MHz local carrier in A3J or F1 modes. The other 1.4 MHz output of U2 is divided by 14 in U3 and by 2 in U6 to produce 50 kHz reference frequency. U6 also supplies 50 kHz to U5 which divides by 5 and feeds U7. U7 divides by 10 to give the 1 kHz reference frequency.

4.3.3 Programmable Divider Board (See figures A-11 and A-12) The two programmable dividers (N1 and N2) and two phase comparators (ϕ1 and ϕ2) used in the synthesizer are located on this board. In addition, VCO2 and its loop filter are also on this board, which means the entire loop 2 is on the programmable divider board.

The divide by N1 circuit consists of a high speed voltage comparator (U13) which converts the analog input to TTL level. This is followed by three programmable decade counters (U14, U15, U16) and a reset recognition gate U12.

The reset pulse from U12 is the output frequency of the divide by N1 circuit and it feeds one input of phase comparator 1 consisting of U17, U18 and Q6, Q7 and Q8. The other input is a 50 kHz TTL square wave which comes from the reference board. The output of phase comparator 1 is sent to VCO1 located on the VCO board.

The divide by N2 circuit contains a divide by 10/11 dual modulus ECL prescalar (U1) controlled by a programmable decade swallow counter (U3). U5, U6, U8 and U9 are programmable decade counters which complete the divide by N2 count sequence. The output frequency of the divide by N2 circuit is taken from the reset pulse developed by U10 and fed into phase comparator 2 consisting of U19, U20 and Q9, Q10 and Q11.

The decade counters for both divide by N1 and divide by N2 are programmed by 24 bits of BCD information stored in three 8-bit shift registers (U4, U7, U11) located on the programmable

divider board. These three registers, plus two others elsewhere in the receiver, perform a serial to parallel conversion of 40 bits of data which are sent by the microprocessor board each time a new frequency is tuned or a receiver function is changed.

VCO2 is also contained on the programmable divider board. Q1 and Q2 are the active devices of the oscillator, while L1 and VVC1 form the tuned circuit controlling the frequency of oscillation. The signal is amplified by Q3 and buffered by Q4 to drive the divide by N2 counter on the programmable divider board and the divide by 200 circuit on the reference board. The outputs are level controlled by Q5.

4.3.4 Divide by 20 Board (See figure A-13)

The divide by 20 board divides the VCO1 frequency by 20. The VCO1 frequency enters the divide by 20 board and is amplified by Q1 and fed to ECL flip-flop U1 which divides the frequency by 2. Q2 translates the ECL output to a TTL signal and feeds U2 which divides the frequency by 10. The output of U2 is attenuated and filtered and sent to the VCO Board.

4.3.5 VCO Board (See figure A-12)

The VCO board contains VCO1, plus two mixers and two filters associated with the loop 1 circuit. The 450-to-500 kHz divided VCO2 frequency enters the board along with 11.2 MHz from the reference board, and they are mixed in U1. The output of U1 is filtered by ceramic filter FL1 and amplified by Q1 to serve as a 10.70-to-10.74999 MHz injection signal for mixer A1.
The divided VCO1 frequency enters the VCO board from the reference board and is filtered and fed to mixer A1. The desired 7.35-to-8.8 MHz signal is filtered by a bandpass filter. The filtered signal is amplified by Q8 before being sent out to the divide-by-N1 divider.

VCO1 covers 38.0085 to 67.9999 MHz in two bands with two separate voltage controlled oscillators VCO1a and VCO1b sharing a common output amplifier. For VCO1 operation below 52.0 MHz, a

bandswitch signal is received from the RF filter board and level shifted by Q2 and Q3 to turn on VCO1a. Q4 and Q6 form the active devices of VCO1a and the tuned circuit consists of L14 and two tuning diode pairs VVC1 and VVC2 in parallel. When VCO1a is active, its output feeds the output amplifier consisting of Q13 and Q12. One output of Q12 is fed to the divide-by-20 board. The other output is the injection frequency to the receiver first mixer. For VCO1 operation above 52 MHz, VCO1b is selected by Q9/Q10 and fed to the output amplifier. VCO1b has Q5 and Q7 as active devices, with L15 and one tuning diode pair VVC3 forming the tuned circuit.

A level control signal for both VCO1a and VCO1b is developed by Q11. The tuning voltage for VCO1a and VCO1b is supplied from phase comparator 1 on the programmable divider board and is filtered by the loop filter consisting of C32, C44, C46, and R38.

4.4 MICROPROCESSOR

4.4.1 Microprocessor Block Diagram Discussion

The entire receiver is controlled by a microprocessor which is composed of two circuit boards, the display board and the microprocessor board. A basic block diagram of the microprocessor system is shown in figure 4-2.

Keyboard entry of receiver frequency, bandwidth and mode, as well as certain other functions (tune, scan, preselector), are converted by the microprocessor into the necessary data to control the receiver and then this data is transmitted as a serial data word to the RF/IF/Synthesizer portion of the receiver. The microprocessor system consists of seven basic elements: a central processing unit (CPU), read only memory (ROM), random access memory (RAM), parallel input/output, serial input/output, a display, and a keyboard. The CPU (the actual microprocessor) is the heart of the system and performs the required data operations in response to commands entered via the keyboard and the parallel input circuitry. The data operations performed by the CPU are defined by the system program which is permanently stored in the read only memory (ROM). As the name implies, the CPU may only read data from the ROM, storage of data is not possible. Any data which must be stored by the CPU during operation is stored in the random access memory (RAM) into which data may be entered and from which data may be read. This is the memory in which operator stored frequencies are placed, as well as other internal data which the CPU must temporarily store during operation. The RAM is provided with a standby battery supply so that stored data is retained even when the receiver is turned off. Data resulting from operations by the CPU is either applied via the parallel output to the display and/or via the serial output to the RF/IF/Synthesizer section. Data sent to the RF/IF/Synthesizer is fed back to the microprocessor, by means of the serial input, for verification prior to use. The serial input is also used to accept the clock signal which is supplied by the synthesizer.

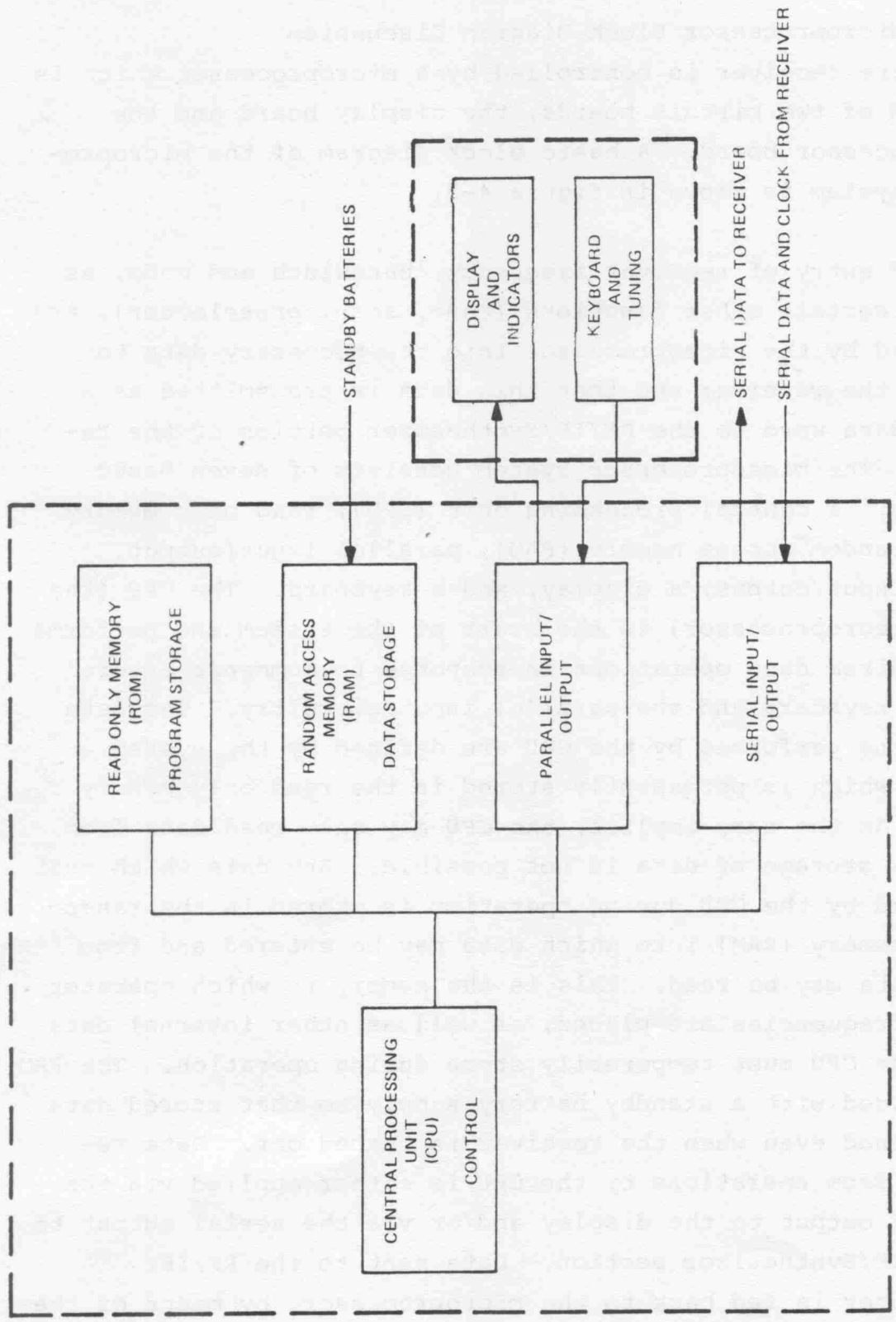

Figure 4-2 Basic Microprocessor System Block Diagram

4.4.2 Receiver Control Data

The serial output of the microprocessor is a 40-bit word, which is sent serially to the RF/IF/Synthesizer section of the receiver. In the serial to parallel shift register, this serial word is converted to parallel form for use as indicated below. Refer also to figure 4-3.

Bits 0-7: Synthesizer N1 ratio. These eight bits, representing 2 Binary Coded Decimal (BCD) digits, are applied directly to the N_1 divider in the synthesizer to specify 1MHz tuning steps.

Bits 8-24: Synthesizer N2 ratio. These 17 bits, representing 5 BCD digits (the first digit is either 0 or 1), are applied directly to the N_2 divider in the synthesizer to specify 100kHz, 10kHz, and 100Hz tuning steps.

Bits 25-26: Synthesizer VCO Band. Depending upon the desired frequency, these 2 bits select one of two VCOs in the synthesizer.

Bits 27-28: Spare

Bits 29-32: RF Filter or Preselector Selection. These four bits represent a binary number that determines the RF filter to be selected. They are applied via a binary to decimal decoder to the RF filter switching network.

Bits 33-36: Demodulation Mode Selection. These four bits, representing the four possible demodulation modes, are applied to the demodulator and also to the synthesizer (via a decoder) to select the correct local carrier.

Bits 37-39: If Filter Selection. These three bits represent a binary number that determines the IF filter to be selected. They are applied via a binary to decimal decoder to the filter switching network. They also determine the selection of either the centered or offset BFO in the synthesizer. The offset BFO is required when utilizing the intermediate bandwidth.

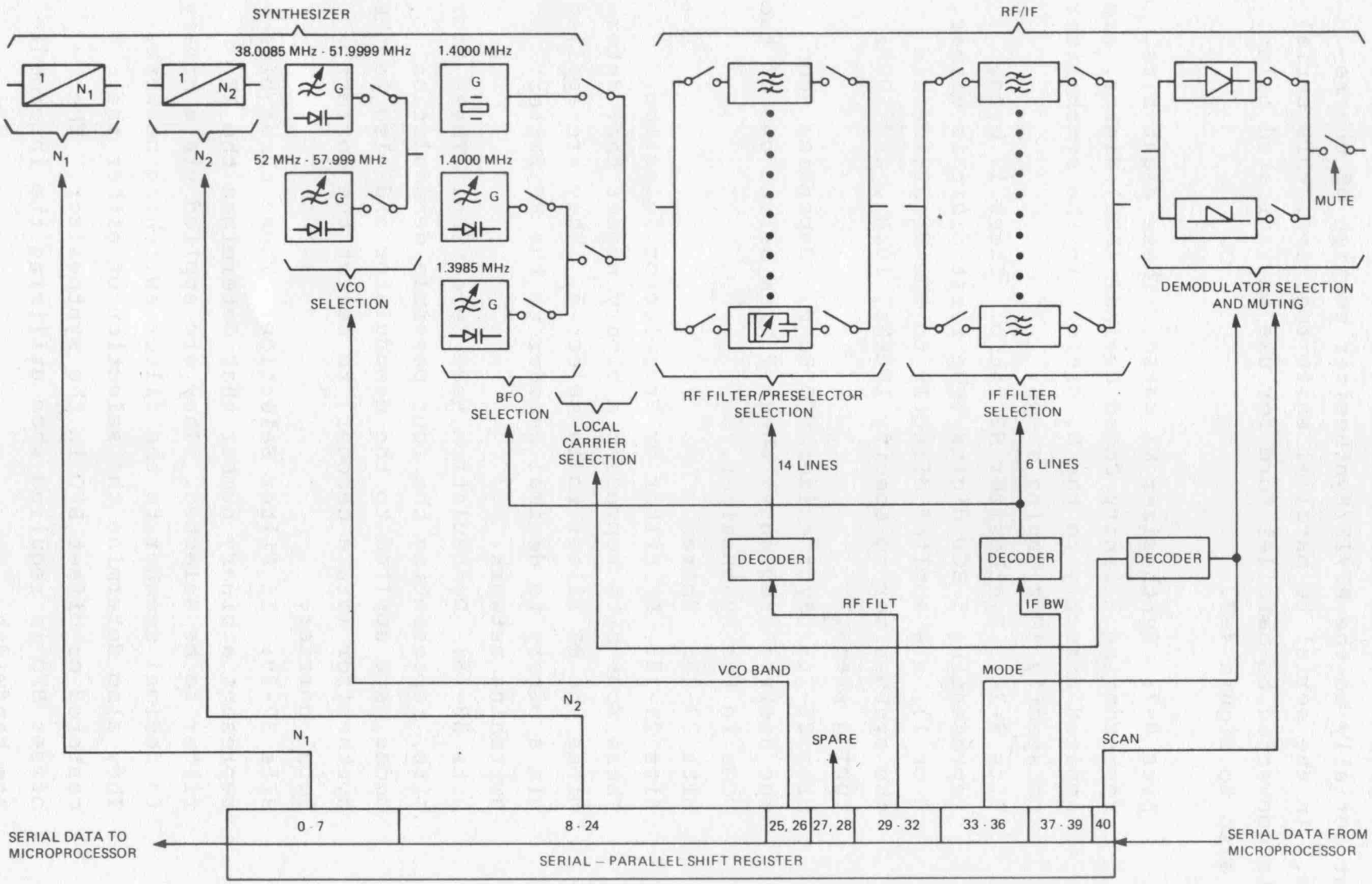

Figure 4-3 Receiver Control Block Diagram

Bit 40: Scan Selection. This bit is used to enable muting of the receiver output as the receiver frequency is changed in the scanning operation.

Thus, any time a new frequency, mode or bandwidth is selected, a new data word is transmitted in which some or all of the bits have changed.

4.4.3 Microprocessor Board

4.4.3.1 Block Diagram Description (See figure 4-4.)
The 11.2MHz reference signal from the synthesizer is applied to counter U12 which develops the required biphase clock at a frequency of 1.12MHz. The clock is applied to the 8-bit central processing unit U7, an 8080A. The 16-bit address output of the CPU is applied to address drivers U25 and U30; the 8-bit data bus is connected to data drivers U6 and U18 with one bit connected also to differential receiver U23. Outputs of both the address and data drivers are applied to the system read only memory (ROM) and random access memory (RAM). The data driver outputs are also applied to status latch U10 and the display latch/drivers. The system ROM has a capacity of 3000 8-bit words in three memory integrated circuits; the system RAM has a capacity of 256 8-bit words in two memory integrated circuits. Selection of ROM or RAM circuits is made by address decode logic under control of the CPU. Address decode logic under control of the CPU also selects the display latch/drivers when update of the display or indicators is required. Status latch U10 generates signals indicating whether data is to be written into or read from memory. This information is utilized by the address decode logic for memory control. Final data output to the RF/IF/Synthesizer section occurs via differential transmitter U28, and data echo for verification is received at the CPU via differential receiver U23.

4.4.3.2 Circuit Description
Referring now to the schematic of the microprocessor board, figure A-15 and A-16, the circuitry will be described by functional sections.

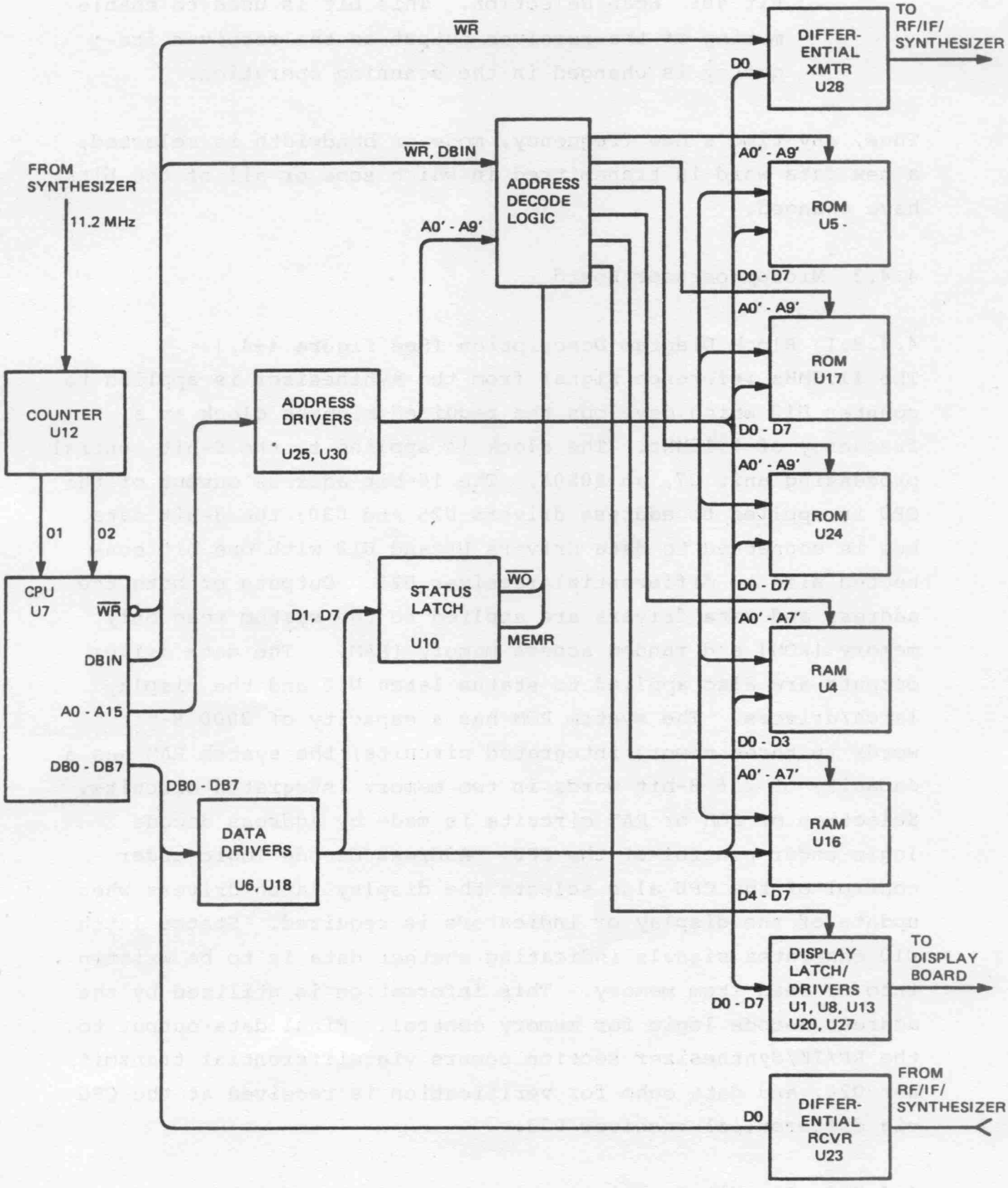

Figure 4-4 Microprocessor Board, Block Diagram

4.4.3.2.1 Clock Generator

Counter U12 is connected as a symmetrical divide by 10 counter. The basic 11.2 MHz frequency is connected to clock 2, terminal 6. The QD output pin 12 is connected to clock 1, terminal 8. This arrangement provides a symmetrical output square wave divided-by-ten at QA output pin 5.

The gating arrangement at U19 and U26 provides $\phi 1$ pulses 178 ns wide and $\phi 2$ 445 ns wide, with the leading edge of $\phi 2$ lagging that of $\phi 1$ by 178 ns.

4.4.3.2.2 Microprocessor (See figures A-15 and A-16)

The 8080A microprocessor is a complete 8-bit parallel, central processor unit (CPU). The CPU transfers data and internal state information via an 8-bit, bidirectional 3-state bus (DO -D7). Memory and peripheral device addresses are transmitted over a separate 16-bit 3-state address bus (A0 - A15). Three timing and control outputs (SYNC, DBIN, $\overline{WR}$) originate from the CPU. Inputs to the CPU include: four control inputs (READY, HOLD, INT, and RESET), four power inputs (+12V, +5V, -5V, and GND) and two clock inputs ($\phi 1$ and $\phi 2$).

The function of the CPU pins used in this application is briefly stated as follows (See figure A-16, U7):

A0 - A15 (output three-state). ADDRESS BUS. The address bus provides the address to memory (up to 64K 8-bit words) or denotes the I/O device number for the output devices. A0 is the least significant address bit.

D0 - D7 (input/output three-state). DATA BUS. The data bus provides bidirectional communication between the CPU, memory, and I/O devices for instructions and data transfers. Also, during the first clock cycle of each machine cycle, the CPU outputs a status word on the data bus that describes the current machine cycle. D0 is the least significant bit.

SYNC (output). SYNCHRONIZING SIGNAL. The SYNC pin provides a signal to indicate the beginning of each machine cycle.

DBIN (output) DATA BUS IN. During the input of data to the CPU, the CPU generates a DBIN signal which is used externally to enable the transfer. DBIN signal indicates that the data bus is in the input mode. This signal is used to enable the gating of data onto the CPU data bus from memory or I/O.

$\overline{WR}$ (output) WRITE. The $\overline{WR}$ signal is used for memory WRITE or I/O output control. The data on the data bus is stable while the $\overline{WR}$ signal is active low.

RESET (input) RESET. While the RESET signal is activated, the content of the program counter in the CPU is cleared. After RESET, the program will start at location 0 in memory.

$\phi 1$ and $\phi 2$. These pins accept two externally supplied clock pulses. These two pins are 0 to +12V levels.

INT and HOLD. These functions of the CPU are not used, and these pins are tied low.

READY. The READY line is tied to the WAIT line. This automatically forces one wait state during each machine cycle.

4.4.3.2.3 PROM (PROGRAMMABLE READ ONLY MEMORY)

The PROM is a type M2708 high speed 8192 bit (1K words x 8-bit organization), ultraviolet erasable and electrically programmable PROM (EPROM). It is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device.

4.4.3.2.3 PROM (PROGRAMMABLE READ ONLY MEMORY) (continued)
In this application, the address inputs are pins 1-8, 22, and 23, with pin 8 being the LSB (Least Significant Bit) and pin 22 the MSB (Most Significant Bit). The data I/O are pins 9-11, and 13-17, with pin 9 being the LSB and pin 17 the MSB. A low state on pin 20 enables the read function.

4.4.3.2.4 RAM (RANDOM ACCESS MEMORY)
The RAM is a type 5101 ultra-low power 1024 bit (256 words x 4 bits) static RAM. The device has two chip enable inputs. Minimum current is drawn when CE2 pin 17 is at a low level. When the device is not selected, it only draws 10 microamps from the power supply or the standby batteries. It is not necessary to pulse the chip select pin for each address transition. The data is read out non-destructively and has the same polarity as the input data.

In this application, the address inputs are pins 1-7 and 21, with pin 4 being the LSB and pin 7 the MSB. The data inputs are pins 10, 12, 14, and 16 and the data outputs are pins 9, 11, 13, and 15. The write function requires a low on CE1, a high on CE2, and a low on R/$\overline{W}$, in which case the data out is the same as the data in. In the read function, a low is required on CE1, a high on CE2, and a high on R/$\overline{W}$, in which case the output is data out.

4.4.3.2.5 Address Bus Drivers
Bus drivers U25 and U30 are hex drivers with 2-line and 4-line enable inputs and six non-inverted 3-state outputs. All enable input pins of U25 and U30 are tied low so that the address outputs are in either the low or high states. Outputs labeled A0' through A9' are applied to the input pins of the three ROM chips, as well as all address lines on the board.

4.4.3.2.6 Address Decode Logic

Under program control, the CPU manipulates address bits through selective gates to control memory, and latches and drivers at the input/output of the microprocessor board.

ROM selection uses gates U15A/B/C/ and inverters U22D/E. The DBIN signal from the CPU, indicating the data bus is in the input mode, and MEMR enables the gates. Then, address bits A10 and A11' select ROM U5; address bit A10 selects ROM U17; address bit A11' selects ROM U24.

RAM enabling uses gate U29B. When DBIN, MEMR, and address bit A12' are set, a low state is placed on CE1 of U4 and U16.

When the $\overline{WO}$ and WR signals are present, the display and indicator output latches are enabled as follows: For bandwidth and mode indication, U27 is enabled by U21A when address bits A0' and A15' are set; function indicators (error, recall, store, frequency, tune, preselector, and scan) are enabled by U14D when address bits A1' and A15' are set; digit select U6 is enabled by U9D when address bits A2' and A15' are set; and segment select U1 is enabled by U2D when address bits A3' and A15' are set.

At output connector contacts J2-3, J2-5, and J2-7, address bits A0', A1', and A2', in conjunction with A15' and A4' for read enable, are available to the display board for decoding and keyboard reading. Count Reset (CNT RST) at J2-1 is enabled by U3C when address bits A6' and A15' are set and $\overline{R}/W$ is true. Count Reset is used by the manual tuning control circuitry on the display board.

4.4.3.2.7 Data Bus Drivers

Data bus drivers U6 and U18 are operated in the tri-state mode. Upon receipt of DBIN from the CPU, the drivers assume a high impedance and are effectively removed from the bus.

The data outputs are labeled D0-D7 and are applied to RAM chips U4 and U16, and to the display output latches U1, U8, U13, U20, and U27.

4.4.3.2.8 Status Latch

Status latch U10 is a 4-bit bistable latch, of which only two bits are used. Data bits D1 and D7 are applied as inputs. When D1 is present, the output is WO, a write memory function. When D7 is present, the MEMR output designates that the data bus will be used for memory read data. The enable signal originates from the SYNC output of the CPU and the $\phi 1$ clock.

4.4.3.2.9 Data Transmission

The microprocessor board is interconnected with the display board by means of connectors J1 and J2 and two ribbon cables. It is interconnected with the RF/IF Synthesizer through the edge connector P1. The RF/IF Synthesizer interface is made at P1 by differential line driver U28 and differential line receiver U23. These are quad differential units, each containing a common enable and disable function control that controls all four elements within each unit.

When data bus drivers U6 and U18 are in the high impedance state, data is read into the CPU from either the keyboard, the ROM memory, or the echo back function. The pullup resistors in U11 supplement the drive power from the ROM chips.

Data transmission to the RF/IF Synthesizer operates in the following manner. Serial data, 40 bits at a time, is transmitted from the CPU (P1-H, P1-7) to shift registers in the RF/IF Synthesizer circuitry. Data is shifted through the registers by the clock A and B signals (P1-D, P1-E). Data is transmitted twice, with the second transmission causing the release of the first transmission as an echo to the CPU (P1-9, P1-J). The CPU makes a comparison. When a correct comparison is made, the CPU enables strobe A and B outputs (P1-B, P1-C) to the RF/IF Synthesizer, latching the data into the RF/IF Synthesizer shift registers and thus making the desired selections in the receiver.

4.4.3.2.10 Power Circuits

Operating voltages for the microprocessor board are filtered at the input power connections on P1. When power is applied to the receiver, the +5V, +9V, and +12V levels are sensed in the power on reset circuit comprising U31 and U19B. U19B applies a high to the CPU reset pin for 1.4 seconds. After that time, the reset goes low. CE2 of the RAM must be low during power up and power down, but is normally held high. The low prevents the loss of information stored in RAM during power up and power down operations.

Diode CR1 prevents any charging current to the standby batteries B1 and B2. On the other hand, when external power is removed from the receiver, the batteries maintain power through CR1 to the two RAM chips so that the information stored in the RAM will be retained. Thus, the operator need not key into memory the list of most used operating frequencies each time the receiver is turned off. Diode CR3 prevents draining batteries through the operating voltage circuits.

4.5 DISPLAY BOARD

Two ribbon cables interconnect the display board and the microprocessor board. Requests from the operator are transmitted to the microprocessor, and microprocessor responses and actions are received at the display board. Operating voltages are also obtained from the microprocessor board. Refer to the block diagram, figure 4-5 and the appropriate logic diagram, figures A-17, A-18, A-19.

See figure A-17. Operating voltages are applied to display board connector J2 pins 39 through 50. Throughout the board, various capacitors and a choke suppress transients on the voltage buses.

See figure A-18. Indicator lights on the display board are activated by microprocessor control signals through drivers U17 and U25. The digital display consists of six 7-segment digital LED displays U9-U14. Of these, only U13 has the decimal point display and the others are numerical. All displays are normally on--the microprocessor signals steal current from segments that should not be lit. All displays are multiplexed, i.e., the microprocessor program refreshes the lamps and digital displays. At connector J2, D1S through D6S are microprocessor-derived enabling signals to buffer U16 for the six digits; DPE is the decimal point enabling signal. SAL through SGL are the segment enabling signals to buffer U15 for the seven segments of the selected display.

See figure A-19. Under program control, the microprocessor outputs an address to U3, a 3- to 8-line decoder, and the decoded address selects a bank of switches. A keyboard read command then enables the tristate gates U1, and the identity of the depressed button is placed on the appropriate DBO-DB5 data bus back to the microprocessor.

In a similar manner, addresses are decoded and data is placed on the data buses via tristate gates U4 and U8 for the following:

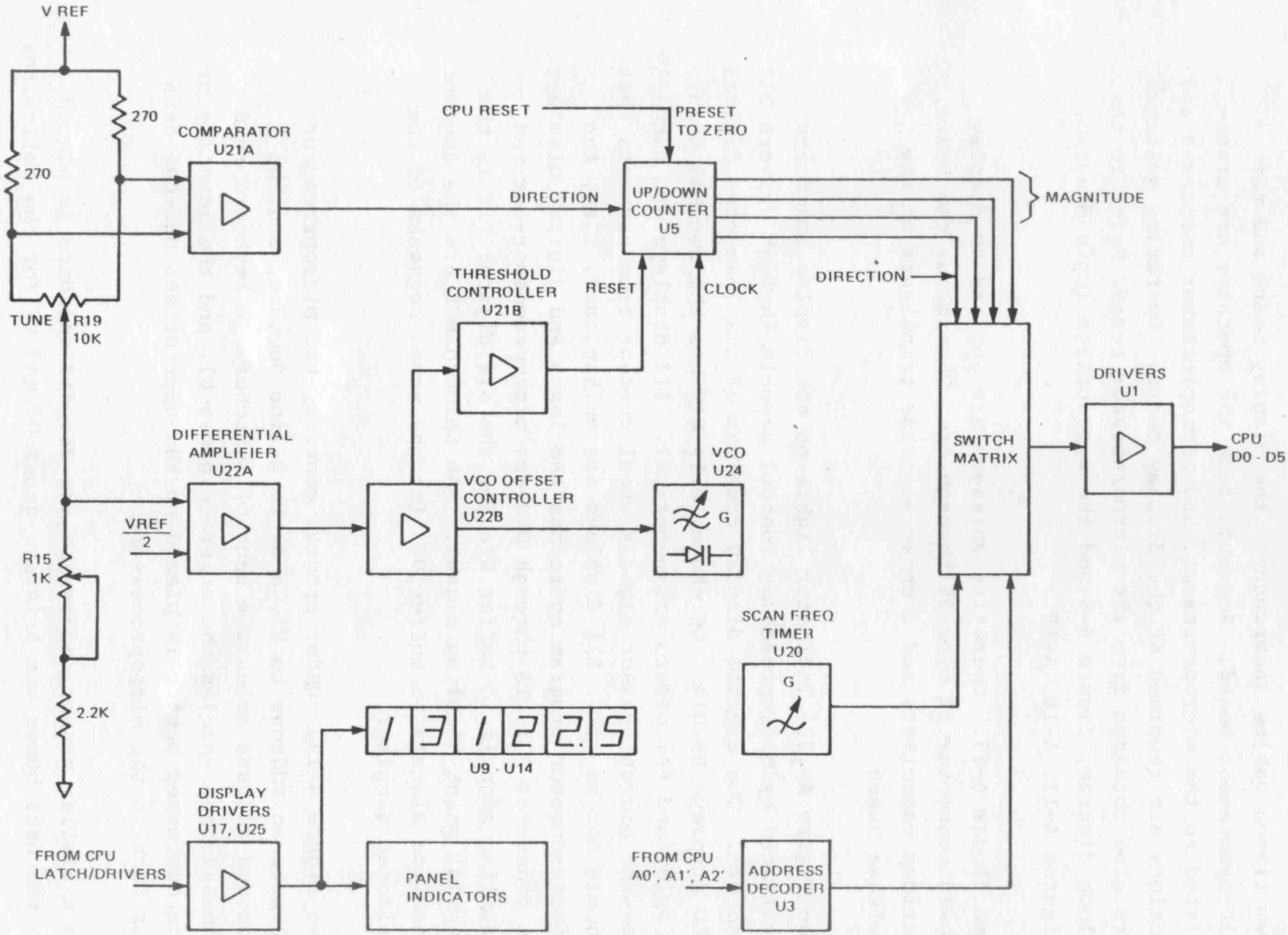

Figure 4-5 Display Board, Block Diagram

when in manual tune, the requested direction and rate; when in scan function, the dwell time on each channel.

In manual tuning, the operator rotates the centered tuning knob CW to increase the frequency or CCW to decrease the frequency. The amount of rotation from center determines the rate of frequency change.

A reference voltage, established by VR1, is applied to both ends of the tuning control R19. The arm of R19 is connected to R15 and a U18 resistor to ground. When the tuning knob is moved off center, more voltage appears on one side of the comparator U21A than the other side. This represents the direction of the desired frequency change (up or down). The output of this comparator drives the up/down control imput to the binary counter U5.

With the ends of tuning control R19 connected to the reference voltage, it can be seen that the potentiometer represents two variable resistors in parallel with respect to the potentiometer arm. With the arm at center rest, both resistors have equal value and a corresponding voltage is applied to one input of differential amplifier U22A-3. The other input to U22A is obtained from the reference voltage across the voltage divider derived from U18 resistors. With the arm turned to a selected position (off center), the paralleled sections of the potentiometer have a combined resistance less than that represented by the smaller of the two. Consequently, a higher voltage than that obtained at rest is applied to U22A-3. U22A provides an output voltage relative to the amount the tuning control was offset from the center position.

The output of the differential amplifier U22A drives op-amp U22B. U22B is connected in a configuration that minimizes device-to-device variations in the frequency vs. voltage characteristics of voltage controlled oscillator U24. Dependent upon the amplitude of the input voltage to U24-9, an output

frequency in the range of 0.5 to 50 Hz is connected from U24-4 to the clock input of U5. The voltage divider, consisting of resistors from U6, drops the +12V output signal to the required +5 volts for the input to U5.

Note that the voltage at U24-11 is also applied to the inverting input of comparator U21B. By connection to the reset terminal of counter U5, U21B establishes the threshold for counting operation, i.e., did the operator turn the tuning knob sufficiently to warrant incrementing or decrementing the up/down counter. A high at U5 pin 9 resets the counter to zero. Pins 3, 4, 12, and 13 of U5 are tied to ground. When the counter reset signal (high) from the microprocessor is applied to the preset enable of U5, the fact that P1-P4 terminals are held low, transfers lows to the Q output terminals and the counter therefore starts from zero. The use of counter U5 is necessary so that rapid frequency change information from the tuning circuitry will not be missed by the microprocessor while it is performing some other operation.

4.6 CHASSIS INTERCONNECTION BOARD

Refer to the schematic diagram, figures A-20, A-21, and A-22. This interconnection board contains the majority of circuits required to interconnect and supply power to all other receiver circuit boards. Edge connectors are provided to connect to all circuit boards, except the display board and power supply boards.

Whereas the power supply boards contain the rectifiers and filters for the receiver operating voltages, the chassis interconnection board contains voltage regulators as follows: For the RF/IF boards--regulators VR1, VR2, VR3, and CR1; for the synthesizer boards--regulators VR5, VR6, VR7, and CR3 and CR4; for the microprocessor board--VR4, VR8, VR9, VR10.

The interconnection board mounts the following controls: CLARIFIER, BFO, VOLUME, SENSITIVITY, AND PRESELECTOR.

4.7 POWER SUPPLY

4.7.1 Block Diagram Discussion

Refer to the block diagram, figure 4-6. The power supply consists of three elements--a power transformer, a power relay printed circuit board, and a power filter printed circuit board.

The power supply operates from AC mains at 110 or 220 V±10%, (47 to 63 Hz), or 24 VDC -10%, +30%.

The AC and DC power sources are connected to AC and DC line filters to provide isolation from EMI disturbances. For operation on AC, input power is applied to transformer T2. The secondaries of T2 are connected to four rectifier filter circuits providing unregulated +40V, +15V, +8V, and -8V operating voltages for circuit boards in the other sections of the receiver. An AC line voltage monitor circuit switches receiver operation from the AC source to the DC source when the AC source has fallen below a preselected voltage. A variable control allows selection of the voltage over a considerable range.

When operation is switched to the DC source, an oscillator/divider circuit is activiated to provide a 200 Hz input to the drivers of the DC primary winding of T2, resulting in continued operation of the rectifier circuits. Taps on that primary winding are selected by a relay to automatically select a transformer winding ratio that will compensate for changes in the amplitude of the 24 VDC standby power source. This minimizes internal power dissipation which may otherwise occur due to the wide input voltage range of the DC supply.

4.7.2 Power Relay Board

Refer to the schematic diagram, figure A-23. S1 on the volume control is the power on/off switch and applies AC and DC to the

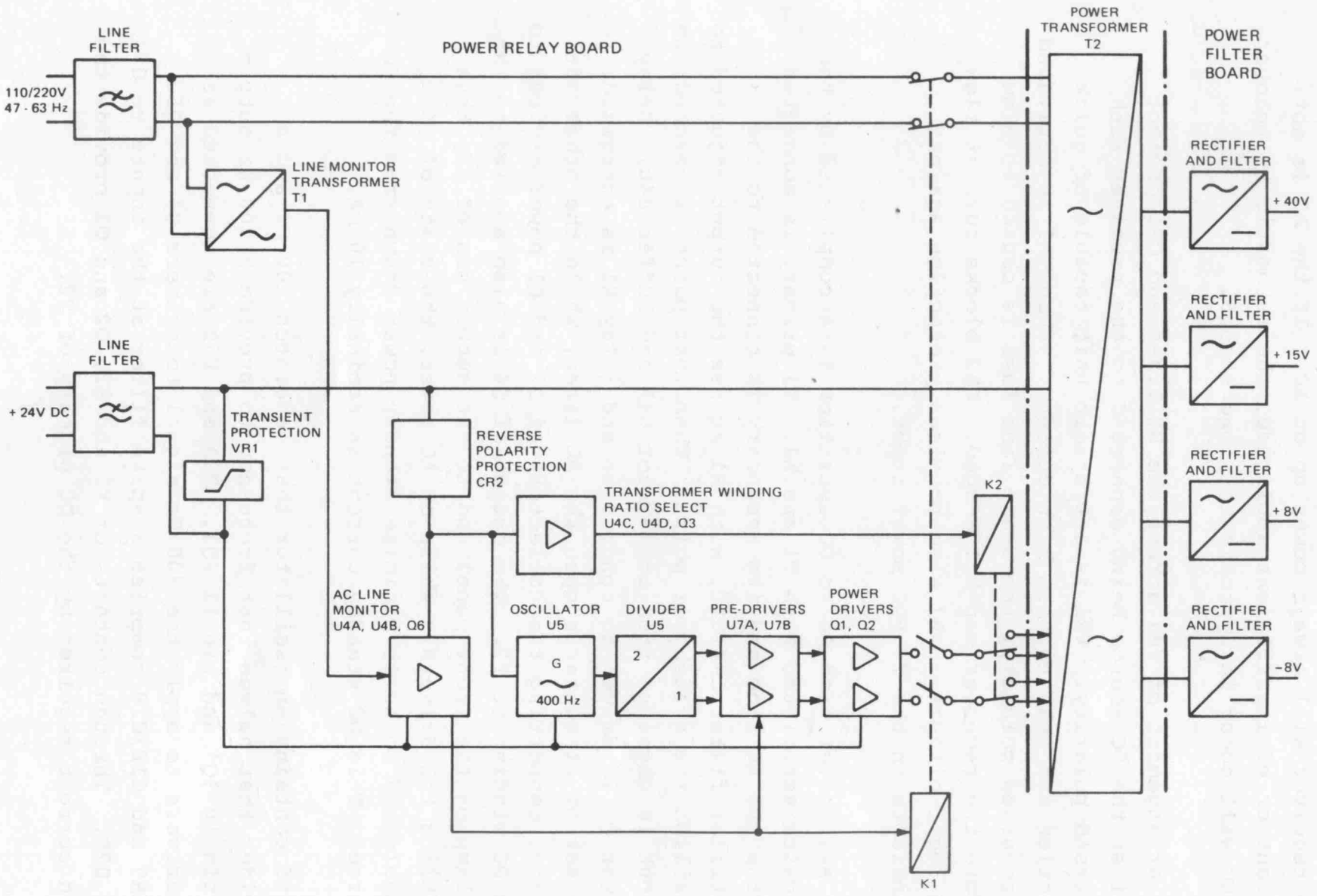

Figure 4-6 Power Supply, Block Diagram

circuits on the power relay board. If the switch is turned on, the receiver will always power up on AC. If the AC is not present or of insufficient amplitude, the automatic switchover to DC will occur in approximately one second.

The arrangement of VR1 across the DC lines and CR2 protect against the DC source being connected to the receiver with reversed polarity. VR1 is a transorb unit capable of quick reaction and able to pass high current. When VR1 is activated by reversed polarity, the 5-amp line fuse is caused to blow before the receiver can be damaged. CR2 blocks current flow to the logic circuit. VR1 also provides protection against transients on the 24 VDC power input.

The switchover from AC to DC operation is accomplished by the circuits associated with T1 and K1. T1 primary is connected across the AC line and its secondary is connected to the rectifier filter CR4/C10, with R1 across the output adjusted to establish the switchover point. When that point is reached, an output is obtained from comparator U4A and buffer U4B. Relay driver Q6 is driven to conduction and relay K1 is energized. One set of K1 contacts open the AC lines, while the other set closes, connecting the collectors of Q2 and Q1 power devices to the DC winding of T2. The output of Q6 is also applied to the DC lamp on the front panel and to the supply pin of U7, thus enabling the drivers. While on AC power, the state of Q6 disables U7 so as to minimize standby power drawn from the DC source. This DC standby current is nominally 10 mA.

IC U5 contains an oscillator that generates 400 Hz and a divider that halves that frequency to provide a 200 Hz output at pin 10 (Q) and pin 11 (Q). U7A and U7B are connected as predrivers to apply the 200 Hz signal to drivers Q4 and Q5. R8/R9 and C18/C19 comprise a spike filter at the inputs to U7A and U7B. Through contacts of K1 and K2, Q2 and Q1 provide the high current required by the DC primary of T2.

Compensation for variations above and below the normal +24 VDC power source are accomplished by circuit elements U4C, U4D, Q3, K2, and the DC winding of T2. Connected across the DC line are the voltage divider U3 (150k) and R2 to establish the state of the lines, and VR2 to provide a reference. Comparator U4C is connected across these two points to detect variations. The output from U4C is applied through buffer U4D to driver Q3. Relay K2 is energized and K2 contacts select either of two winding ratios on the DC winding of T2.

4.7.3 Power Filter Board.

Refer to the schematic diagram, Figure A-24. The secondary windings of the power transformer are connected to four rectifier-filter circuits which supply the four unregulated DC voltages required by the receiver.

SECTION 5
MAINTENANCE

WARNING

A high voltage hazard exists as soon as the covers are removed from the receiver.

CAUTION

Exercise care in handling all receiver circuit boards, as many of them contain integrated circuits which may be damaged by static voltages. Additionally, even when removed from the chassis, the microprocessor board has power due to the batteries; therefore, take care to avoid short circuiting the traces on the rear of the board, as damage to the board may result.

5.1 PREVENTIVE MAINTENANCE

The modern design of the 2000 Main Receiver is such that it requires relatively little preventive maintenance.

Maintenance work inside the receiver should only be carried out by skilled personnel. When such work is carried out, the AC power plug must be taken out of the AC line supply and/or the battery disconnected.

Maintenance work carried out in the vicinity of frequency-determining parts such as coils, trimmers, or variable capacitors is to be performed with great care to avoid damaging the components or changing their settings.

5.2 CORRECTIVE MAINTENANCE

5.2.1 Disassembly Of The Receiver

Access to the circuit boards is gained by removing the top and bottom covers and the front panel.

To remove the covers, remove the screws around the edge of the cover and on the cover surface.

To remove the front panel, first remove all panel knobs. The front of each knob is an insert. Carefully pry off the inserts to expose the knob securing nuts. Next, remove two hex screws that secure each handle and remove the handles. Two rectangular holes in each side panel provide access to the above hex screws. Now, carefully remove the front panel to gain access to the display board.

Figures 5-1 and 5-2 are top and bottom views of the receiver with top and bottom covers removed. Except for the power supply boards and the display board, all circuit boards may be removed by withdrawing them upward to separate the edge connectors on the boards from receptacles mounted in the chassis interconnection board. The power supply boards and the display board are screwed to standoffs on the chassis. When reinserting the circuit boards, take care that the connectors are aligned.

5.2.2 Maintenance Aids

Logic diagrams for each circuit board are furnished in the Appendix to this manual. In addition to figures 5-1 and 5-2 which identify the circuit boards as mounted in the receiver, component location diagrams for each circuit board are furnished in figures 5-3 through 5-18.

1. RF FILTER BOARD
2. PRESELECTOR BOARD
3. 38 MHz IF BOARD
4. 1.4 MHz IF FILTER BOARD
5. 1.4 MHz IF/DEMODULATOR BOARD
6. REMOTE INTERFACE BOARD
7. VCO BOARD
8. DIVIDE BY 20 BOARD
9. PROGRAMMABLE DIVIDER BOARD
10. REFERENCE BOARD
11. MICROPROCESSOR BOARD
12. DISPLAY BOARD
13. CHASSIS INTERCONNECTION BOARD
14. POWER RELAY BOARD
15. POWER FILTER BOARD

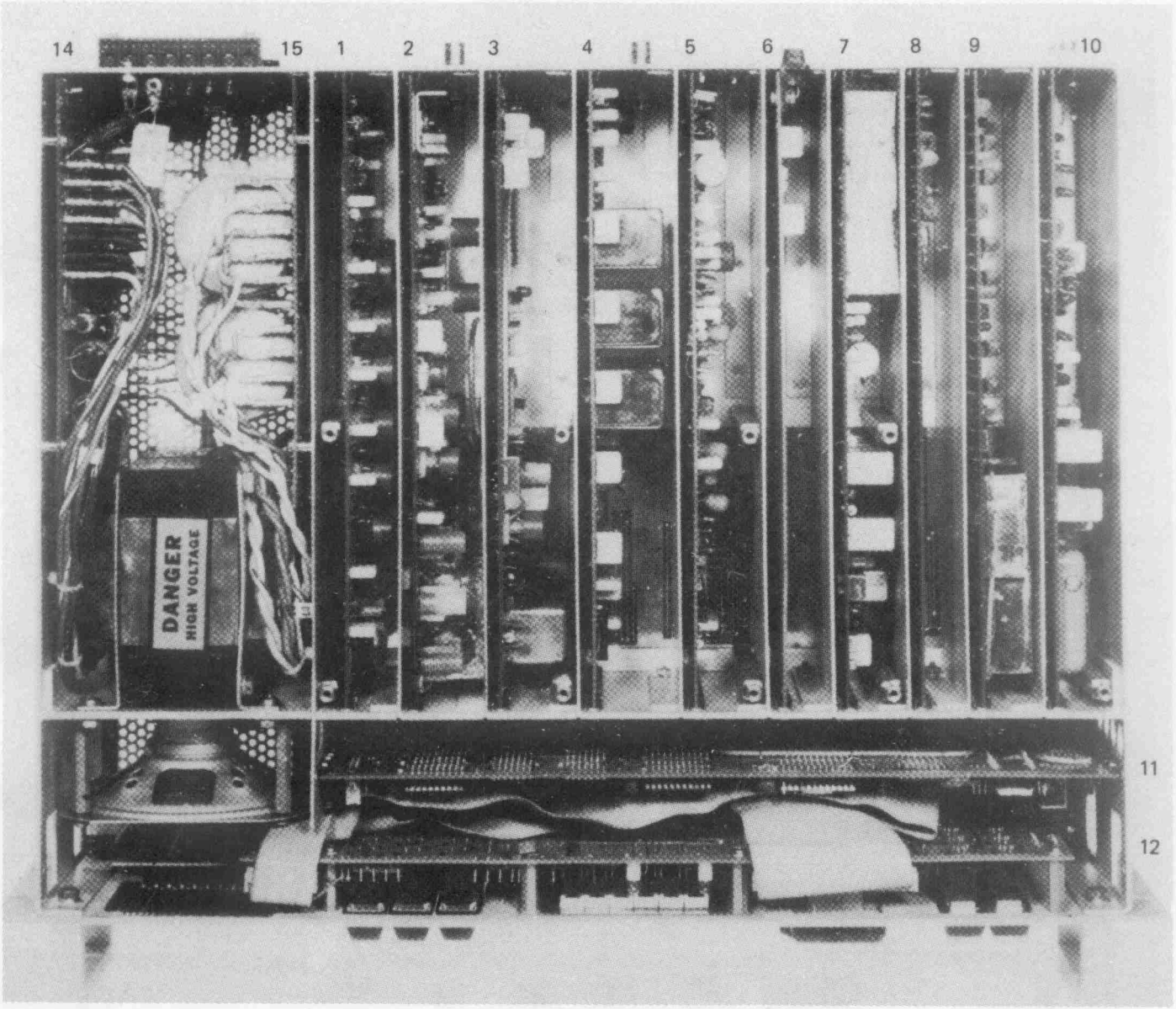

Figure 5-1 2000 Receiver, Top View (Cover Removed)

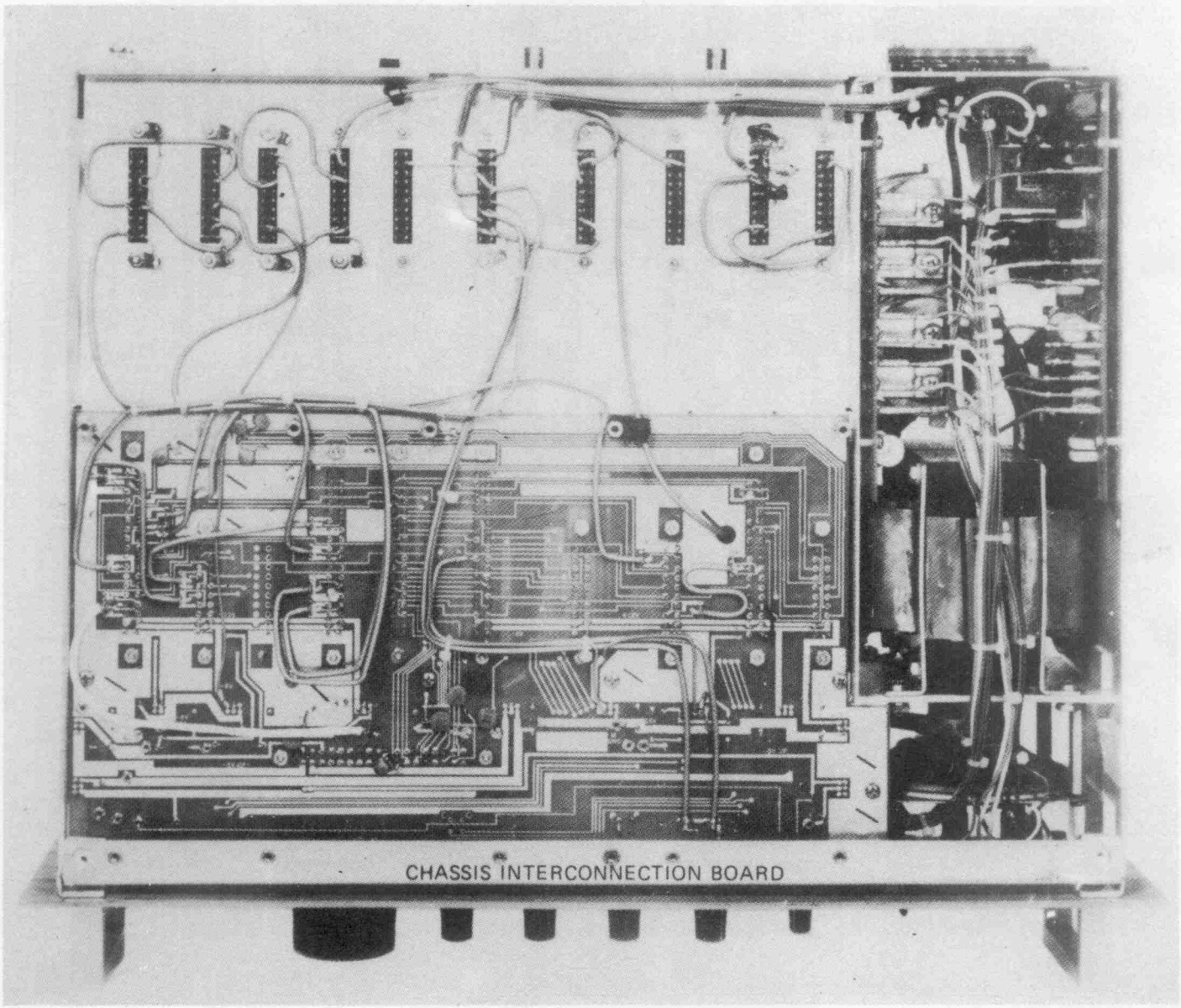

Figure 5-2 2000 Receiver, Bottom View (Cover Removed)

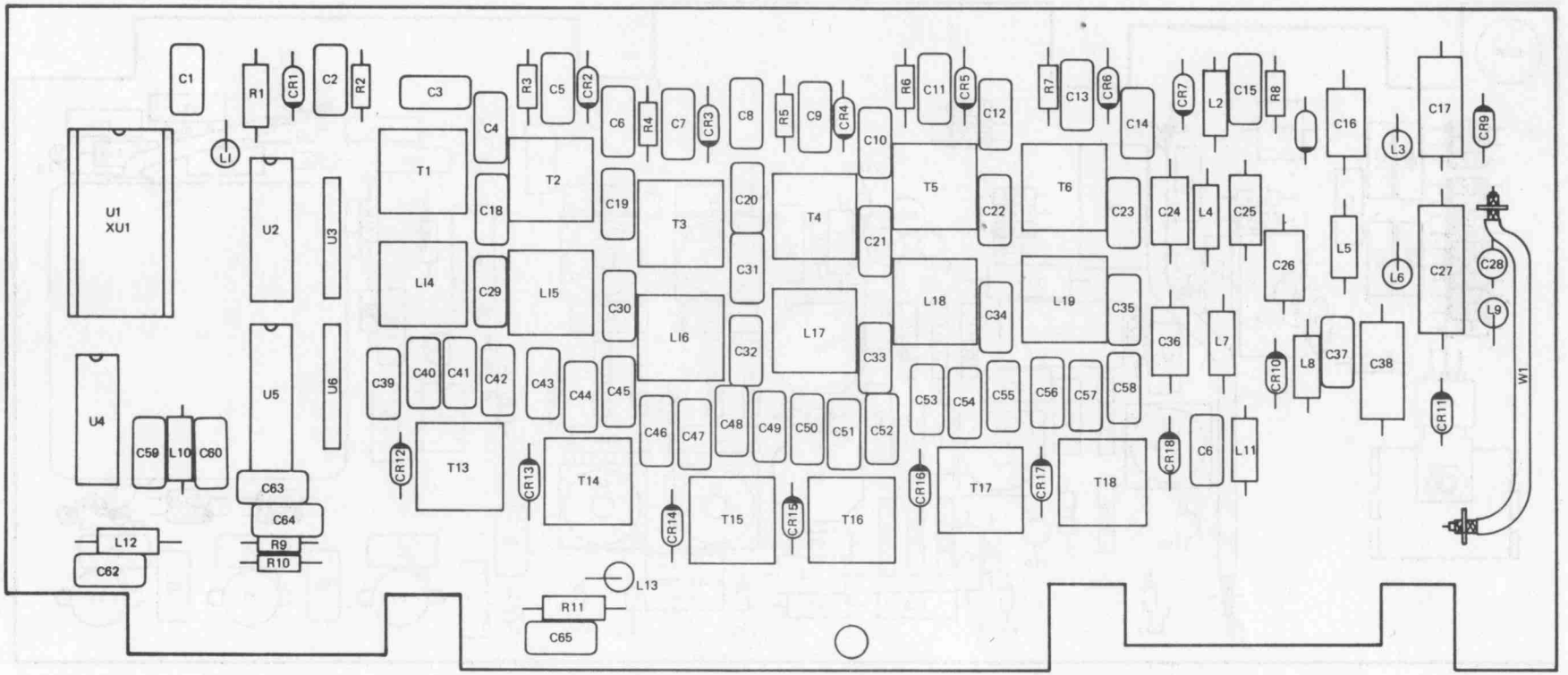

Figure 5-3 RF Filter Board, Component Locations

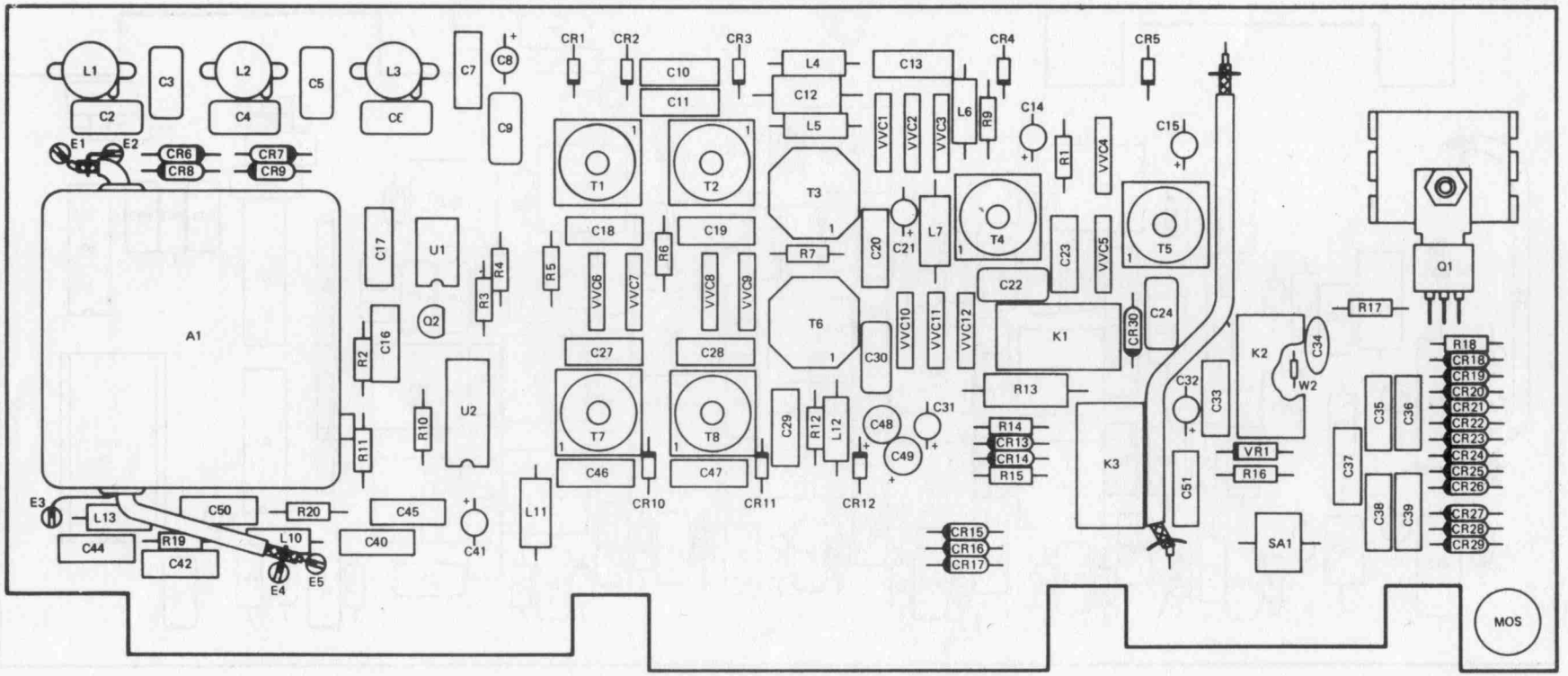

Figure 5-4 Preselector Board, Component Locations

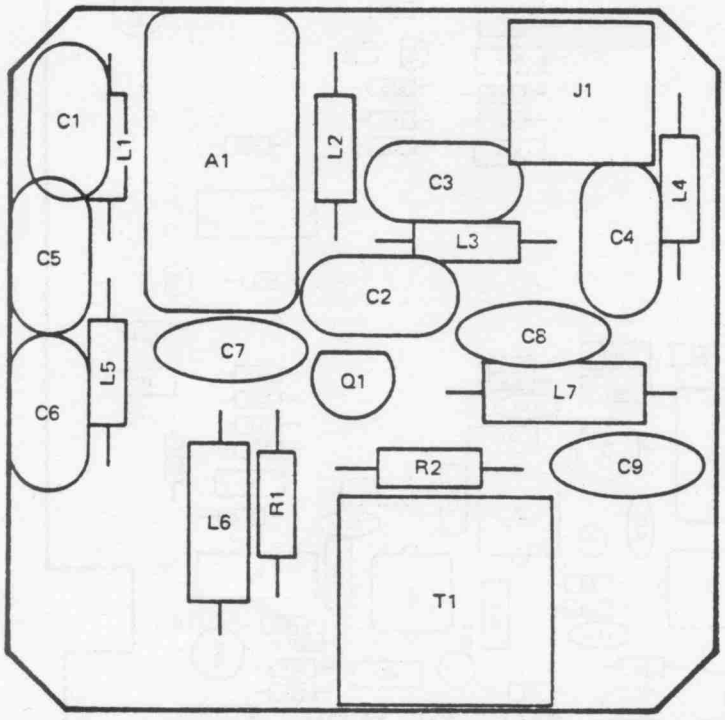

Figure 5-5 First Mixer Board, Component Locations

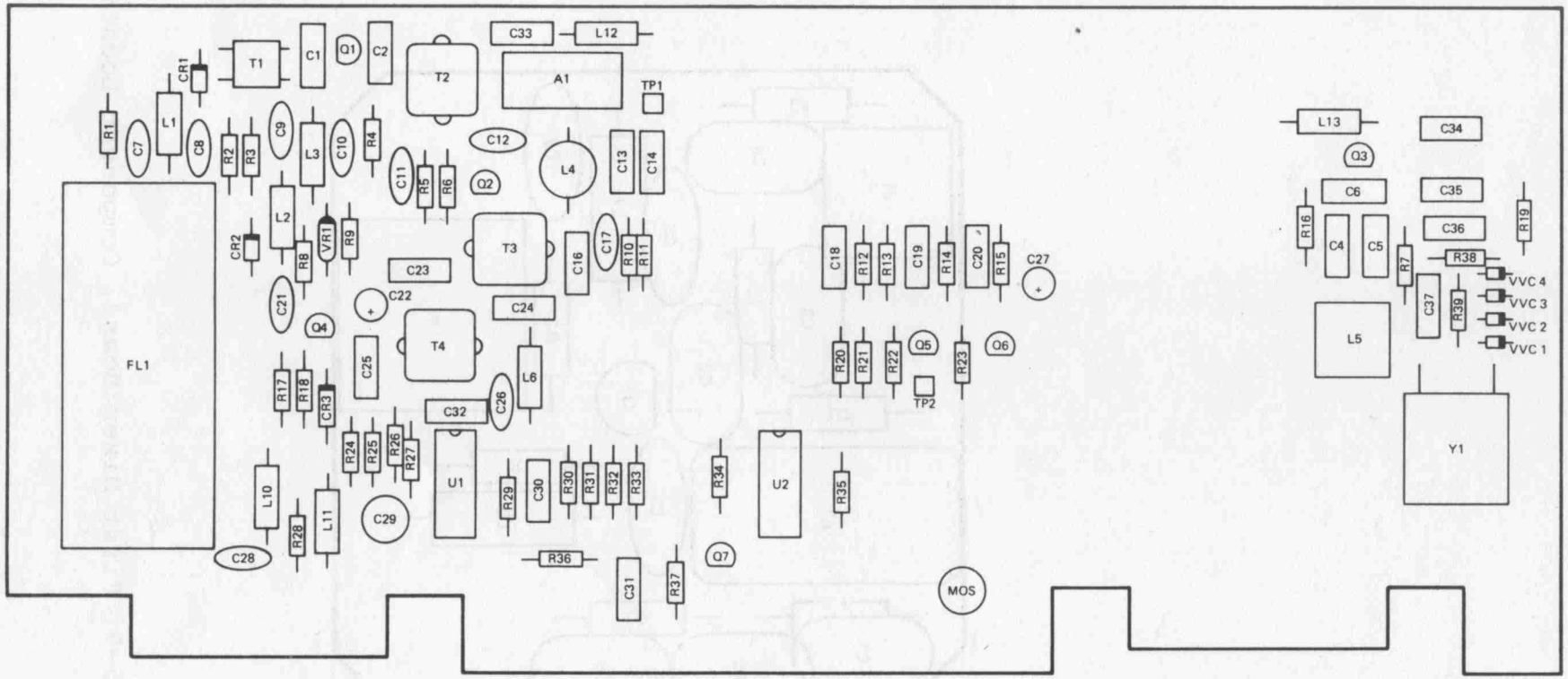

Figure 5-6 38 MHZ IF Board, Component Locations

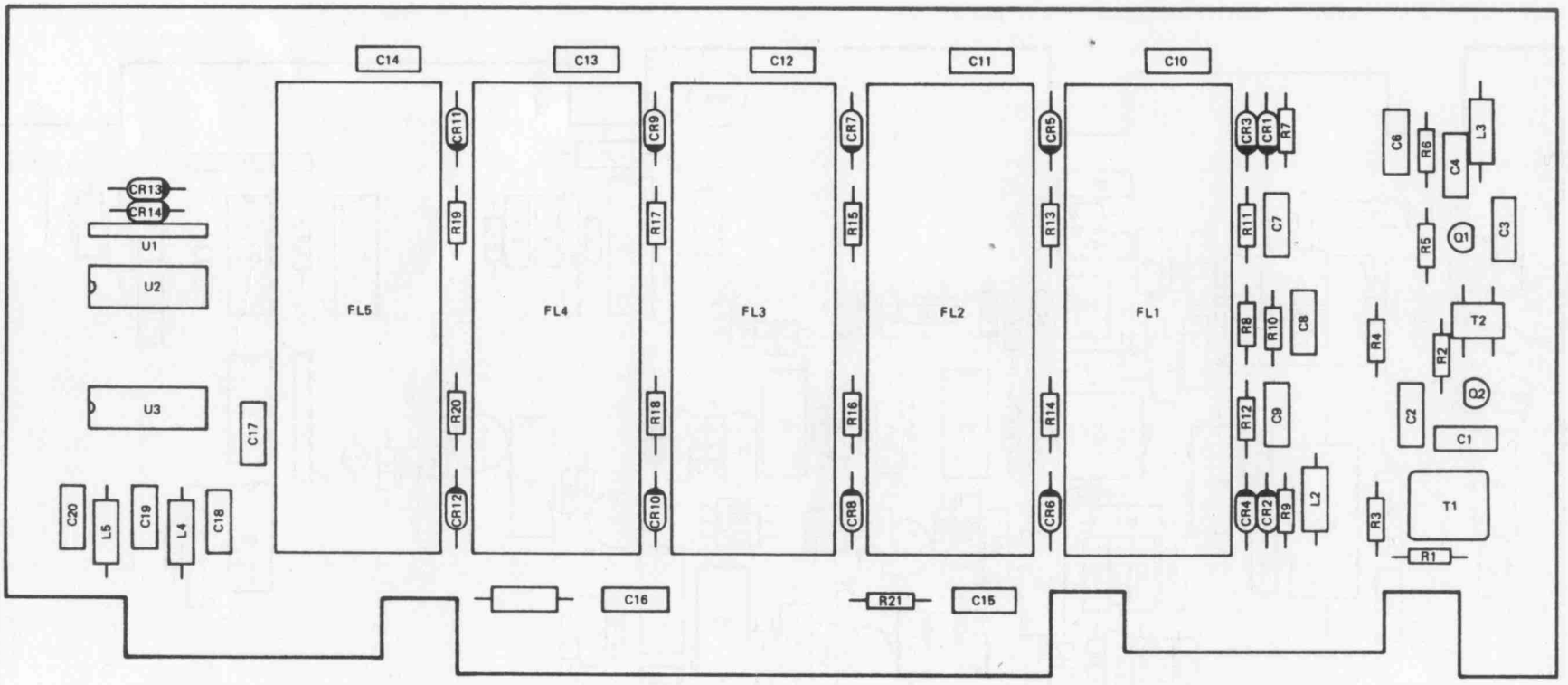

Figure 5-7 1.4 MHz IF Filter Board, Component Locations

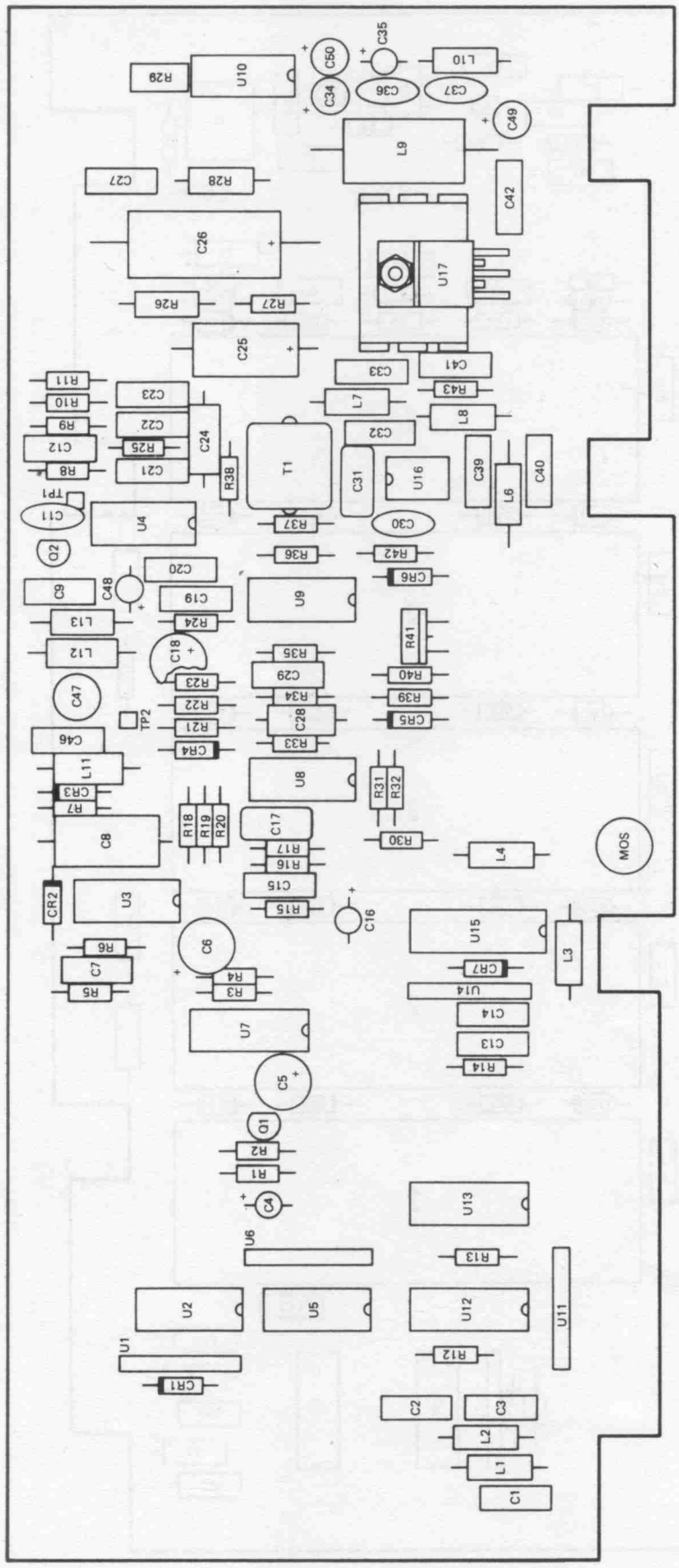

Figure 5-8 1.4 MHz IF/Demodulator Board, Component Locations

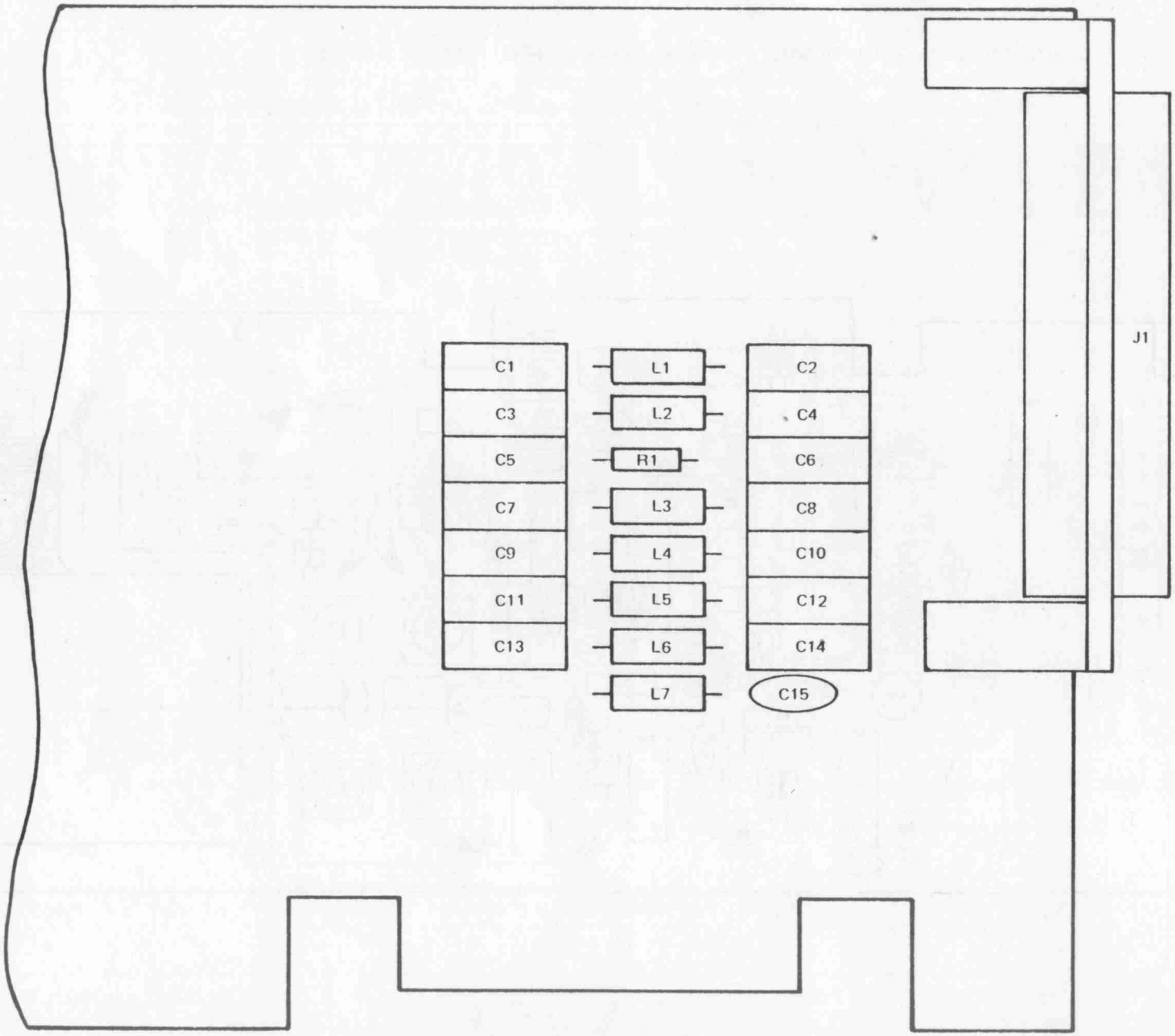

Figure 5-9 Remote Interface Board, Component Locations

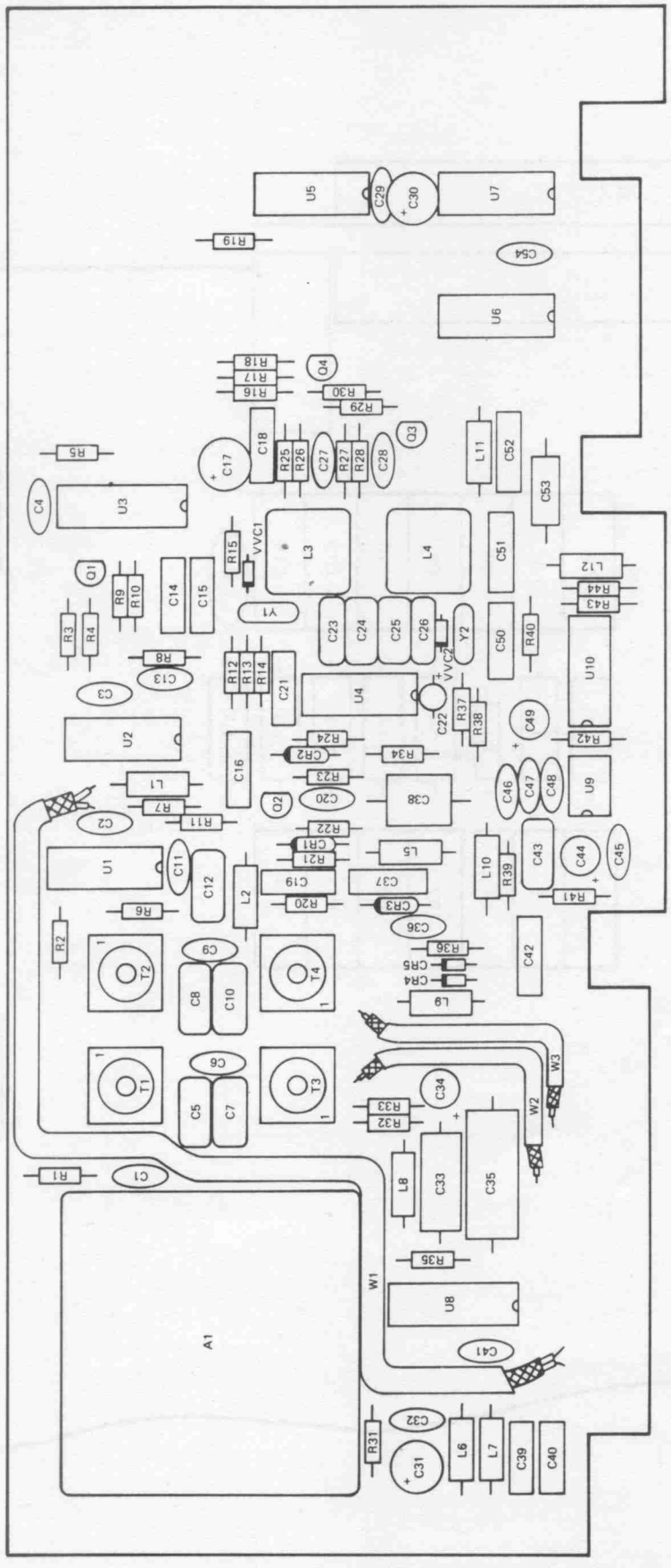

Figure 5-10 Reference Board, Component Locations

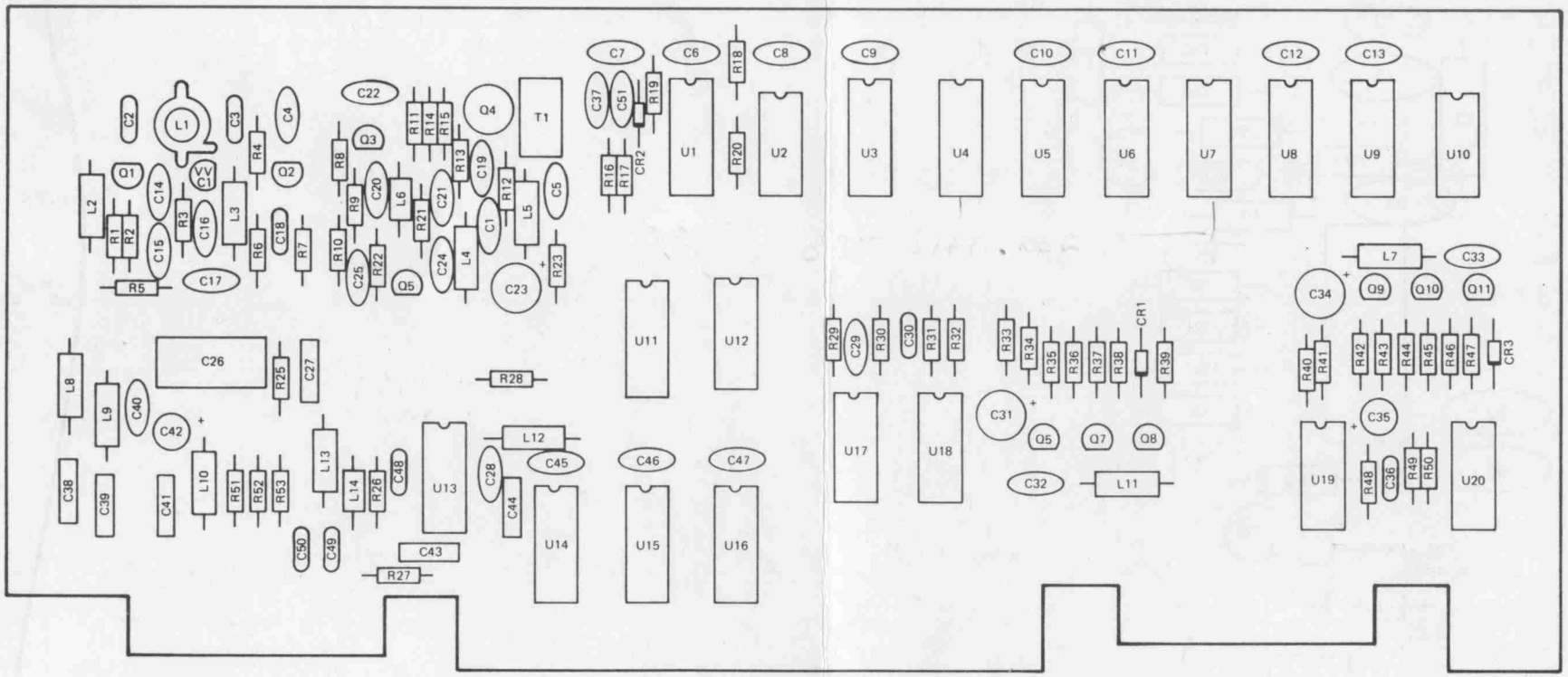

Figure 5-11 Programmable Divider Board, Component Location

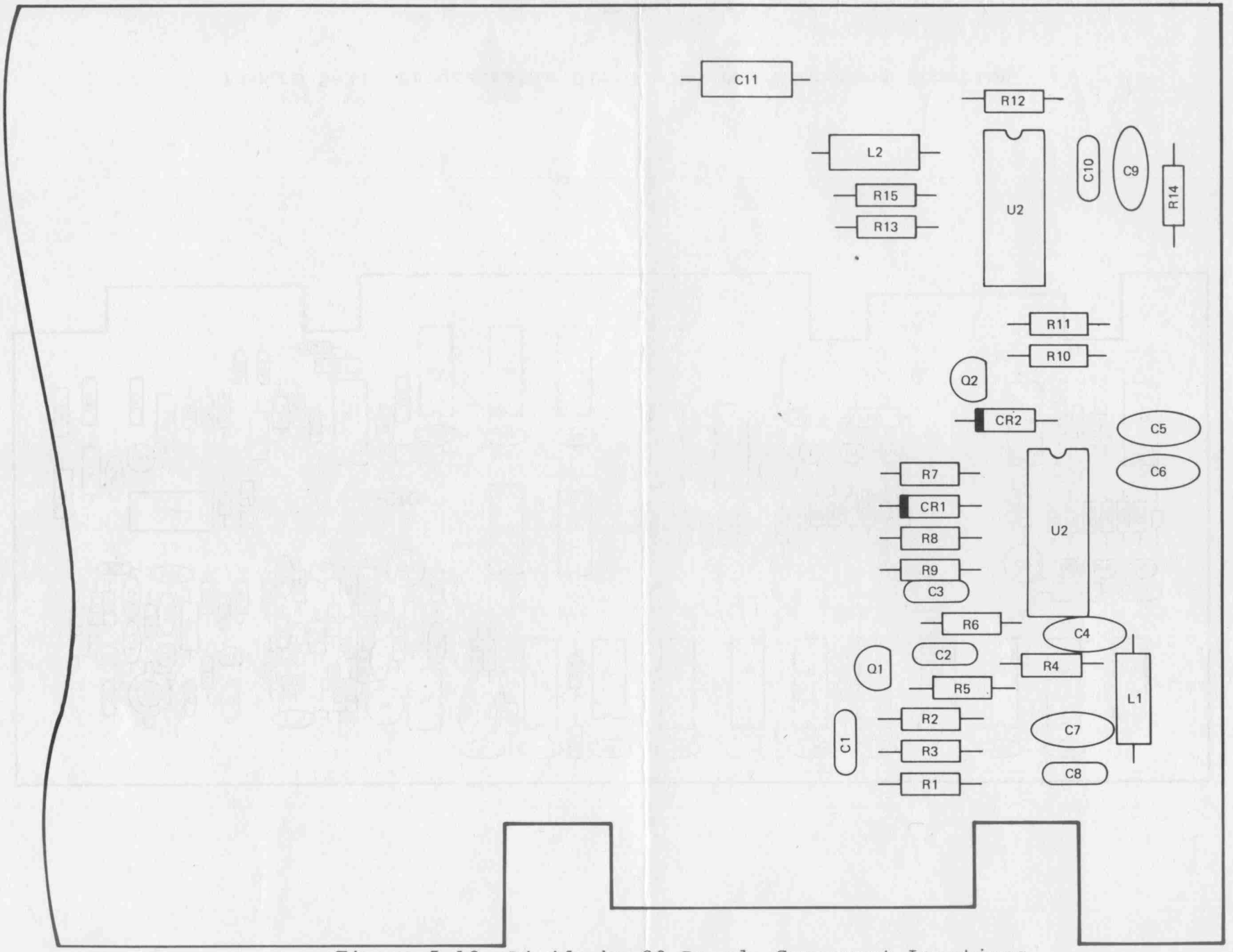

Figure 5-12 Divide by 20 Board, Component Locations

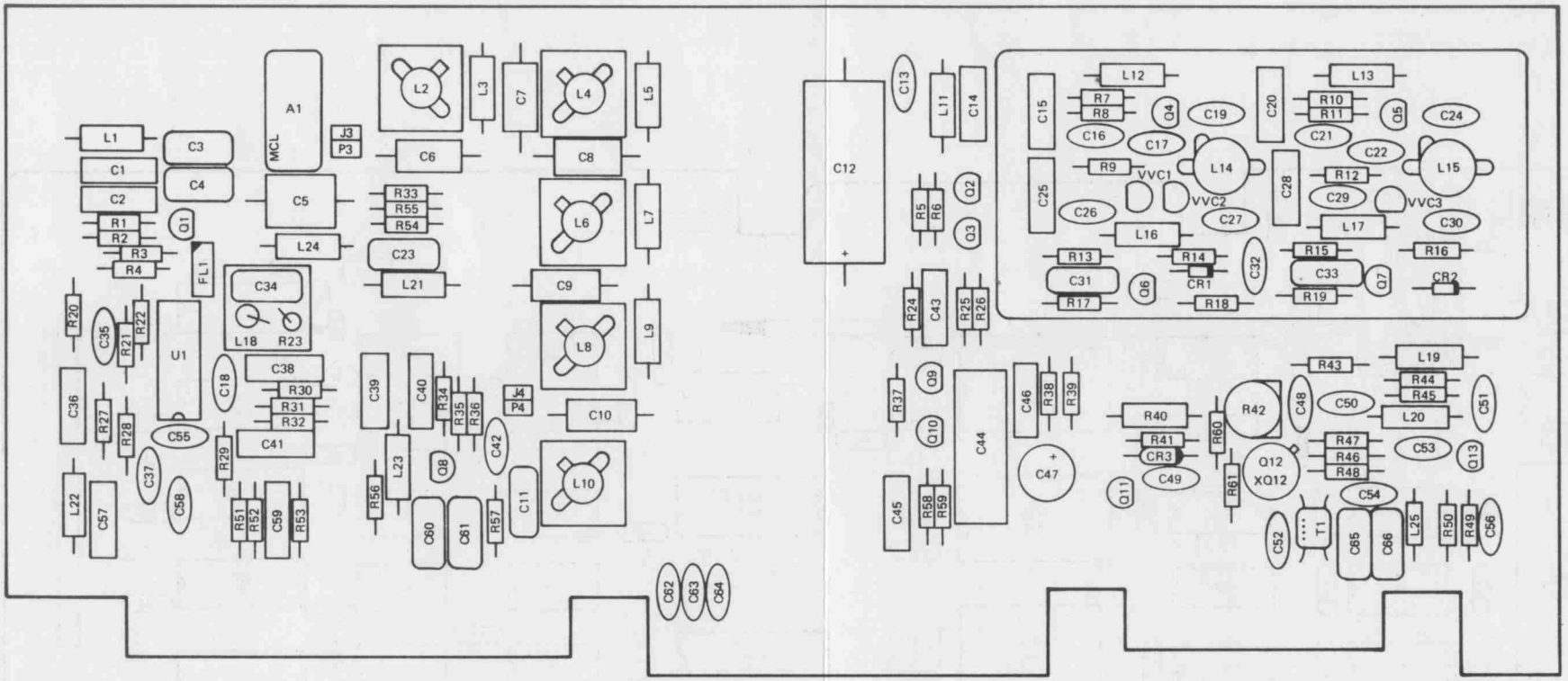

Figure 5-13 VCO Board, Component Locations

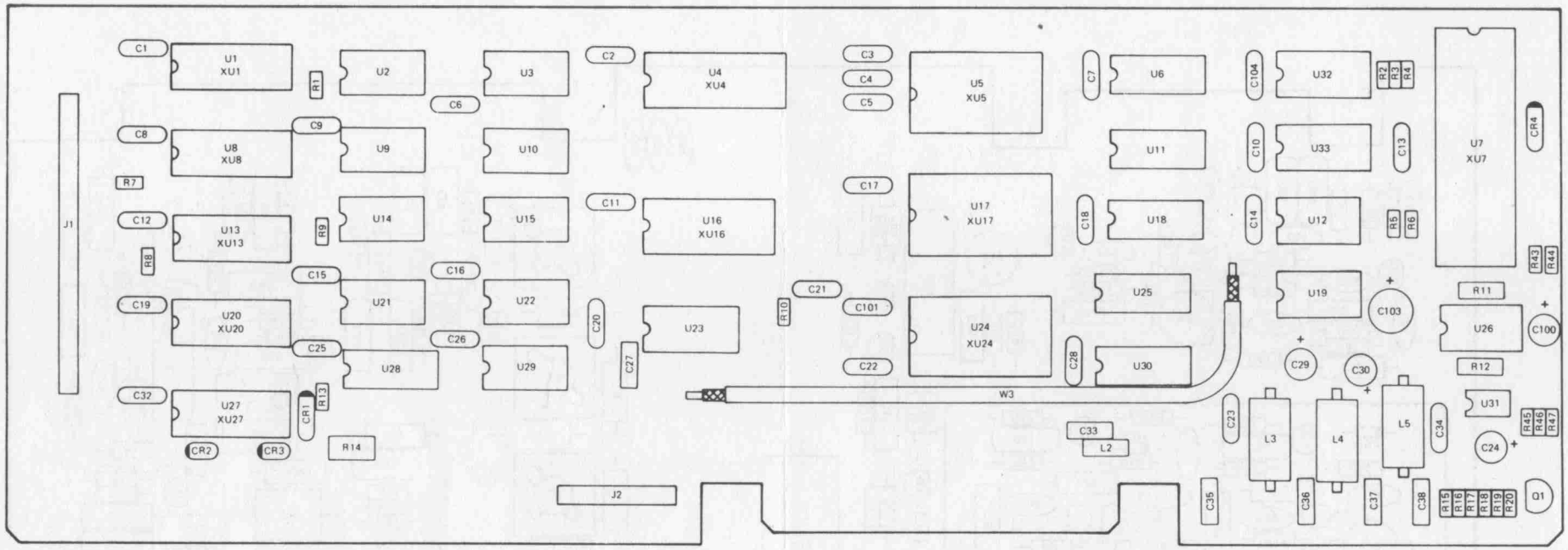

Figure 5-14 Microprocessor Board, Component Locations

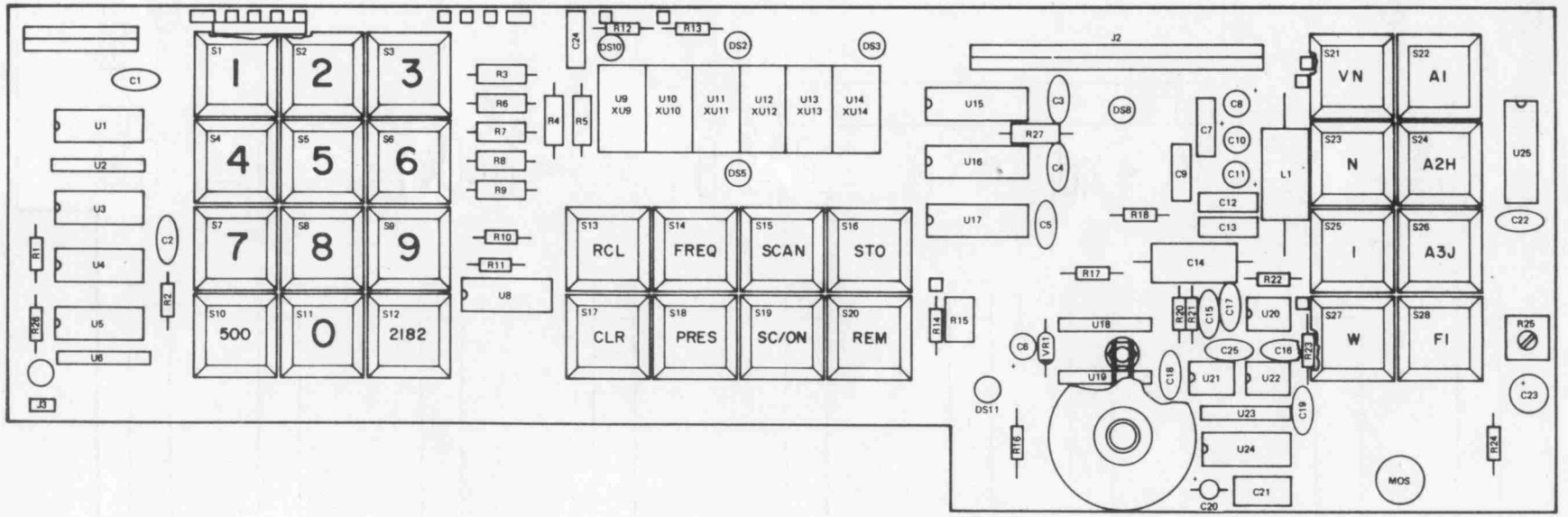

Figure 5-15 Display Board, Component Locations

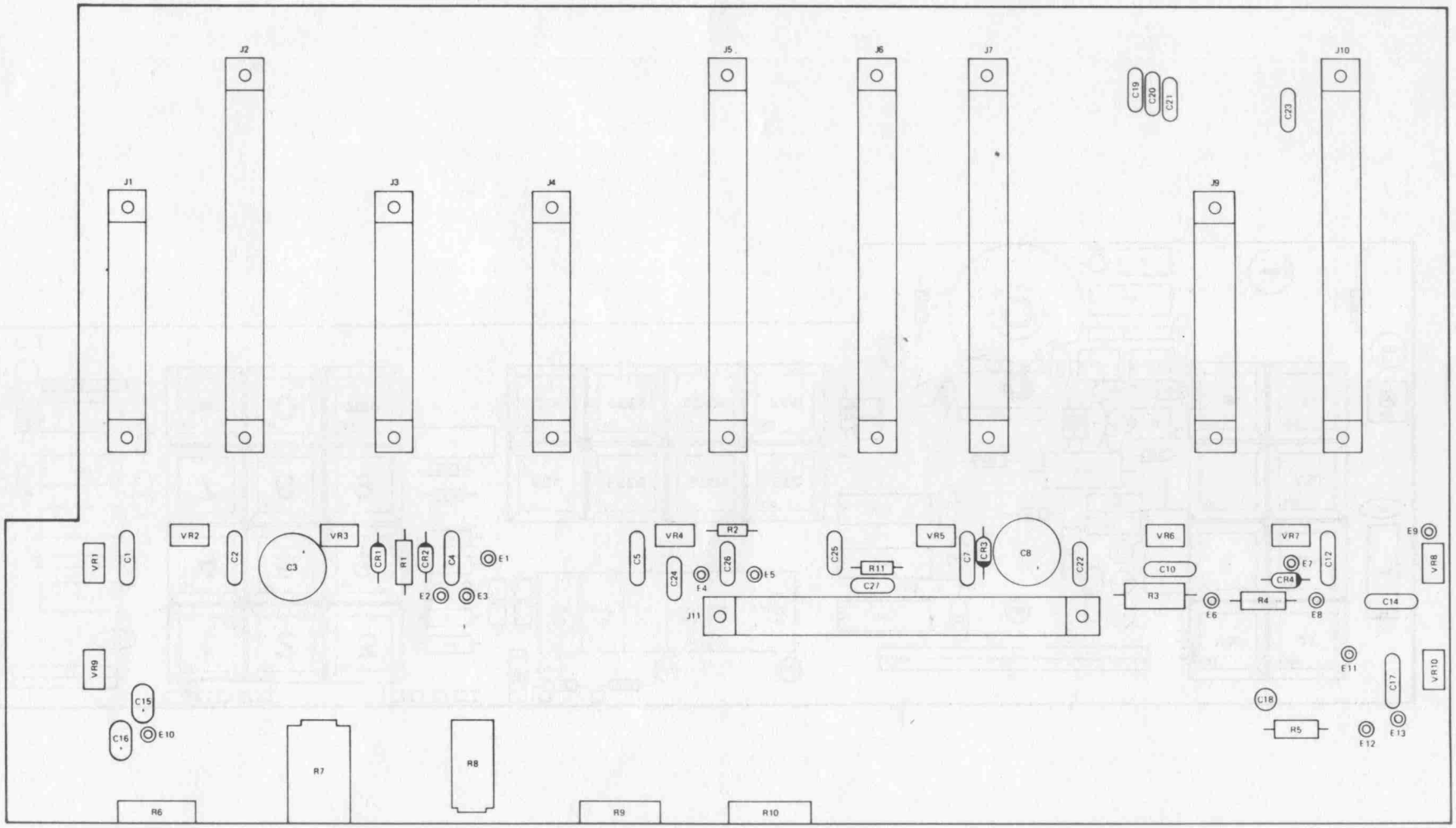

Figure 5-16 Chassis Interconnection Board, Component Locations

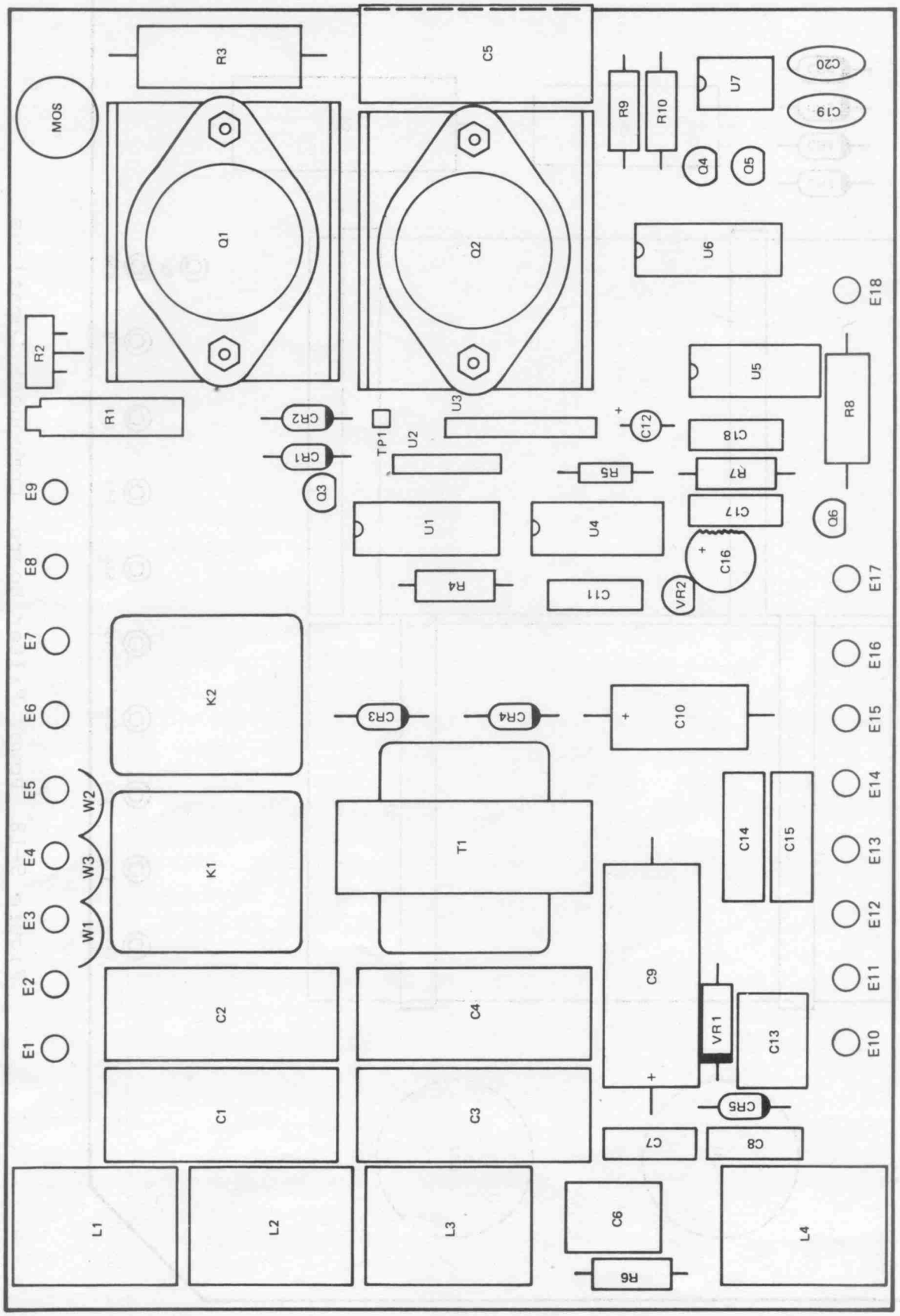

Figure 5-17 Power Relay Board, Component Locations

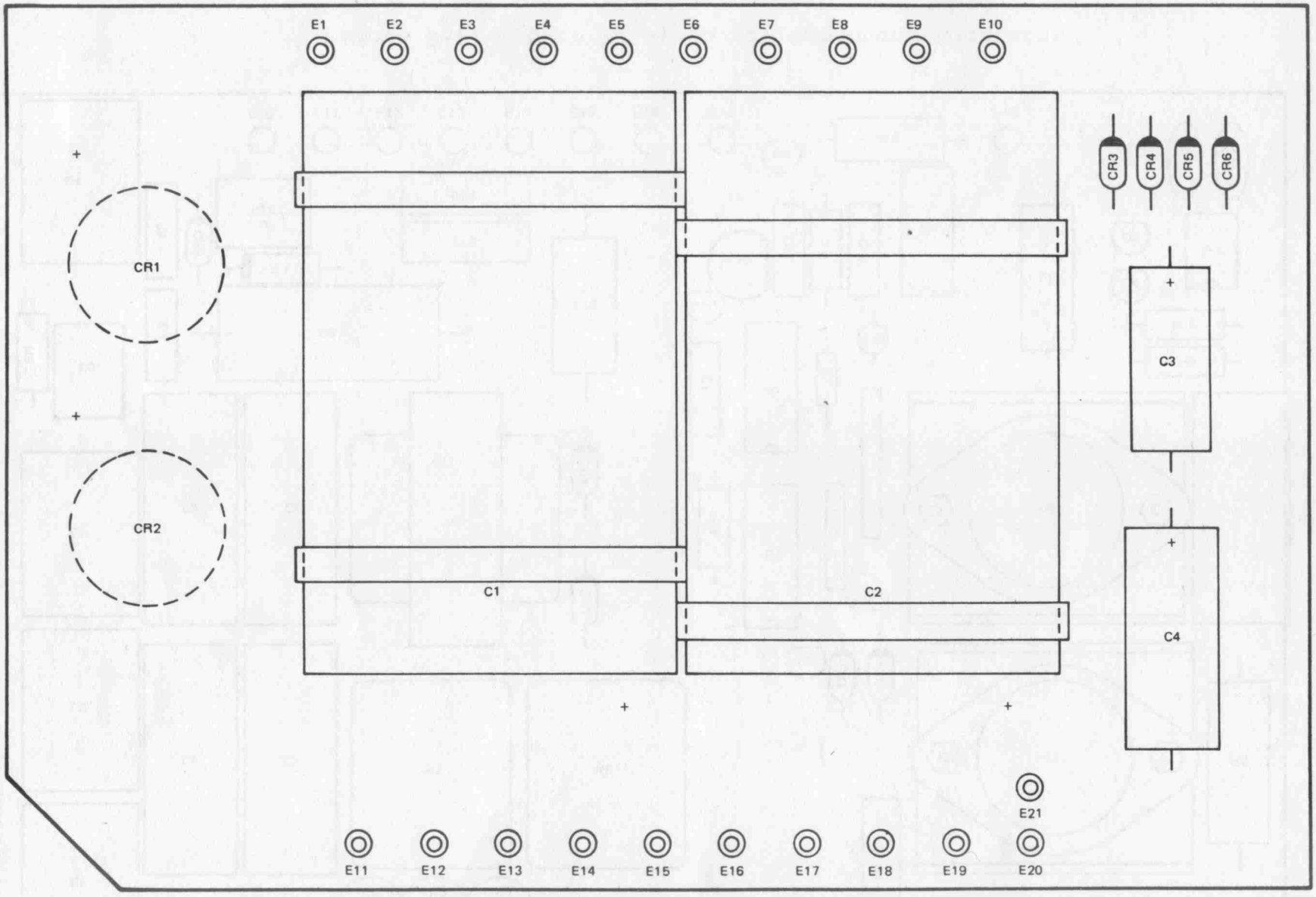

Figure 5-18 Power Filter Board, Component Locations